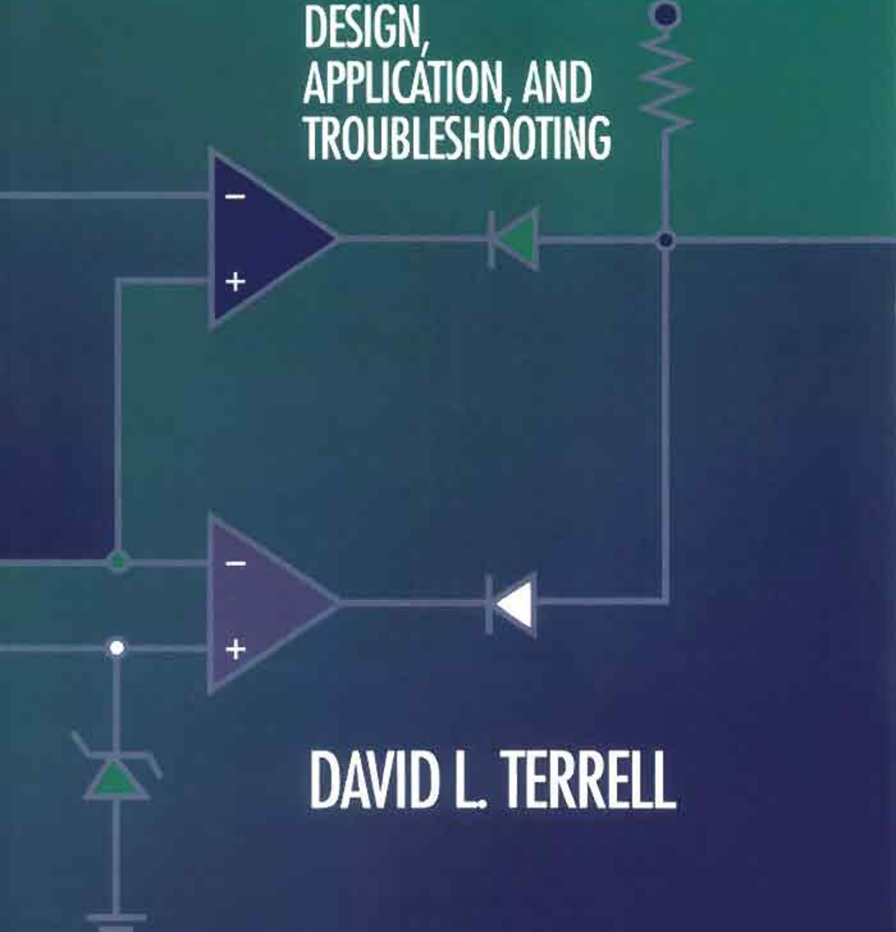
SECOND EDITION

Op Amps

DESIGN, APPLICATION, AND TROUBLESHOOTING



DAVID L. TERRELL

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Design, Application, and Troubleshooting

SECOND EDITION

David L. Terrell
President
Terrell Technologies, Inc.

Butterworth-Heinemann
Boston Oxford Melbourne Singapore Toronto Munich New Delhi Tokyo

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Many people have friends, many people have partners, and many people have spouses. But only a lucky few ever have all three in the same person. Thanks, Linda.

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PREFACE

What is the value of pi (π)? Is it 3? Is it 3.1? How about 3.14? Or perhaps you think 3.1415952653589793238462643383279 is more appropriate. Each of these answers is correct just as each of these answers is incorrect; they vary in their degrees of resolution and accuracy. The degree of accuracy is often proportional to the complexity or difficulty of computation. So it is with operational amplifier circuits, or all electronic circuits for that matter. The goal of this text is to provide workable tools for analysis and design of operational amplifier circuits that are free from the shrouds of complex mathematics and yet produce results that have a *satisfactory degree of accuracy*.

This book offers a subject coverage that is fairly typical for texts aimed at the postsecondary school market. The organization of each circuits chapter, however, is very consistent and provides the following information on each circuit presented:

1. *Theory of operation*. A discussion that describes what the circuit does, explains why it behaves the way it does, and identifies the purpose of each component. This section contains no mathematics, promotes an intuitive understanding of circuit operation, and is based on an application of basic electronics principles such as series and parallel circuits, Ohm's Law, Kirchhoff's Laws, and so on.
2. *Numerical analysis*. Techniques are presented that allow calculation of most key circuit parameters for an existing op amp circuit design. The mathematics is strictly limited to basic algebra and does not require (although it permits) the use of complex numbers.
3. *Practical design*. A sequential design procedure is described that is based on the preceding numerical analysis and application of basic electronics principles. The goals of each design are contrasted with the actual circuit performance measured in laboratory tests.

In addition to presenting these areas for each type of circuit, each circuits chapter has a discussion of troubleshooting techniques as they apply to the type of circuits discussed in that particular chapter.

The majority of this text treats the op amp as a quasi-ideal device. That is, only the nonideal parameters that have a significant impact on a particular design are considered. Chapter 10 offers a more thorough discussion of nonideal behavior and includes both AC and DC considerations.

The analytical and design methods provided in the text are not limited to a particular op amp. The standard 741 and its higher-performance companion, the MC1741SC, are frequently used as example devices because they are still used in major electronics schools. However, the equations and methodologies directly extend to newer, more advanced devices. In fact, because newer devices typically perform closer to the ideal op amp, the equations and methods frequently work even better for the newer op amps. To provide a perspective regarding the range of op amp performance that is available, Chapter 11 includes a comparison between a general-purpose op amp and a hybrid op amp, which has for example, a 5500 volts-per-microsecond slew rate as compared to the 0.5 volts-per-microsecond slew rate often found in general-purpose devices.

Every circuit in every circuits chapter has been constructed and tested in the laboratory. In the case of circuit design examples, the actual performance of the circuit was captured in the form of oscilloscope plots. The following test equipment was used to measure circuit performance:

1. Hewlett-Packard Model 8116A Pulse/Function Generator
2. Hewlett-Packard Model 54501A Digitizing Oscilloscope
3. Hewlett-Packard Think Jet Plotter
4. Heath Model 2718 Triple Output Power Supply

Items 1 to 3 were provided courtesy of Hewlett-Packard. This equipment delivered exceptional ease of use and accuracy of measurement, and produced a camera-ready plotter output of the scope displays. The oscilloscope plots presented in the text are unedited and represent the actual circuit performances, thus alleviating the confusion that is frequently encountered when the ideal waveform drawings typically presented in textbooks are contrasted with the actual results in the laboratory. Any deviations from the ideal that would have been masked by an artist's ideal drawings are there for your examination in the actual oscilloscope plots presented throughout this book.

Although this text is appropriate for use in a resident electronics school, the consistent and independent nature of the discussions for each circuit make it equally appropriate as a reference manual or handbook for working engineers and technicians.

So what is considered to be a *satisfactory degree of accuracy* in this text? On the basis of more than 20 years of experience as a technician, an engineer, and a classroom instructor, it is apparent to the author that most practical designs require tweaking in the laboratory before a final design evolves. That is, the engineer can design a circuit using the most appropriate models and the most extensive analysis, but the exact performance is rarely witnessed the first time the circuit is constructed. Rather, the paper design generally puts us close to the desired performance. Actual measurements on the circuit in a laboratory environment will then allow optimization of component values. The methods presented in this text, then, will produce designs that can deliver performance close to the original design goals. If tighter performance is required, then tweaking can be done in the laboratory . . . a step that would generally be required even if more elaborate methods were employed.

The majority of text material included in the first edition is retained in this second edition. Feedback from reviewers emphasized the point "Take nothing out . . . it's all important!" However, all known typographical errors and oversights that appeared in the first edition have been corrected here. We have also updated several references to actual A/D and D/A conversion products in Chapter 8, to identify newer products that are more readily available. Additionally, an instructor's answer key has been developed and is available from the publisher; it includes solutions to all end-of-chapter problems.

For reasons stated previously, we have elected to continue using the basic 741 as the primary op amp for use in the analysis and design examples. Clearly, the 741 is a mature product, but the analytical techniques presented work well with newer and more ideal op amps. Fortunately, the decision to focus on these older devices to satisfy the requirements of many school curriculums does not lessen the applicability of the material to programs that use higher-performance devices.

Your comments, criticisms, and recommendations for improvement of this text are welcomed. You may send your comments to the publisher; or alternatively, if you prefer you may send your comments directly to the author via e-mail to `feedback@terrelltech.com`. While visiting the Terrell Technologies, Inc., home page, you can also download other useful educational materials and software products. In early 1996, the company plans to have PSpice files available for all the op amp designs presented in this text; they will be available to be downloaded for free.

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There were countless professionals whose efforts contributed to the completion of this textbook. In particular, I want to express my appreciation to Jo Gilmore (Butterworth–Heinemann), Marilyn Rash (Ocean Publication Services), and Dianne Cannon Wood (Galley Slaves). I am also grateful for the valuable comments offered by Teresa Bowen and other reviewers of the original manuscript. My sincere thanks also go to Rick Lane of Hewlet-Packard whose assistance on this project was instrumental.

I want to acknowledge the support given by the manufacturers of the op amps and other components whose data sheets are included in the appendices of this book. Their cooperation greatly enhances the authenticity and utility of my efforts.

Finally, I want to thank the thousands of students who continue to ask, "Why didn't they just say that in the book?" and who reward their instructors by saying, "That's not so hard. It's easy when you do it that way!"

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CHAPTER ONE

Basic Concepts of the Integrated Operational Amplifier

1.1 OVERVIEW OF OPERATIONAL AMPLIFIERS

1.1.1 Brief History

Operational amplifiers began in the days of vacuum tubes and analog computers. They consisted of relatively complex differential amplifiers with feedback. The circuit was constructed such that the characteristics of the overall amplifier were largely determined by the type and amount of feedback. Thus the complex differential amplifier itself had become a building block that could function in different "operations" by altering the feedback. Some of the operations that were used included adding, multiplying, and logarithmic operations.

The operational amplifier continued to evolve through the transistor era and continued to decrease in size and increase in performance. The evolution continued through molded or modular devices and finally in the mid 1960s a complete operational amplifier was integrated into a single integrated circuit (IC) package. Since that time, the performance has continued to improve dramatically and the price has generally decreased as the benefits of high-volume production have been realized. The performance increases include such items as higher operating voltages, lower current requirements, higher current capabilities, more tolerance to abuse, lower noise, greater stability, greater power output, higher input impedances, and higher frequencies of operation.

In spite of all the improvements, however, the high-performance, integrated operational amplifier of today is still based on the fundamental differential amplifier. Although the individual components in the amplifier are not accessible to you, it will enhance your understanding of the op amp if you have some appreciation for the internal circuitry.

1.1.2 Review of Differential Voltage Amplifiers

You will recall from your basic electronics studies that a differential amplifier has two inputs and either one or two outputs. The amplifier circuit is not directly affected by the voltage on **either** of its inputs alone, but it is affected by **the difference** in voltage between the two inputs. This difference voltage is amplified by the amplifier and appears in the output in its amplified form. The amplifier may have a single output, which is referenced to common or ground. If so, it is called a single-ended amplifier. On the other hand, the output of the amplifier may be taken between two lines, neither of which is common or ground. In this case, the amplifier is called a double-ended or differential output amplifier.

Figure 1.1 shows a simple transistor differential voltage amplifier. More specifically, it is a single-ended differential amplifier. The transistors have a shared emitter bias so the combined collector current is largely determined by the –20-volt source and the 10-kilohm emitter resistor. The current through this resistor then divides (Kirchhoff's Current Law) and becomes the emitter currents for the two transistors. Within limits, the total emitter current remains fairly constant and simply diverts from one transistor to the other as the signal or changing voltage is applied to the bases. In a practical differential amplifier, the emitter network generally contains a constant current source.

Now consider the relative effect on the output if the input signal is increased with the polarity shown. This will decrease the bias on Q_2 while increasing the bias on Q_1. Thus a larger portion of the total emitter current is diverted through Q_1 and less through Q_2. This decreased current flow through the collector resistor for Q_2 produces less voltage drop and allows the output to become more positive.

If the polarity of the input were reversed, then Q_2 would have more current flow and the output voltage would decrease (i.e., become less positive).

Suppose now that both inputs are increased or decreased in the same direction. Can you see that this will affect the bias on both of the transistors in the same way? Since the total current is held constant and the relative values for each transistor did not change, then both collector currents remain constant. Thus the output does not reflect a change when both inputs are altered in the same way. This latter effect gives rise to the name *differential amplifier*. It only amplifies the difference between the two inputs, and is relatively unaffected by the absolute values applied to each input. This latter effect is more pronounced when the circuit uses a current source in the emitter circuit.

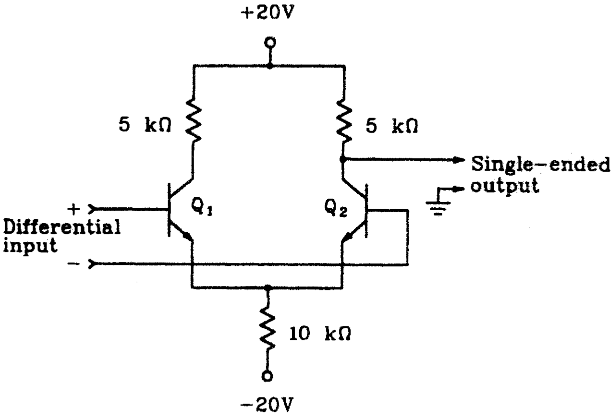


FIGURE 1.1 A simple differential voltage amplifier based on transistors.

In certain applications, one of the differential inputs is connected to ground and the signal to be amplified is applied directly to the remaining input. In this case the amplifier still responds to the difference between the two inputs, but the output will be in or out of phase with the input signal depending on which input is grounded. If the signal is applied to the (+) input, with the (–) input grounded, as labeled in Figure 1.1, then the output signal is essentially in phase with the input signal. If, on the other hand, the (+) input is grounded and the input signal is applied to the (–) input, then the output is essentially 180 degrees out of phase with the input signal. Because of the behavior described, the (–) and (+) inputs are called the *inverting* and *noninverting inputs*, respectively.

1.1.3 A Quick Look Inside the IC

Figure 1.2 shows the schematic diagram of the internal circuitry for a common integrated circuit op amp. This is the 741 op amp which is common in the industry. It is not particularly important for you to understand the details of the internal operation. Nor is it worth your while to trace current flow through the internal components. The internal diagram is shown here for the following reasons:

1. To emphasize the fact that the op amp is essentially an encapsulated circuit composed of familiar components
2. To show the differential inputs on the op amp
3. To gain an understanding of the type of circuit driving the output of the op amp

You can see that the entire circuit is composed of transistors, resistors, and a single 30 picofarad (pF) capacitor. A closer examination shows that the inverting and noninverting inputs go directly to the bases of two transistors connected as a differential amplifier. The emitter circuit of this differential pair is supplied by a

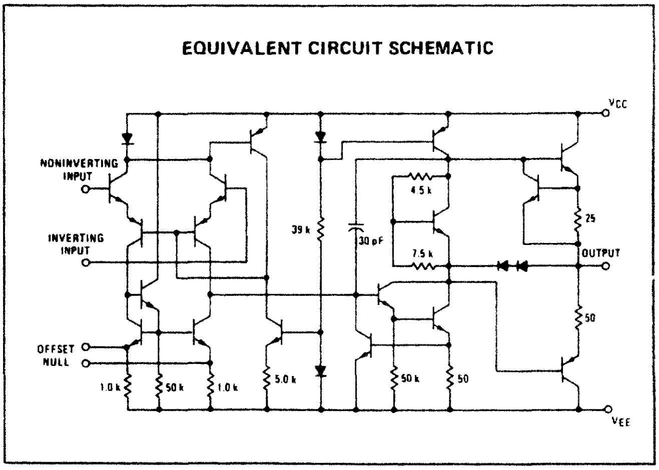


FIGURE 1.2 The internal schematic for an MC1741 op amp. (Copyright of Motorola, Inc. Used by permisssion.)

constant current source. If you examine the output circuitry, you can see that it resembles that of a complementary-symmetry amplifier. The output is pulled closer to the positive supply whenever the upper output transistor conducts harder. Similarly, if the lower output transistor were to turn on harder, then the output would be pulled in a negative direction. Also note the low values of resistances in the output circuit.

The inputs labeled "offset null" are provided to allow compensation for imperfect circuitry. Use of these inputs is discussed at a later point.

1.1.4 A Survey of Op Amp Applications

Now you know where op amps came from, what they are made of, and a few of their characteristics. But what uses are there for an op amp in the industry? Although the following is certainly not an exhaustive list, it does serve to illustrate the range of op amp applications.

Amplifiers. Op amps are used to amplify signals that range from DC through the higher radio frequencies (RF). The amplifier can be made to be frequency selective (i.e., act as a filter) much like the tone control on your favorite stereo system. It may be used to maintain a constant output in spite of changing input levels. The output can produce a compressed version of the input to reduce the range needed to represent a certain signal. The amplifier may respond to microvolt signals originating in a transducer, which is used to measure temperature, pressure, density, acceleration, and so on. The gain of the amplifier can be controlled by a digital computer, thus extending the power of the computer into the analog world.

Oscillators. The basic op amp can be connected to operate as an oscillator. The output of the oscillator may be sinusoidal, square, triangular, rectangular, sawtooth, exponential, or other shape. The frequency of oscillation may be stabilized by a crystal or controlled by a voltage or current from another circuit.

Regulators. Op amps can be used to improve the regulation in power supplies. The actual output voltage is compared to a reference voltage and the difference is amplified by an op amp and used to correct the power supply output voltage. Op amps can also be connected to regulate and/or limit the current in a power supply.

Rectification. Suppose you want to build a half-wave rectifier with a peak input signal of 150 millivolts. This is not enough to forward bias a standard silicon diode. On the other hand, an op amp can be configured to provide the characteristics of an ideal diode with 0 forward voltage drop. Thus it can rectify very small signals.

Computer Interfaces. The op amp is an integral part of many circuits used to convert analog signals representing real-world quantities (such as temperature, RPM, pressure, and so forth) into corresponding digital signals that can be manipulated by a computer. Similarly, the op amp is frequently used to convert the digital output of a computer into an equivalent analog form for use by industrial devices (such as motors, lights, and solenoids).

Fields of Application. Op amps find use in such diverse fields as medical electronics, industrial electronics, agriculture, test equipment, consumer products, and automotive products. It has become a basic building block for analog systems and for the analog portion of digital systems.

1.2 REVIEW OF IMPORTANT BASIC CONCEPTS

Throughout my career in the electronics field, I have known certain individuals whose observable skills in circuit analysis far exceeded most others with similar levels of education and experience. These people all have one definite thing in common: They have an unusually strong mastery of basic—really basic—electronics. And they have the ability to look at a complex, unfamiliar circuit and see a combination of simple circuits that can be analyzed with such tools as Ohm's and Kirchhoff's Laws. We will strive to develop these two skills as we progress through the text.

This portion of the text provides a condensed review of several important laws and theorems that are used to analyze electronic circuits. A mastery of these basic ideas will greatly assist you in understanding and analyzing the operation of the circuits presented in the remainder of the text and encountered in industry.

1.2.1 Ohm's Law

The basic forms of Ohm's Law are probably known to everyone who is even slightly trained in electronics. The three forms are

$$\boxed{V = IR \qquad (1.1)}$$

$$\boxed{I = \frac{V}{R} \qquad (1.2)}$$

$$\boxed{R = \frac{V}{I} \qquad (1.3)}$$

where V (or E) represents the applied voltage (volts), R represents the resistance of the circuit (ohms), and I represents the current flow (amperes). Your concept of Ohm's Law, however, should extend beyond the arithmetic operations required to solve a problem. You need to develop an intuitive feel for the circuit behavior. For example, without the use of mathematics, you should know that if the applied voltage to a particular circuit is increased while the resistance remains the same, then the value of current in the circuit will also increase proportionately. Similarly, without mathematics, it needs to be obvious to you that an increased current flow through a fixed resistance will produce a corresponding increase in the voltage drop across the resistance.

Many equations presented in this text appear to be new and unique expressions to describe the operation of op amp circuits. When viewed more closely, however, they are nothing more than an application of Ohm's Law. For example, consider the following expression:

$$i_X = \frac{v_I - v_D}{R_I}$$

Once the subtraction has been completed in the numerator, which is like computing the value of two batteries in series, the problem becomes a simple Ohm's Law problem as in Equation (1.2).

For a test of your intuitive understanding of Ohm's Law as applied to series-parallel circuits, try to evaluate the problem shown in Figure 1.3 without resorting to the direct use of mathematics. In the figure, no numeric values are given for the various components. The value of R_3 is said to have increased (i.e., has more resistance). What will be the relative effects on the three current meters (increase, decrease or remain the same)? Try it on your own before reading the next paragraph.

Your reasoning might go something like this. If R_3 increases in value, then the current (I_3) through it will surely decrease. Since R_3 increased in value, the parallel combination of R_2 and R_3 will also increase in effective resistance. This increase in parallel resistance will drop a greater percentage of the applied voltage. This increased voltage across R_2 will cause I_2 to increase. Since the parallel combination of R_2 and R_3 have increased in resistance, the total circuit resistance is greater, which means that total current will decrease. Since the total current flows through R_1, the value of I_1 will show a decrease.

This example illustrates an intuitive, nonmathematical method of circuit analysis. Time spent in gaining mastery in this area will pay rewards to you in the form of increased analytical skills for unfamiliar circuits.

Ohm's Law also applies to AC circuits with or without reactive components. In the case of AC circuits with reactive devices, however, all voltages, currents, and impedances must be expressed in their complex form (e.g., $2 - j5$ would represent a series combination of a 2-ohm resistor and a 5-ohm capacitive reactance).

1.2.2 Kirchhoff's Current Law

Kirchhoff's Current Law tells us that all of the current entering a particular point in a circuit must also leave that point. Figure 1.4 illustrates this concept with sev-

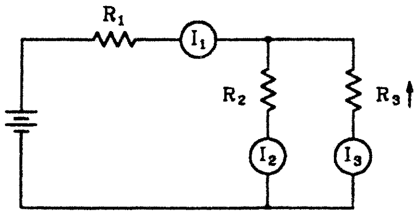


FIGURE 1.3 How does an increase in the resistance of R_3 affect the currents I_1, I_2, and I_3?

eral examples. In each case, the current entering and leaving a given point is the same. This law is generally stated mathematically in the form of

$$I_T = I_1 + I_2 + I_3 + \ldots I_N \tag{1.4}$$

where I_T is the total current leaving a point (for instance) and I_1, I_2, and so on, are the various currents entering the point. In the case of Figure 1.4(c), we can apply Equation (1.4) as

$$I_4 = I_1 + I_2 + I_3$$

Here again, though, it is important for you to strive to develop an intuitive, nonmathematic appreciation for what the law is telling you.

Consider the examples in Figure 1.5. Without using your calculator, can you estimate the effect on the voltage drop across R_1 when resistor R_3 opens? Try it before reading the next paragraph.

In the first case, Figure 1.5(a), your reasoning might be like this. Since the open resistor (R_3) was initially very small compared to parallel resistor R_2, it will have a dramatic effect on total current when it opens. That is, Kirchhoff's Current Law would tell us that the total current (I_1) is composed of I_2 and I_3. Since R_3 was initially much smaller than R_2, its current will be much greater (Ohm's Law). Therefore, when R_3 opens, the major component of current I_1 will drop to zero. This reduced value of current through R_1 will greatly reduce the voltage drop across R_1.

In the second case, Figure 1.5(b), R_3 is much larger than the parallel resistor R_2 and therefore contributes very little to the total current I_1. When R_3 opens, there will be no significant change in the voltage across R_1.

Again be reminded of the value of a solid intuitive view of electronic circuits.

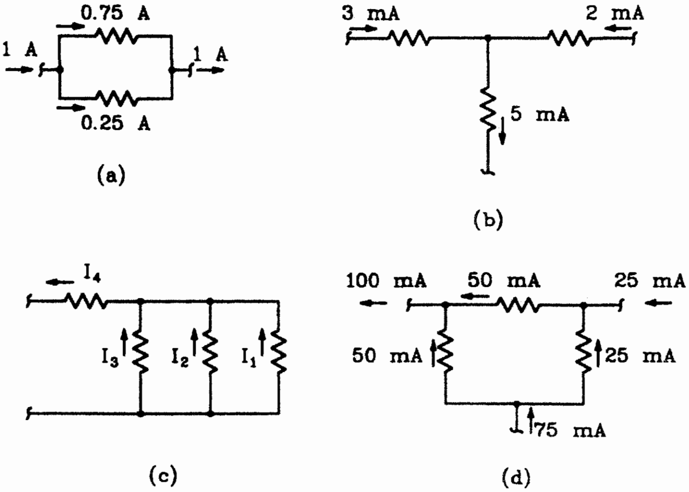
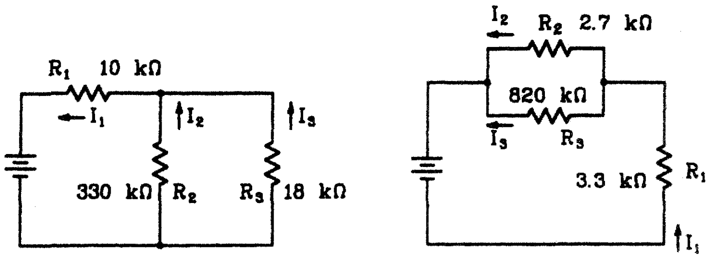


FIGURE 1.4 Examples of Kirchhoff's Current Law illustrate that the current entering a point must equal the current leaving that same point.


R_1 10 kΩ
I_1
I_2
I_3
330 kΩ R_2
R_3 18 kΩ
I_2 R_2 2.7 kΩ
820 kΩ
I_3 R_3
3.3 kΩ R_1
I_1

(a) (b)

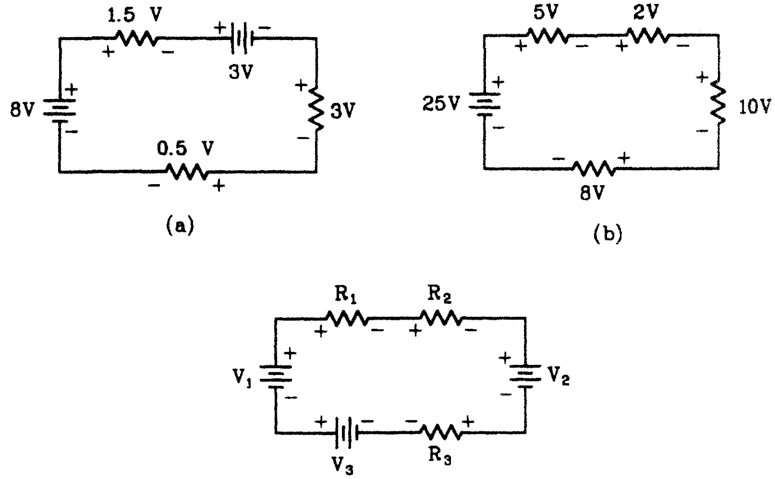
FIGURE 1.5 Estimate the effect on circuit operation if R_3 were to become open.

Kirchhoff's Current Law can also be used to analyze AC circuits with reactive components provided the circuit values are expressed in complex form.

1.2.3 Kirchhoff's Voltage Law

Kirchhoff's Voltage Law basically says that all of the voltage sources in a closed loop must be equal to the voltage drops. That is, the net voltage (sources + drops) is equal to zero. Figure 1.6 shows some examples. This law is most often stated mathematically in a form such as

$$V_1 + V_2 + V_{APP} = 0 \tag{1.5}$$


1.5 V
3V
8V
3V
0.5 V
5V
2V
25V
10V
8V
R_1
R_2
V_1
V_2
V_3
R_3

(a) (b) (c)

FIGURE 1.6 Examples of Kirchhoff's Voltage Law illustrate the sum of all voltages in a closed loop must equal zero.

In the case of Figure 1.6(c), we apply Equation (1.5) as

$$+V_1 - V_{R_1} - V_{R_2} - V_2 - V_{R_3} + V_3 = 0$$

Another concept that is closely related to Kirchhoff's Voltage Law is the determination of voltages at certain points in the circuit **with respect to** voltages at other points. Consider the circuit in Figure 1.7. It is common to express circuit voltage with respect to ground. Voltages such as $V_B = 5$ volts, $V_D = -2$ volts, and $V_A = 8$ volts are voltage levels with respect to ground. In our analysis of op amp circuits, it will also be important to determine voltages with respect to points other than ground. The following is an easy two-step method:

1. Label the polarity of the voltage drops
2. Start at the reference point and move toward the point in question. As you pass through each component, add (algebraically) the value of the voltage drop using the polarity nearest the end you exit.

For example, let us determine the voltage at point *A* with respect to point *C* in Figure 1.7. Step one has already been done. We will begin at point C (reference point) and progress in either direction toward point *A*, combining the voltage drops as we go. Let us choose to go in a counterclockwise direction because that is the shortest path. Upon leaving R_2 we get +4 volts, upon leaving R_1 we get +3 volts, which adds to the previous +4 volts to give us a total of +7 volts. Since we are now at point *A* we have our answer of +7 volts. This is an important concept and one that deserves practice.

Kirchhoff's Voltage Law can also be used to analyze AC circuits with reactive components provided the circuit values are expressed in complex form.

1.2.4 Thevenin's Theorem

Thevenin's Theorem is a technique that allows us to convert a circuit (often a complex circuit) into a simple equivalent circuit. The equivalent circuit consists of a constant voltage source and a single series resistor called the *Thevenin voltage* and *Thevenin resistance,* respectively. Once the values of the equivalent circuit have been calculated, subsequent analysis of the circuit becomes much easier.

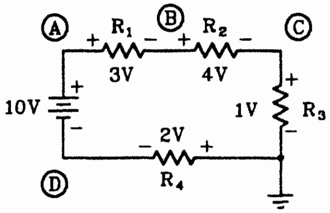


FIGURE 1.7 A circuit used to illustrate the concept of reference points.

You can obtain the Thevenin equivalent circuit by applying the following sequential steps:

1. Short all voltage sources and open all current sources. (Replace all sources with their internal impedance if it is known.) Also open the circuit at the point of simplification.
2. Calculate the value of Thevenin's resistance as seen from the point of simplification.
3. Replace the voltage and current sources with their original values and open the circuit at the point of simplification.
4. Calculate Thevenin's voltage at the point of simplification.
5. Replace the original circuit components with the Thevenin equivalent for subsequent analysis of the circuit beyond the point of simplification.

Consider, for example, the circuit in Figure 1.8. Here four different values of R_x are connected to the output of a voltage divider circuit. The value of loaded voltage is to be calculated. Without a simplification theorem such as Thevenin's Theorem, each resistor value would require several computations. Now let us apply Thevenin's Theorem to the circuit.

First we will define the point of simplification to be the place where R_x is connected. This is shown in Figure 1.9(a). The voltage source is shorted and the

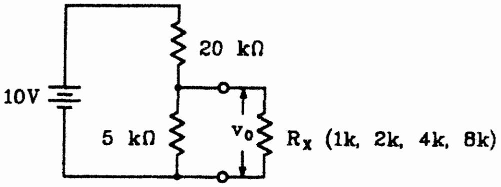


FIGURE 1.8 Determine the voltage V_O for each of the values of R_X.

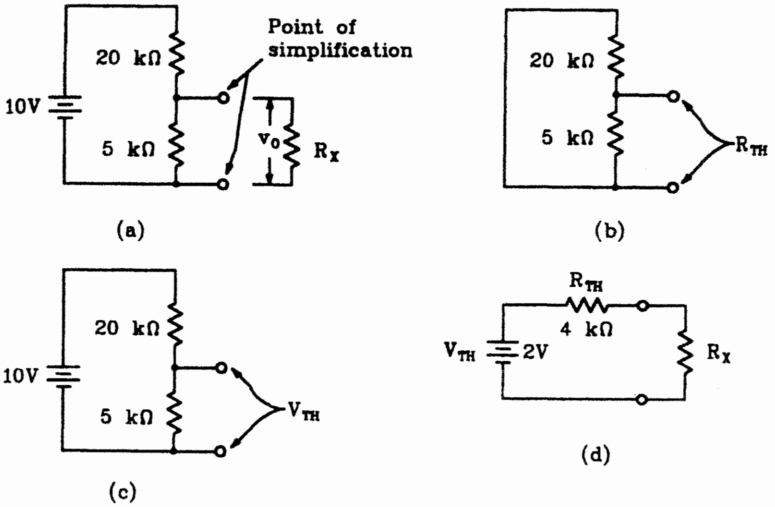


FIGURE 1.9 Thevenizing the circuit of Figure 1.8.

circuit is opened at the point of simplification in Figure 1.9(b). We can now calculate the Thevenin resistance (R_{TH}). By inspection, we can see that the 5-kilohm and the 20-kilohm resistors are now in parallel. Thus the Thevenin resistance is found in this case by the parallel resistor equation:

$$R_T = \frac{R_1 R_2}{R_1 + R_2} \tag{1.6}$$

In this particular case,

$$\begin{aligned} R_{TH} &= \frac{5\ k\Omega \cdot 20\ k\Omega}{5\ k\Omega + 20\ k\Omega} \\ &= \frac{100 \times 10^6}{25 \times 10^3} \\ &= 4\ k\Omega \end{aligned}$$

Next we determine the Thevenin voltage by replacing the sources (step 3). This is shown in Figure 1.9(c). The voltage divider equation, Equation (1.7), is used in this case to give us the value of Thevenin's voltage.

$$V_{R_1} = \left(\frac{R_1}{R_1 + R_2}\right) V_{APP} \tag{1.7}$$

That is,

$$\begin{aligned} V_{TH} &= \left(\frac{5\ k\Omega}{5\ k\Omega + 20\ k\Omega}\right) \times 10\ V \\ &= 0.2 \times 10\ V \\ &= 2\ V \end{aligned}$$

Figure 1.9(d) shows the Thevenin equivalent circuit. Calculations for each of the values of R_x can now be quickly computed by simply applying the voltage divider equation. The value of Thevenin's Theorem would be even more obvious if the original circuit were more complex.

The preceding discussion was centered on resistive DC circuits. The techniques described, however, apply equally well to AC circuits with inductive and/or capacitive components. The voltages and impedances are simply expressed in their complex form (e.g., $5 + j7$ would represent a 5-ohm resistance and a 7-ohm reactance).

1.2.5 Norton's Theorem

Norton's Theorem is similar to Thevenin's Theorem in that it produces an equivalent, simplified circuit. The major difference is that the equivalent circuit is composed of a current source and a parallel resistance rather than a voltage source and a series resistance like the Thevénin equivalent. The sequential steps for obtaining the Norton equivalent circuit are as follows:

1. Short all voltage sources and open all current sources (replace all sources with their internal impedance if it is known). Also open the circuit at the point of simplification.
2. Calculate the value of Norton's resistance as seen from the point of simplification.
3. Replace the voltage and current sources with their original values and short the circuit at the point of simplification.
4. Calculate Norton's current at the point of simplification.
5. Replace the original circuit components with the Norton's equivalent for subsequent analysis of the circuit beyond the point of simplification.

Figure 1.10 shows these steps as they apply to the circuit given in Figure 1.8. Once the equivalent circuit has been determined, the various values of R_x can be connected and the resulting voltage calculated. The calculations, though, are simple current divider equations.

Norton's Theorem can also be used to analyze AC circuits with reactive components provided the circuit values are expressed in complex form.

1.2.6 Superposition Theorem

The Superposition Theorem is most useful in analyzing circuits that have multiple voltage or current sources. Essentially it states that the net effect of all of the sources can be determined by calculating the effect of each source singly and then combining the individual results. The steps are

1. For each source, compute the values of circuit current and voltage with all of the remaining sources replaced with their internal impedances. (We generally short voltage sources and open current sources.)

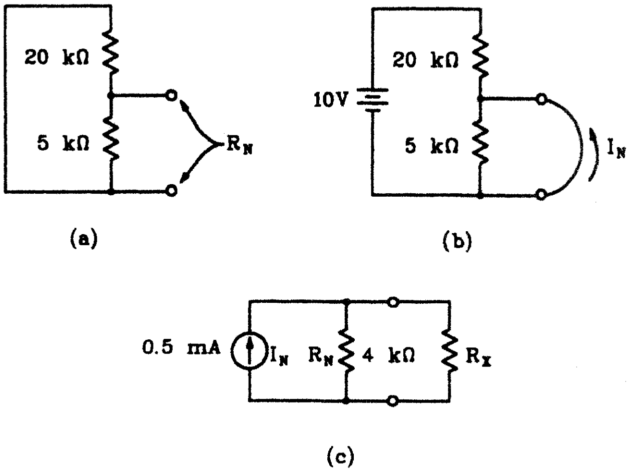


FIGURE 1.10 Determining the Norton equivalent for the circuit of Figure 1.8.

2. Combine the individual voltages or currents at the point(s) of interest to determine the net effect of the multiple sources.

As an example, let us apply the Superposition Theorem to the circuit in Figure 1.11(a) for the purpose of determining the voltage across the 2-kilohm resistor. Let us first determine the effect of the 10-volt battery. We short the 6-volt battery and evaluate the resulting circuit, Figure 1.11(b). Analysis of this series-parallel circuit will show you that the 2-kilohm resistor has approximately 1.43 volts across it with the upper end being positive.

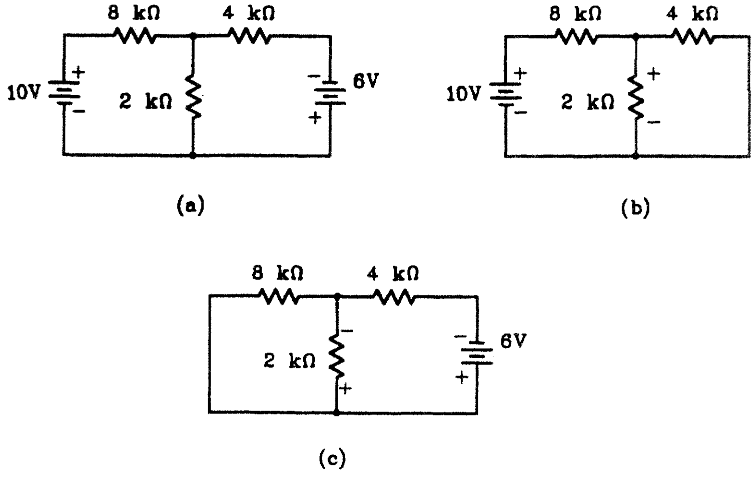
Next we evaluate the effects of the 6-volt source in Figure 1.11(c). This is another simple circuit that produces about 1.71 volts across the 2-kilohm resistor with the upper end being negative.

Since the two individual sources produced opposite polarities of voltage across the 2-kilohm resistor, we determine the net effect by subtracting the two individual values. Thus the combined effect of the 10- and 6-volt sources is $1.43\ V - 1.71\ V = -0.28$ volts.

The Superposition Theorem works with any number of sources either AC or DC and can include reactive components as long as circuit values are expressed as complex numbers.

1.3 BASIC CHARACTERISTICS OF IDEAL OP AMPS

Let us now examine some of the basic characteristics of an ideal operational amplifier. By focusing on ideal performance, we are freed from many complexities associated with nonideal performance. For many real applications, the ideal characteristics may be used to analyze and even design op amp circuits. In more demanding cases, however, we must include other operating characteristics which are viewed as deviations from the ideal.



(a)

(b)

(c)

FIGURE 1.11 Applying the Superposition Theorem to determine the effects of multiple sources.

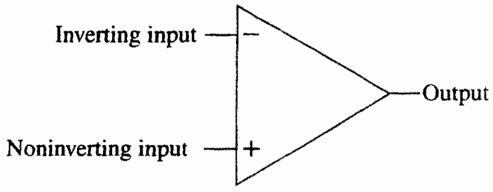


FIGURE 1.12 The basic operational amplifier symbol.

The basic schematic symbol for an ideal op amp is shown in Figure 1.12. It has the inverting and noninverting inputs labeled (−) and (+), respectively, and has a single output. Although it certainly must have power supply connections, they are not generally included on schematic diagrams.

1.3.1 Differential Voltage Gain

The differential voltage gain is the amount of amplification given to voltage appearing between the input terminals. In the case of the ideal op amp, the differential voltage gain is infinity. You will recall from your studies of transistor amplifiers that the output from an amplifier is limited by the magnitude of the DC supply voltage. If an attempt is made to obtain greater outputs, then the output is clipped or limited at the maximum or minimum levels. Since the op amp has such extreme (infinite) gain this means that with even the smallest input signal the output will be driven to its limits (typically ±15 volts for ideal op amps).

This is an important concept so be sure to appreciate what is being said. To further clarify the concept let us compare the ideal op amp with a more familiar amplifier. We will suppose that the familiar amplifier has a differential voltage gain of 5 and has output limits of ±15 volts. You will recall that the output voltage (v_o) of an amplifier can be determined by multiplying its input voltage times the voltage gain.

$$v_o = v_i A_V \tag{1.8}$$

Let us compute the output for each of the following input voltages: −4.0, −2.0, −1.0, −0.5, −0.1, 0.0, 0.1, 0.5, 1.0, 2.0, 4.0.

$$\begin{aligned}
V_o &= -4\ V \times 5 = -20\ V \text{ [output limited to −15 volts]} \\
&= -2\ V \times 5 = -10\ V \\
&= -1\ V \times 5 = -5\ V \\
&= -0.5\ V \times 5 = -2.5\ V \\
&= -0.1\ V \times 5 = 0.5\ V \\
&= 0\ V \times 5 = 0.0\ V \\
&= 0.1\ V \times 5 = 0.5\ V \\
&= 0.5\ V \times 5 = 2.5\ V
\end{aligned}$$

$$= 1\ V \times 5 = 5\ V$$

$$= 2\ V \times 5 = 10\ V$$

$$= 4\ V \times 5 = 20\ V \text{ [output limited to +15 volts]}$$

Now let us do similar calculations with the same input voltages applied to an ideal op amp. You can quickly realize that in all cases except 0.0 volts input, the output will try to go beyond the output limit and will be restricted to ±15 volts. For example, if 0.1 volts is applied

$$V_o = 0.1\ V \times \infty = \infty\ V \text{ [output limited to +15 volts]}$$

In the case of 0.0 volts at the input, we will have 0.0 volts in the output since 0.0 times anything will be zero. At this point you might well be asking, "So what good is it if every voltage we apply causes the output to be driven to its limit?" Well, review Section 1.1.4 of this text, which indicates the usefulness of the op amp in general. In Chapter 2 you will become keenly aware of how the infinite gain can be harnessed into a more usable value. For now, however, it is important for you to remember that **an ideal op amp has an infinite differential voltage gain.**

1.3.2 Common-mode Voltage Gain

Common-mode voltage gain refers to the amplification given to signals that appear on both inputs relative to the common (typically ground). You will recall from a previous discussion that a differential amplifier is designed to amplify the difference between the two voltages applied to its inputs. Thus, if both inputs had +5 volts, for instance, with respect to ground, then the difference would be zero. Similarly, the output would be zero. This defines ideal behavior and is a characteristic of an ideal op amp. In a real op amp, common-mode voltages can receive some amplification and thus depart from the desired behavior. Since we are currently defining ideal characteristics you should remember that **an ideal op amp has a common-mode voltage gain of zero.** This means the output is unaffected by voltages that are common to both inputs (i.e., no difference). Figure 1.13 further illustrates the measurement of common-mode voltage gains.

1.3.3 Bandwidth

Bandwidth, as you might expect, refers to the range of frequencies that can be amplified by the op amp. Most op amps respond to frequencies down to and including DC. The upper limit depends on several things including the specific op amp being considered. But in the case of an ideal op amp, we will consider the

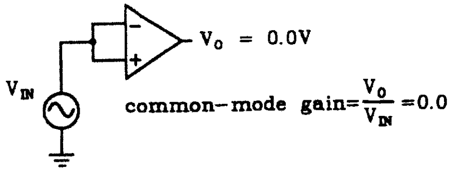


FIGURE 1.13 The common-mode voltage gain of an ideal op amp is 0.

range of acceptable frequencies to extend from DC through an infinitely high frequency. That is, **the bandwidth of an ideal op amp is infinite.** This is illustrated graphically in Figure 1.14. The graph shows that all frequencies of input voltage receive equal gains (infinite).

1.3.4 Slew Rate

The output of an ideal op amp can change as quickly as the input voltage changes in order to faithfully reproduce the input waveform. We will see in a later section that a real op amp has a practical limit to the rate of change of voltage on the output. This limit is called the *slew rate* of an op amp. Therefore, **the slew rate of an ideal op amp is infinite.**

1.3.5 Input Impedance

The input impedance of an op amp can be represented by an internal resistance between the input terminals (refer to Figure 1.15.) As the value of this internal impedance increases, the current supplied to the op amp from the input signal source decreases. That is to say, higher input impedances produce less loading by the op amp. Ideally, we would want the op amp to present minimum loading effects so we want a high input impedance. It is important to remember that **an ideal op amp has infinite input impedance.** This means that the driving circuit does not have to supply any current to the op amp. Another way to view this characteristic is to say that no current flows in or out of the input terminals of the op amp. They are effectively open circuited.

1.3.6 Output Impedance

Figure 1.16 shows an equivalent circuit that illustrates the effect of output impedance. The output circuit is composed of a voltage source and a series resistance (r_o). You can think of this as the Thevenin equivalent for the internal circuitry of the op amp. The internal voltage source has a value of $A_V v_i$. This says simply that the output has a potential similar to the input but is larger by the amount of volt-

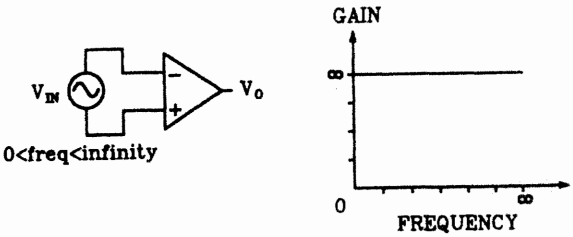


FIGURE 1.14 The bandwidth of an ideal op amp is infinite.

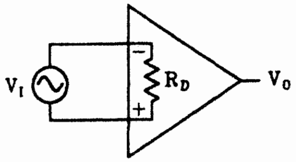


FIGURE 1.15 The input impedance of an ideal op amp is infinite.

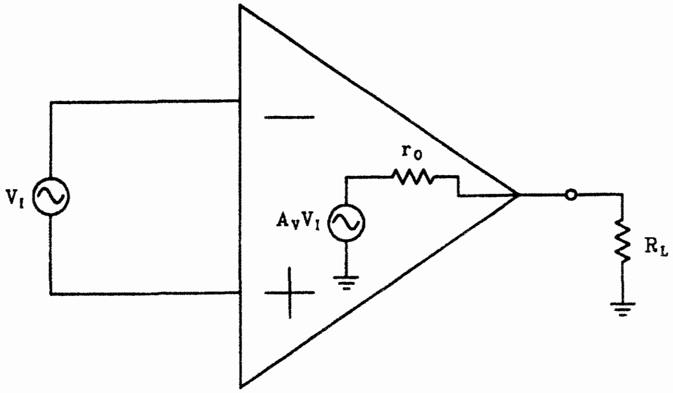


FIGURE 1.16 The output impedance of an ideal op amp is 0.

age gain. Regardless of the absolute value of the internal source, the equivalent circuit shows that this voltage is divided between the external load (R_L) and the internal series resistance r_o. In order to get the most voltage out of the op amp and to minimize the loading effects of external loads, we would want the internal output resistance to be as low as possible. Thus, **the output impedance of an ideal op amp is zero.** Under these ideal conditions, the output voltage will remain constant regardless of the load applied. In other words, the op amp can supply any required amount of current without its output voltage changing. A practical op amp will have limitations, but the output impedance will still be quite low.

NOTE: For most purposes throughout this text, we do not distinguish between input/output resistance and input/output impedance.

1.3.7 Temperature Effects

Because the op amp is constructed from semiconductor material, its behavior is subject to the same temperature effects that plague transistors, diodes, and other semiconductors. Reverse leakage currents, forward voltage drops, and the gain of internal transistors all vary with temperature. For now we will ignore these effects and conclude that **an ideal op amp is unaffected by temperature changes.** Whether we can ignore temperature effects in practice depends on the particular op amp, the application, and the operating environment.

1.3.8 Noise Generation

Anytime current flows through a semiconductor device, electrical noise is generated. There are several mechanisms that can be responsible for the creation of the noise, but in any case it is generally considered undesirable. In many applications the noise levels generated are so small as to be insignificant. In other cases, we must take precautions to minimize the effects of the noise generation. For now, however, we will consider that **an ideal op amp does not generate internal noise.** If we apply a noise-free signal on the input, then we can expect to see a noise-free, high-fidelity signal reproduced at the output.

1.3.9 Troubleshooting Tips

Even though we have barely begun to discuss op amps and how they work, we can still extend our troubleshooting skills to include op amps. Figure 1.17 shows a simple op amp circuit. Notice the addition of the power supply connections (+15V and −15V) and the pin numbers of the integrated circuit package (741). With reference to the ideal op amp circuit shown in Figure 1.17, we know the following represent normal operation:

1. There should be positive 15 volts DC on pin 7 with respect to ground.
2. There should be negative 15 volts DC on pin 4 with respect to ground.
3. As long as V_i is greater than 0, the output should be at either of two extreme voltages (approximately ±15 volts).

Items 1 and 2 are essential checks regardless of the circuit being evaluated. Item 3 results from the infinite voltage gain of the ideal op amp. If you applied an AC signal and monitored the output of Figure 1.17 (under normal conditions) with an oscilloscope, you would see a square wave. The amplitude would be near ±15 volts and the frequency would be identical to the input. Satisfy yourself that this latter statement is true, and you will be well on your way toward understanding op amp operation.

1.4 INTRODUCTION TO PRACTICAL OP AMPS

Now let us consider some of the nonideal effects of an op amp. By understanding the ideal characteristics described in the preceding sections and the nonideal characteristics presented in this section, we will be in a position to evaluate and discuss these characteristics as we analyze and design the circuits in the remainder of this text. As the circuits are presented, an ideal approach will be used whenever practical to introduce the concept. We will then identify those nonideal characteristics that should be considered for each application. A more detailed discussion of the nonideal performance of op amps is presented in Chapter 10. As each characteristic is discussed in the following paragraphs, we will compare the following items:

1. The ideal value
2. A typical nonideal value
3. The value for a real op amp

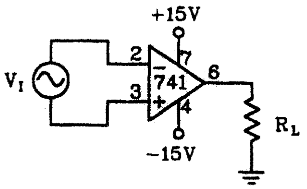


FIGURE 1.17 Schematic representation of an op amp showing the ± power supply connections.

Appendix 1 presents the manufacturer's specification sheets for a 741 op amp, one of the most widely used devices. We will refer to these specifications in the following paragraphs.

1.4.1 Differential Voltage Gain

You will recall that an ideal op amp has an infinite differential voltage gain. That is, any nonzero input signal will cause the output to be driven to its limits. In the case of a real op amp, the voltage gain is affected by several things including

1. The particular op amp being considered
2. The frequency of operation
3. The temperature
4. The value of supply voltage

For DC and very low-frequency applications the differential voltage gain will generally be from 50,000 to 1,000,000. Although this is less than the infinite value cited for ideal op amps, it is still a very high gain value. As the frequency increases, the available gain decreases. The point at which this decreasing gain becomes a problem is discussed briefly in a subsequent paragraph and more thoroughly in Chapter 10. For purposes of the present discussion, you should know that **the differential voltage gain of a typical nonideal op amp starts at several hundred thousand and decreases as frequency increases.**

Now let us determine the differential voltage gain for an actual 741 op amp (refer to Appendix 1). In the specification sheet, the manufacturer calls this parameter the *Large Signal Voltage Gain*. The value is given as ranging from a low of 20,000 to a typical value of 200,000. No maximum value is given. You will also find a number of graphs in Appendix 1. You should examine the graphs that present *open-loop* voltage gain as a function of another quantity. The terms *open* and *closed* loops are used extensively when discussing op amps. If a portion of the amplifier's output is returned to its input (i.e., feedback), then the amplifier is said to have a closed loop. You can readily see from the graphs in Appendix 1 that the gain of the op amp is not especially stable. Pay particular attention to the graph showing open-loop voltage gain as a function of frequency. Notice that the gain drops dramatically as the frequency increases.

In Chapter 2 you will learn that the gain of the op amp can be easily stabilized with a few external components. In fact, the fluctuating gain characteristic can be made insignificant in an actual op amp circuit.

1.4.2 Common-mode Voltage Gain

Although an ideal op amp has no response to voltages that are common to both inputs (i.e., no difference voltage), a practical op amp may have some response to such signals. Figure 1.18 shows how the common-mode voltage gain is measured. In the ideal case, of course, there would be no output and the computed gain would be zero. In the real case, there might be, for example, as much as 2 millivolts generated with a 1 millivolt common-mode input signal. That is, the common-mode voltage gain might be 2 in a typical case.

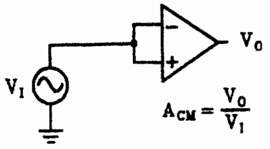


FIGURE 1.18 Measurement of the common-mode voltage gain for an op amp.

Manufacturers usually provide this data by contrasting the differential voltage gain and the common-mode voltage gain. This parameter, called *common-mode rejection ratio* (CMRR), is computed as follows:

$$CMRR = \frac{A_D}{A_{CM}} \tag{1.9}$$

where A_D and A_{CM} are the differential and common-mode gains respectively. On a specification sheet this is usually written in the decibel form. To convert from the decibel value given in the data sheet to the form shown, the following conversion formula is used:

$$CMRR = 10^{dB/20} \tag{1.10}$$

where dB is the value of the common-mode rejection ratio expressed in decibels. Now let us refer to Appendix 1 and determine the common-mode voltage gain for a 741 op amp. The minimum value is listed as 70 dB with 90 dB being cited as typical. Converting the typical value to the standard CMRR ratio form requires application of Equation (1.10).

$$\begin{aligned} CMRR &= 10^{dB/20} \\ &= 10^{90/20} \\ &= 10^{4.5} \\ &= 31{,}622 \end{aligned}$$

To determine the actual common-mode voltage gain, we simply divide the differential voltage gain by the CMRR value [transposed version of Equation (1.9)].

$$A_{CM} = \frac{A_D}{CMRR} \tag{1.11}$$

Recall that a typical differential voltage gain for the 741 is 200,000. Thus a typical common-mode voltage gain can be shown to be

$$A_{CM} = \frac{200{,}000}{31{,}622} = 6.3$$

Whether this value is good or bad, high or low, acceptable or unacceptable is determined by the particular application being considered. For now, you should strive to understand the meaning of common-mode voltage gain and how it differs from the differential voltage gain.

1.4.3 Bandwidth

You will recall from your studies of basic amplifier and/or filter theory that the bandwidth of a circuit is defined as the range of frequencies that can be passed or amplified with less than 3 dB power loss. In the case of the ideal op amp, we said that the bandwidth was infinite because it could respond equally well to frequencies extending from DC through infinitely high frequencies. As we saw in our discussion of differential voltage gain, however, not all frequencies receive equal gains in a practical op amp.

If you examine the behavior of the op amp itself with no external circuitry, it acts as a basic low-pass filter. That is, the low frequencies (all the way to DC) are passed or amplified maximally. The higher frequencies are attenuated. The bandwidth of practical op amps nearly always begins at DC. The upper edge of the passband, however, may be as low as a few hertz. This would seem to represent a serious op amp limitation. We will see, however, that this apparently restricted bandwidth can be dramatically increased by the addition of external components.

Now let us determine the bandwidth of a 741 op amp by examining the specification sheets in Appendix 1. The bandwidth often cited for 741 op amps is 1.0 megahertz (MHz). This seems like a fairly respectable value but it is misleading when viewed from the basic definition of bandwidth. In the case of op amps, the true open-loop (i.e., no external components) bandwidth is of very little value since it is so very low (a few hertz). The bandwidth generally cited in the data sheet is more appropriately labeled the *gain-bandwidth product.* Recall that the differential gain decreases as the frequency increases. The gain-bandwidth product indicates the frequency at which the differential gain drops to 1 (unity). This frequency is also called the *unity gain frequency.*

To further illustrate the bandwidth characteristics of the 741, examine the graph showing open-loop voltage gain as a function of frequency. You can see that the amplifier has a gain of about 100 dB at 1 hertz, but the gain has dropped dramatically by the time the input frequency reaches 10 hertz. In fact, the actual upper edge of the passband (the half-power or 3 dB frequency) is about 5 hertz. This is the actual bandwidth of the open-loop op amp. Observe that the gain drops steadily until it reaches unity at a frequency of 1.0 megahertz. This is the unity-gain frequency. This same value (1.0 MHz) is obtained by multiplying the DC gain (200,000) by the bandwidth (5 hertz). Thus it is also called the *gain-bandwidth product.* It is the gain-bandwidth product that is labeled "bandwidth" in some manufacturers' data sheets.

1.4.4 Slew Rate

Although the output of an ideal op amp can change levels instantly (as required by changes on the input), a practical op amp is limited to a rate of change specified by the slew rate of the op amp. The slew rate is specified in volts per second and indicates the highest rate of change possible in the output.

To further appreciate this characteristic, consider a square wave input to an op amp. In the case of an ideal op amp, the output also will be a square wave. In the case of a real op amp, however, the rise and fall times will be limited by the slew rate of the op amp. In the extreme case, a square wave input can produce a triangle output if the slew rate is so low that the output is not given adequate time to fully change states during a given alternation of the input cycle.

The 741 op amp has a slew rate of 0.5 volts per microsecond. Other op amps have significantly higher rates.

The slew rate (in conjunction with the output amplitude) limits the highest usable frequency of the op amp. The highest **sinewave** frequency that can be amplified without slew rate distortion is given by Equation (1.12).

$$f_{SRL} = \frac{\text{slew rate}}{\pi v_o(\max)} \tag{1.12}$$

where $v_o(\max)$ is the maximum peak-to-peak output voltage swing. In the case of a 741 op amp, for example, the 0.5 volts-per-microsecond slew rate limits the useable frequency range for a ±10 volt output swing to

$$\begin{aligned} f_{SRL} &= \frac{\text{slew rate}}{\pi v_o(\max)} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 20\ V} = 7.96\ kHz \end{aligned}$$

1.4.5 Input Impedance

The input impedance of an op amp is the impedance that is seen by the driving device. The lower the input impedance of the op amp, the greater is the amount of current that must be supplied by the signal source. You will recall that we considered an ideal op amp to have an infinite input impedance, and therefore, drew no current from the source.

A real op amp does require a certain amount of input current to operate but the value is generally quite low compared to the other operating currents in the circuit. You may wish to reexamine Figure 1.2 and notice that the current for the input terminals is essentially providing base current for the differential amplifier transistors. Since the transistors have a constant current source in the emitter circuit, the input impedance is very high. A typical op amp will have an input impedance in excess of 1 megohm with several megohms being reasonable. If this is still not high enough, then an op amp with a field-effect transistor input may be selected.

Appendix 1 shows the data sheet for a 741 op amp. If you look under the heading of Input Resistance you will find that these devices have a minimum input resistance rating of 0.3 megohms and a typical value of 2.0 megohms. Further, the input impedance is not constant. It varies with both input frequency and operating temperature. In many applications, we can ignore the nonideal effects of input impedance. As we study the applications in this text, we will learn when and how to consider the effects of less than ideal input impedances.

1.4.6 Output Impedance

The output impedance of an ideal op amp is 0. This means that regardless of the amount of current drawn by an external load, the output voltage of the op amp remains unaffected. That is, no loading occurs.

In the case of a practical op amp, there is some amount of output impedance. The ideal output voltage is divided between this internal resistance and any external load resistance. Generally this is an undesired effect so we prefer the op amp to have a very low output impedance.

The manufacturer's specification sheet in Appendix 1 lists the typical value of output resistance for a 741 as 75 ohms. What is not clear from the data sheet is that this value refers to open-loop output resistance. In most practical applications, the op amp is provided with feedback (i.e., closed-loop). Under these conditions, the effective output impedance can be dramatically reduced with values as low as $\frac{1}{100}$th of the open-loop output impedance being reasonable.

1.4.7 Temperature Effects

Although we want an ideal op amp to be unaffected by temperature, some effects are inevitable since the op amp is constructed from semiconductor material that has temperature-dependent characteristics. In a practical op amp, nearly every parameter is affected to some degree by temperature variations. Whether the changes in a particular characteristic are important to us depends on the application being considered and the nature of the operating environment. We will examine methods for minimizing the effects of temperature problems as we progress through the remainder of the text.

1.4.8 Noise Generation

Under ideal conditions, an amplifying or signal-processing circuit should have no signal voltages at the output that do not have corresponding signal voltages at the input. When the circuit has additional fluctuations in the output we call these changes *noise.*

There are many sources of electrical noise generation inside of the op amp. A detailed analysis of the contribution of each source to the total circuit noise is a complex subject and well beyond the goal of this text. We will, however, examine techniques that can be used to minimize problems with noise. It is fortunate that noise problems are most prevalent in circuits operating under low-signal conditions. Most other circuits do not require a detailed analysis of the circuit noise and can be adequately controlled by applying some basic guidelines and precautions for minimizing noise.

We can get an appreciation for the noise generated in a 741 by examining the data supplied by the manufacturer and shown in Appendix 1. Several graphs describe the noise performance of the 741. The op amp noise is effectively added to the desired signal at the input of the op amp. If the input signal is small or even comparable in amplitude to the total op amp noise, then the noise voltages will likely cause erroneous operation. On the other hand, if the desired signal is much larger than the noise signal, then the noise can be ignored for many applications.

1.4.9 Power Supply Requirements

When ideal op amps were discussed, we briefly indicated that all op amps require an external DC power supply. Many op amps are designed for dual supply operation with ±15 volts being the most common. Other op amps are specifically designed for single-supply operation. However, in all cases, we must provide a DC supply for the op amp in order for it to operate.

The power supply connections on the op amp are generally labeled $+V_{cc}$ or V^+ for the positive connection and $-V_{cc}$ or V^- for the negative connection. You will recall from Figure 1.2 that the DC power source provides the bias and operating voltages for the op amp's internal transistors. The magnitude of the power supply voltage is determined by the application and limited by the specific op amp being considered. A typical op amp will operate with supply voltages as low as 6 volts and as high as 18 volts, although neither of these values should be viewed as extremes. Certain devices in specific applications can operate on less than 5 volts. Other high-voltage op amps are designed to operate normally with voltages substantially higher than 18 volts.

The current capability of the power supply is another consideration. The actual op amp draws fairly low currents with 1–3 milliamperes being typical. Some low-power op amps require only a few microamperes of supply current to function properly. In most applications, the external circuitry plays a greater role in power supply current requirements than the op amp itself.

Yet another power supply consideration involves the amount of noise contributed to the circuit by the power supply. There are several forms of power-supply noise including

1. Power line ripple caused by incomplete filtering
2. High-frequency noise generated within the supply circuitry
3. Switching transients produced by switching regulators
4. Noise coupled to the DC supply line from other circuits in the system
5. Externally generated noise that is coupled onto the DC supply line
6. Noise caused by poor voltage regulation

Noise that appears on the DC power supply lines can be passed through the internal circuitry of the op amp and appear at the output. Depending on the type and in particular the frequency of the noise voltages, they will undergo varying amounts of attenuation as they pass through the op amp's components. Frequencies below 100 hertz are severely attenuated with losses as great as 10,000 being typical. As the noise frequencies increase, however, the attenuation in the op amp is less. Frequencies greater than 1.0 megahertz may be coupled from the DC supply line to the output of the op amp with no significant reduction in amplitude. The degree to which the output is affected by noise on the DC supply lines is called the *power supply rejection ratio* (PSRR).

Power distribution is a very important consideration in circuit design, yet frequently receives only minimal attention. This issue will be addressed in the following section with regard to circuit construction.

1.4.10 Troubleshooting Tips

At this point in our study of op amps, there is little difference between ideal and nonideal devices. You will recall from Section 1.3.9 that the following items are necessary for proper operation of the op amp:

1. There should be positive 15 volts DC on the V^+ connection with respect to ground.
2. There should be negative 15 volts DC on the V^- connection with respect to ground.
3. As long as the differential input voltage is greater than zero, the output should be at either of two extreme voltages (approximately ±15 volts).

Items 1 and 2 are essential checks regardless of the circuit being evaluated and whether it is viewed as ideal or nonideal. In the case of Item 3, we can now refine our expectations of normal operation. We saw from Figure 1.2 that the output of an op amp has two transistor/resistor pairs between the output and the $\pm V_{cc}$ connections. As you know, when current flows through these components a portion of the supply voltage is dropped. For most bipolar op amps, the internal voltage drop is approximately 2 volts regardless of the polarity of the output voltage. Thus, if the output of an op amp was forced to its positive extreme and was being operated from a ±15 volt supply, we would expect the output to measure approximately +13 volts. This is called the *positive saturation voltage* ($+V_{SAT}$). Similarly, the negative extreme of the output is called the *negative saturation voltage* ($-V_{SAT}$) and is about 2 volts above (i.e., less negative than) the negative power supply voltage.

1.5 CIRCUIT CONSTRUCTION REQUIREMENTS

This is one of the most important sections in the text and yet the most likely to be skipped or skimmed. Every technician and engineer believes he or she knows how to build circuits. Perhaps you do know how to build circuits, but you are urged to study the following sections anyway. It is difficult to convince people of the value of many of the techniques discussed. The reason for the lack of acceptance is that many of the techniques can be skipped or slighted without any observable deterioration in circuit performance in many cases. But it is equally true that some of the most elusive problems experienced when building and testing circuits are a direct result of poor, or at least inappropriate, circuit construction techniques. So, to repeat, you are urged to apply the following techniques on a consistent basis whether or not there appears to be an observable change in performance.

1.5.1 Prototyping Methods

There are numerous ways to construct a circuit for purposes of testing prior to committing the design to a printed circuit board. The techniques and precautions described in subsequent paragraphs are universal and are appropriate to all prototyping methods including the following:

1. Protoboard
2. Wirewrap
3. Perforated board
4. Copper-clad board

This is not intended as a complete list of prototyping methods or even the best methods. Rather, the list represents some of the most common methods used by technicians and engineers in the industry.

1.5.2 Component Placement

Circuit construction essentially consists of placing the components on some sort of supporting base, then interconnecting the appropriate points. If the circuit being constructed is a noncritical, DC, resistive circuit, then component placement may be arbitrary. As the frequency of circuit operation increases, the importance of proper component placement also increases. An op amp is inherently a high-frequency device. Even if it is being used as a DC amplifier, high-frequency noise signals will be present and can adversely affect circuit operation. Therefore component placement is important when constructing op amp circuits regardless of the application.

The components should be physically placed such that both of the following goals are accomplished:

1. Interconnecting leads can be as short as practical
2. Low-level signals and devices should not be placed adjacent to high-level devices

Although these rules may seem difficult or unnecessarily restrictive at first, they will become second nature to you if you consistently use these practices.

1.5.3 Routing of Leads

If you consistently achieve the goals cited in Section 1.5.2, then the task of properly routing the interconnecting wires is much easier. The wire routing should achieve the following goals:

1. Make all leads as short as practical
2. Avoid routing input leads or low-level signals parallel to output or high-level signals
3. Make straight, direct connections rather than forming cables or bundles of wires

1.5.4 Power Supply Distribution

Power supply distribution refers to the way that the $\pm V_{cc}$ and ground connections are routed throughout the circuit. For consistently good results with prototype operation, you should apply the following power supply distribution techniques:

1. Use a wire size that is large enough to minimize impedance.
2. Run ±V_{cc} and ground parallel and as close as possible to each other.
3. Avoid longer lead lengths than necessary.
4. Do not allow the current for digital or high-current devices to flow through the same ground wires as small linear signals (except for the main system groundpoint).
5. Twist the power distribution lines that run between the power supply and the circuit under test.

For many circuits, these rules and practices can be severely abused with no apparent reduction in circuit performance. But why take the chance? If failure to apply these techniques is the cause of poor circuit performance, it may be very difficult to isolate, and an otherwise good design may be classed as unpredictable, unreliable, impractical, and so on.

1.5.5 Power Supply Decoupling

Closely associated with power supply distribution is power supply decoupling. Again, this is an area that is hard to appreciate and frequently gets slighted. To help you understand the mechanisms involved, let us examine the problem of power distribution more closely.

In theory, each device or circuit connected between a DC source and ground receives the same voltage, and they are unaffected by each other (i.e., they are in parallel). In practice, however, the wires supplying the power contain resistance and inductance. Figure 1.19 shows a simplified representation of the problem.

As the current for circuit 1 flows through the power supply lines, the inductance and resistance cause voltage to be dropped. Thus circuit 1 receives less voltage than expected. Circuit 2 cannot receive more voltage than circuit 1 and, in fact, receives even less due to the voltage drop across the resistances and inductances between circuits 1 and 2.

You may not be alarmed at this point because you know that the resistance in copper wire is very low and so the resulting voltage drop must surely be very low. You may be right as long as **both** the current and the frequency are low.

In the case of an op amp circuit, the frequency is rarely low. Even if it is your intention to build a DC amplifier, there still will be high-frequency noise signals in the circuit. The high frequencies, whether desired or undesired, cause high-frequency fluctuations in the power supply current. These changes in current

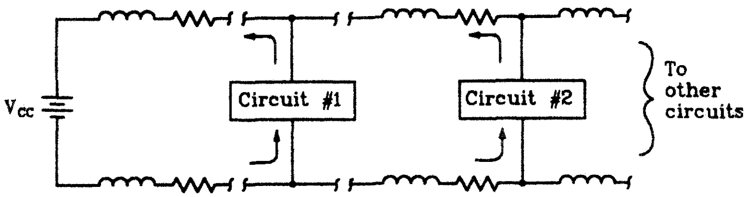


FIGURE 1.19 Printed circuit traces and wire used for DC power distribution have distributed inductance and resistance that cause voltage drops for high-frequency currents.

cause voltage drops across the distributed inductance in the power and ground lines. Since the frequencies are generally in the megahertz range, substantial inductive reactance and therefore voltage drop may result.

The high-frequency voltage drops just described cause several problems including the following:

1. The noise and/or high-frequency signal from one circuit affects the supply voltage for another circuit. The circuits are now coupled rather than being independent as theory would suggest.
2. The output of a circuit can be shifted in phase and coupled back to its input. If the circuit has sufficient gain, then we will have all the conditions necessary for sustained oscillation.
3. The overall power distribution circuit tends to behave like a loop antenna and radiates the high-frequency signals into adjacent circuits or systems.

Section 1.5.4 specifies the use of an adequate wire size. This primarily affects the DC resistance of the wire. By running the V_{CC} line and the ground return physically close together as suggested in Section 1.5.4, however, you can reduce the actual inductance of the supply lines and thus improve the high-frequency performance. Additionally, by keeping the supply lines close together, you reduce the loop area of an effective loop antenna and dramatically reduce radiations from the power supply loop.

Sections 1.5.2, 1.5.3, and 1.5.4 all recommend the use of short lead lengths. Shorter lead length directly reduces the value of distributed inductance and so reduces the magnitude of the high-frequency voltage drop problem.

You are now in a position to appreciate the value of decoupling components. The intent of decoupling is to further isolate one circuit from another with reference to the DC power distribution lines. We will examine decoupling at two important points in the system:

1. Circuit decoupling
2. Power-entry decoupling

Circuit decoupling generally consists of a capacitor connected between $\pm V_{cc}$ and ground at a point physically close to the circuit being decoupled. Figure 1.20 illustrates the effect of the decoupling capacitor. Without the coupling capacitors (refer to Figure 1.19), surges in current (i.e., high-frequency changes) had to pass

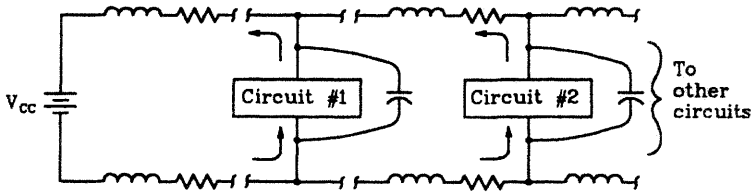


FIGURE 1.20 Decoupling capacitors placed physically close to the circuit being decoupled helps improve circuit isolation.

through the inductance and resistance of the power supply distribution lines. With the decoupling capacitors in place, short-term demands for increased current (i.e., transients or high-frequency changes) can be supplied by the decoupling capacitor. You may view it as a filter capacitor that disallows sudden changes in voltage across its terminals. You may also consider that the decoupling capacitor has a low reactance to high-frequency signals and bypasses those signals around the circuit being decoupled. In any case, the net result is that the circuits are provided with a more stable, electrically quiet source of DC power and are more effectively isolated from each other.

In most cases, ceramic disc capacitors in the range of 0.01–0.1 microfarad are good choices for circuit decoupling capacitors. Aluminum electrolytic capacitors are useless for this purpose because of their high internal inductance. It should be clear from Figure 1.20 that the decoupling capacitor must be connected physically close to the circuit or device being decoupled in order to be effective. Additionally, the leads of the decoupling capacitor should be kept as short as possible. Lengths as small as ¾ inch can nullify the effects of the decoupling capacitor in many cases.

Power-entry decoupling provides a similar function but is applied at the point where the power supply leads attach to the circuit under test. Power-entry decoupling consists of the following:

1. A tantalum electrolytic capacitor connected between each V_{cc} line and ground. The ideal value is dependent upon the circuit being tested, but generally a value of 25 to 100 microfarad is adequate.
2. A 0.1-microfarad ceramic capacitor connected in parallel with the tantalum decoupling capacitor.
3. An optional, but desirable, ferrite bead slipped over the $\pm V_{cc}$ wires leading to the power supply.
4. Twisted leads between the power supply and the power entry point.

1.5.6 Grounding Considerations

Since ground is inherently part of the power distribution system, many of the practices presented in Sections 1.5.4 and 1.5.5 apply to the ground structure as well. In addition to these practices, though, we must take some additional precautions to ensure reliable circuit performance. We shall examine the following techniques:

1. Use of a ground plane
2. Quiet grounds

The performance of a circuit can nearly always be improved by using a large planar area as the ground connection. For prototyping purposes, however, it is not always easy to get a ground plane. Perforated board is probably the most impractical method of prototyping when a ground plane is desired. Wirewrap boards, on the other hand, are available with an integral ground plane.

Copper-clad board prototyping is probably the least professional from the standpoint of appearance, but can provide electrical results that exceed those of the other methods when high-frequency operation is required. In this case, the entire surface of the copper-clad board is connected to system ground. This minimizes the resistance of the ground path and provides a shield against external interference. Additionally, when the insulated $\pm V_{cc}$ wires are routed against the ground plane, the inductance of the power distribution system is greatly reduced. Radiation into neighboring circuits is also minimized. It should be noted that multilayer printed circuit boards use one or more entire layers for the ground plane. This practice minimizes the ground impedance and dramatically reduces both emissions from the circuit and susceptibility to externally generated noise.

Protoboard provides one of the fastest methods for prototyping circuits. Additionally, the metal base plate (on some models) provides a ground plane. The ground currents, however, do not flow through this ground plane. The ground and V_{cc} distribution buses are physically close and parallel, which lowers the inductance and radiation. One potential problem that you must be aware of with this type of board is that there is a significant amount of capacitance between the various connections on the board. The problems caused by this capacitance increase as the frequency increases and/or the signal amplitudes decrease. Boards of this type are generally best suited for low-frequency circuits. It should be noted, however, that most of the circuits presented in this text were constructed and tested on such a system with excellent results.

The term *quiet ground* is most often used with reference to digital systems or, more commonly, systems that have a combination of analog and digital devices. Digital circuits can generate high levels of transient currents in the ground network. These currents can interfere with the proper operation of low-level analog circuits. The degree of interference is generally worsened for faster rise times and increased current drive in the digital gates. To minimize the ground noise problem (sometimes called *ground bounce*), the circuit should be constructed such that the analog devices are connected directly to the main ground (power input) connection. That is, the ground currents for the digital devices should not be allowed to flow through the ground wires of the analog devices. Figure 1.21 clarifies this concept. In Figure 1.21(a), the return, or ground, current for the digital circuitry flows through wires (generally printed circuit traces) that are common to the analog circuitry. This will likely cause interference or noise in the analog circuitry. By contrast, Figure 1.21(b) shows a similar circuit that utilizes a separate ground path for the digital and analog circuitry. In practice, we can often achieve this result through proper positioning of the components on the circuit board.

1.5.7 Actual Circuit Performance

This section is included as a final effort to make a believer of you. Figure 1.22 shows two sets of oscilloscope waveforms. These waveforms are real and were obtained from the plotter output on a digitizing oscilloscope; they are not theoretical drawings. Each set of waveforms illustrates the effect of one of the circuit construction rules presented in preceding sections. The first oscilloscope plot in each set illustrates circuit performance with a construction rule violated. The companion waveform shows the exact circuit with that one rule implemented properly. The results clearly indicate the change in performance. Figure 1.22(a) shows an effect of improper component placement. Figure 1.22(b) illustrates how the circuit performance can deteriorate when excessive lead lengths are used to construct the circuit.

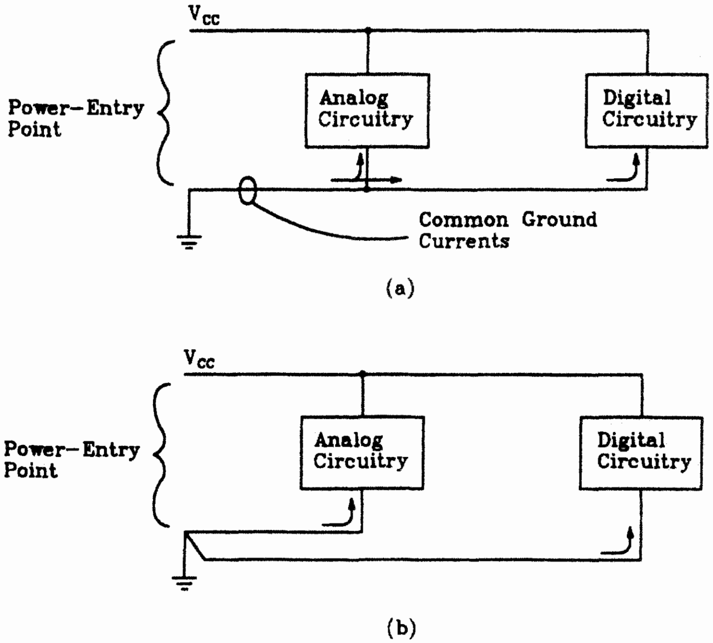


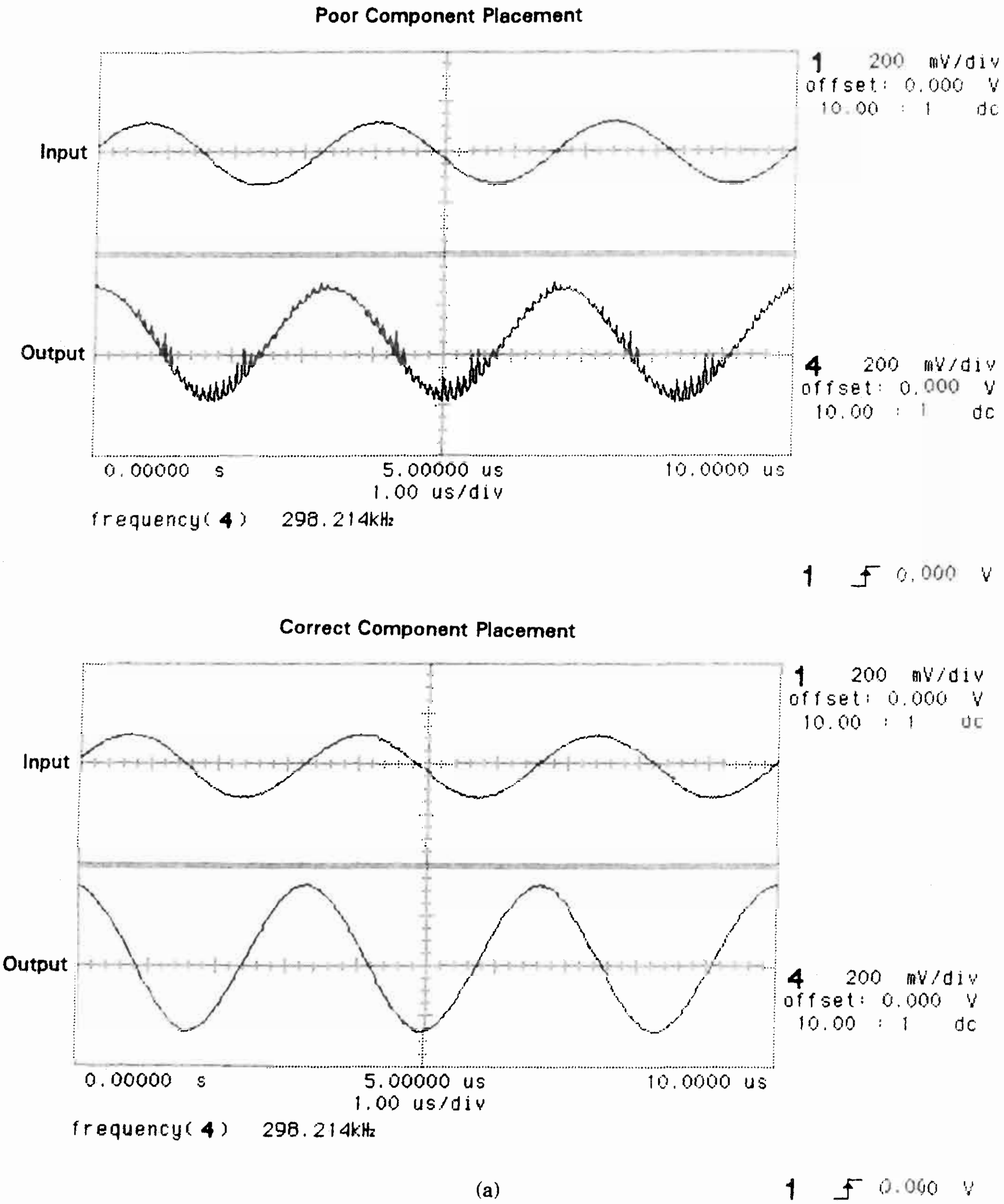
FIGURE 1.21 Wires that carry both digital and analog currents can introduce noise to the analog circuits.

1.6 ELECTROSTATIC DISCHARGE

Anyone who has been in a cold, dry climate has probably walked across a carpet or slid across a car seat and then witnessed a sizable high-voltage arc jumping between his or her body and a nearby metal object. This discharge of static electricity is called *electrostatic discharge* or simply ESD, and can pose a serious threat to op amps and other integrated electronic components. The sensitivity of an op amp (or other component) to ESD is largely a function of the technology used to build the device. In general, integrated circuits using MOSFET transistors are more susceptible to damage by ESD than circuits employing bipolar transistors. But, even bipolar circuits can be destroyed, or at least weakened, by ESD currents.

When handling integrated circuits—particularly in a cold, dry climate—you should be sure that your body is not allowed to accumulate static charge. This can be accomplished in several ways:

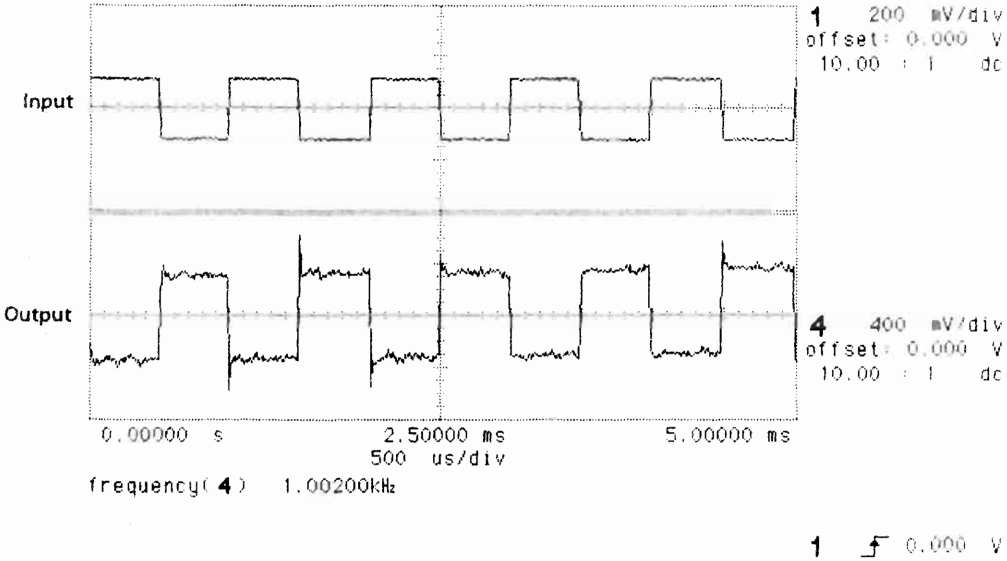
1. Attach a conductive strap to your wrist with the other end connected to a ground potential. Many manufacturers offer straps of this type that provide a discharge path for the static electricity, but do not present a safety hazard to the wearer.
2. Always touch ground (e.g., a metal chassis) before contacting the integrated circuit.
3. Condition the environment by either ionizing the air or using an effective humidifier.



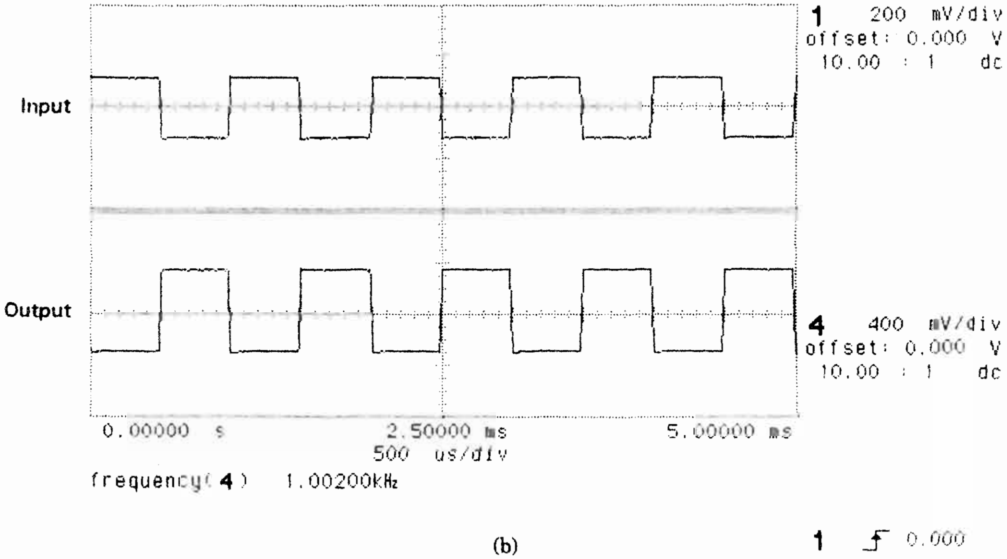
(a)

FIGURE 1.22 Performance problems can be caused by component placement (a) and excessive lead lengths (b). (Test equipment courtesy of Hewlett-Packard Company.)

Long Lead Length



Short Lead Length



(b)

FIGURE 1.22 *Continued*

SUMMARY

Operational amplifiers are integrated circuits that contain complete functional amplifier circuits whose electrical characteristics can be altered by external feedback. The input circuitry and essentially the heart of an op amp is the differential amplifier circuit. An op amp responds to the difference in potential on its two input terminals.

Ohm's and Kirchhoff's laws are essential tools for the analysis of op amp circuits. Additionally, simplification methods such as Thevenin's Theorem, Norton's Theorem, and the Superposition Theorem can simplify the analysis of otherwise complex op amp circuits.

Table 1.1 contrasts the characteristics of an ideal op amp with those of a typical op amp.

Practical op amps require a DC power source, and in many cases, a dual (±) supply. It is important that the power distribution system be properly constructed and effectively decoupled to prevent oscillation and other performance problems.

Care should be used when handling op amps—especially those with MOSFETS—because they can be damaged by ESD.

TABLE 1.1 A Comparison of Ideal and Typical Op Amp Characteristics

Characteristic	*Ideal Op Amp*	*Typical Op Amp*
Differential voltage gain	infinite	>100,000 for low frequencies, but decreases with frequency
Common-mode voltage gain	zero	2–3
Bandwidth	infinite	<10 Hz open-loop, but can be increased with feedback
Slew rate	infinite	≥0.5 V/μs
Input impedance	infinite	>1.0 megohm
Output impedance	zero	A few ohms
Affected by temperature	no	Several characteristics change with temperature
Noise generation	none	Generates some internal noise

REVIEW QUESTIONS

1. How many inputs does a differential amplifier have?
2. If a differential amplifier has a single output pin, it is called a ____-ended amplifier, and the output is referenced to ____.
3. A differential amplifier whose output is taken between two pins (neither of which is ground) is called a ____-ended amplifier.
4. What is the lowest frequency that can be amplified by a typical op amp?

5. If three 10-megohm resistors were connected in series across a 10-volt power supply and one of the resistors became open, would this open have much effect (e.g., >5%) on the currents in the remaining resistors?
6. What is the effect (significant or negligible) on *total* current if the resistors described in Question 5 are all connected in parallel with the power source?
7. If two 10-megohm resistors are connected in parallel with a 1.0-kilohm resistor, explain the relative effect on *total* current if one of the 10-megohm resistors opens. Repeat this question for the case where the 1.0-kilohm resistor develops an open.
8. If zero volts is applied directly to the inverting input of an ideal op amp at the same time that −0.1 volts is applied to the noninverting input, compute or describe the value of the output voltage.
9. If a portion of an op amp's output signal is returned to its input (i.e., feedback), we say that the amplifier is operating ____-loop.
10. What is the value of each of the following parameters for an ideal op amp?
    a. Bandwidth
    b. Input current
    c. Open-loop voltage gain
    d. Input impedance
    e. Lowest operating frequency
    f. Highest operating frequency
    g. Slew rate
    h. Output impedance
    i. Common-mode voltage gain
11. Can a real (i.e., practical) op amp be used to amplify DC?
12. If the largest output voltage swing for a particular 741 design is ±5 volts, what is the highest sinewave frequency that can be amplified before slew rate limiting begins to distort the output? (Assume a slew rate of 0.5 V/μs.)

Refer to Appendix 1 for questions 13 to 15.

13. What is the open-loop voltage gain of a standard 741 op amp at a frequency of 2 hertz (interpret the graphical data)?
14. What is the minimum input resistance of a 741 op amp?
15. What is the approximate open-loop voltage gain of a standard 741 op amp at a frequency of 100 kilohertz (interpret the graphical data)?

CHAPTER TWO

Amplifiers

2.1 AMPLIFIER FUNDAMENTALS

2.1.1 Gain

This chapter focuses on the analysis and design of several basic amplifier circuits. Not only is the amplifier circuit a fundamental building block in linear circuits, but the analytical techniques introduced in this chapter will greatly enhance your ability to analyze the circuits presented in subsequent chapters. Regardless of the specific circuit application (e.g., summing circuit, active filter, voltage regulator, and so forth), the op amp itself is simply an amplifier. Therefore, a thorough understanding of op amp behavior in circuits designed specifically as amplifiers will provide us analytical insight that is applicable to nearly all op amp circuits.

An amplifier generally accepts a small signal at its input and produces a larger, amplified version of the signal at its output. The gain (A) or amplification is expressed mathematically as

$$\boxed{gain = A = \frac{output}{input} \qquad (2.1)}$$

We may speak of voltage gain, current gain, or power gain. In each of these cases the above equation is valid. If, for example, a particular voltage amplifier produced a 5-volt RMS output when provided with a 2-volt RMS input, we would compute the voltage gain as

$$voltage\ gain = A_V = \frac{output\ voltage}{input\ voltage} = \frac{5\ V}{2\ V} = 2.5$$

There are no units for gain; it is simply a ratio of two numbers. It is also convenient to express a gain ratio in its equivalent decibel (dB) form. The conversion equations are listed below:

$$\textit{voltage gain}(dB) = A_V(dB) = 20 \log_{10} \frac{V_{OUT}}{V_{IN}} \tag{2.2}$$

$$\textit{current gain}(dB) = A_I(dB) = 20 \log_{10} \frac{I_{OUT}}{I_{IN}} \tag{2.3}$$

$$\textit{power gain}(dB) = A_P(dB) = 10 \log_{10} \frac{P_{OUT}}{P_{IN}} \tag{2.4}$$

The voltage gain of 2.5 on the amplifier discussed in the prior example could be expressed in decibels by applying Equation (2.2):

$$\begin{aligned} A_V(dB) &= 20 \log_{10} \frac{V_{OUT}}{V_{IN}} \\ &= 20 \log_{10} \frac{5V}{2V} \\ &= 20 \log_{10} 2.5 \\ &= 20 \times 0.3979 \\ &= 7.96\ dB \end{aligned}$$

Thus, we see that an amplifier with a voltage gain of 2.5 also has a voltage gain of 7.96 dB. It should be noted that, technically, the equations cited previously for calculating voltage and current gains in their decibel form require that the input and output impedances be equal. In practice, this is rarely the case. Despite this known error, it is common in the industry to calculate and express the gains as described.

You should also be reminded that fractional gains (i.e., losses) are expressed as negative decibel values.

2.1.2 Frequency Response

The frequency response of an amplifier describes how its amplification varies with changes in frequency. We often communicate the frequency response of an amplifier in graphical form. Figure 2.1 shows a typical frequency response curve.

The vertical axis indicates the amplifier's voltage gain expressed in decibels. The horizontal axis shows the input frequency range.

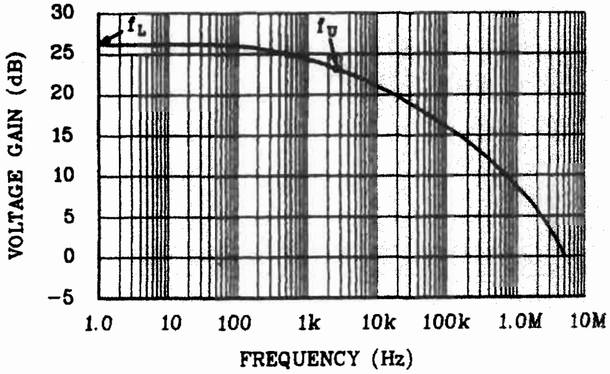


FIGURE 2.1 The bandwidth of an amplifier is the range of frequencies between the upper (f_U) and lower (f_L) cutoff frequencies.

The frequency response curve shown in Figure 2.1 indicates that the amplifier provides greater gain for low frequencies. Once the input frequency exceeds a certain value, the amplification begins to reduce significantly. Frequencies that are amplified to within 3 dB of the maximum output voltage level are considered as having passed the amplifier. Any frequency whose output voltage is lower than the maximum output voltage by more than 3 dB is considered to have been rejected by the amplifier. The frequency that separates the passband frequencies from the stopband frequencies is called the *cutoff frequency*. And since –3 dB corresponds to a power ratio of 0.5, the cutoff frequency is also called the *half-power point* on the frequency response curve.

The bandwidth of an amplifier is measured between the two half-power points. If the frequency response of an amplifier extends to include 0 (i.e., DC), then the bandwidth of the amplifier is the same as the upper cutoff frequency. This is the case for the amplifier represented in Figure 2.1. Here the lower frequency range extends all the way to 0, but in many circuits there will be a lower cutoff frequency that is greater than DC. The bandwidth is expressed as

$$bandwidth = bw = f_U - f_L \qquad (2.5)$$

where f_U and f_L are the upper and lower cutoff frequencies, respectively.

2.1.3 Feedback

So far in our discussions of op amps, we have considered only the behavior of the op amp itself with no external components. The op amp has been examined only in its open-loop configuration. In most practical applications, a portion of the amplifier's output is returned through external components to the input of the amplifier. The return signal, called *feedback*, is then mixed with the incoming signal to determine the effective signal applied to the input of the op amp.

The amplitude, frequency, and phase characteristics of the feedback signal can dramatically alter the behavior of the overall circuit. If the feedback signal has a phase relationship that is additive when mixed with the incoming signal, we refer to the return signal as *positive feedback*. On the other hand, if the feedback signal is out of phase (optimally 180 degrees) with the input signal, then the effective input signal is reduced and we label it *negative feedback*. Both forms of feedback are useful in certain op amp applications, but for the remainder of this chapter we will limit our attention to negative feedback.

The external components that provide the feedback path may be frequency selective. That is, if some frequencies pass through the feedback circuit with less attenuation than other frequencies, then we have frequency-selective feedback. This is a very useful form of feedback, but for the remainder of this chapter we will limit our discussion to nonselective feedback methods.

2.2 INVERTING AMPLIFIER

The first circuit we will examine in detail is the inverting amplifier, one of the most common op amp applications. Figure 2.2 shows the schematic diagram of the basic inverting amplifier.

2.2.1 Operation

Under normal operation, an amplified but inverted (i.e., 180° phase shifted) version of the input signal (v_I) appears at the output (v_O). If the input signal is too large or the amplifier's gain is too high, then the output signal will be clipped at the positive and negative saturation levels ($\pm V_{SAT}$).

Now let us understand how the negative feedback returned through R_F affects the amplifier operation. To begin our discussion, let us momentarily freeze the input signal as it passes through 0 volts. At this instant, the op amp has no input voltage (i.e., $v_D = 0$ volts). It is this differential input voltage that is amplified by the gain of the op amp to become the output voltage. In this case, the output voltage will be 0.

Now suppose the output voltage tried to drift in a positive direction. Can you see that this positive change would be felt through R_F and would cause the inverting pin (–) of the op amp to become slightly positive? Since essentially no current flows in or out of the op amp input, there is no significant voltage drop across R_B. Therefore the (+) input of the op amp is at ground potential. This causes v_D to be greater than 0 with the (–) terminal being the most positive. When v_D is amplified by the op amp it appears in the output as a negative voltage (inverting amplifier action). This forces the output, which had initially tried to drift in a positive direction, to return to its 0 state. A similar, but opposite, action would occur if

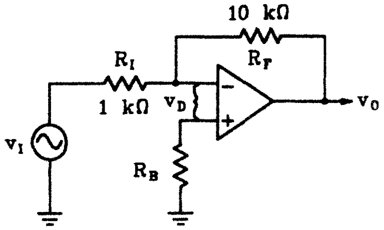


FIGURE 2.2 A basic inverting amplifier circuit.

the output tried to drift in the negative direction. Thus, as long as the input is held at 0 volts, the output is forced to stay at 0 volts.

Now suppose we allow the input signal to rise to a +2 volt instantaneous level and freeze it for purposes of the following discussion. With +2 volts applied to R_I and 0 at the output of the op amp, the voltage divider made up of R_F and R_I will have two volts across it. Since the (–) terminal of the op amp does not draw any significant current, the voltage divider is essentially unloaded. We can see, even without calculating values, that the (–) input will now be positive. Its value will be somewhat less than 2 volts because of the voltage divider action, but it will definitely be positive. The op amp will now amplify this voltage (v_D) to produce a negative-going output. As the output starts increasing in the negative direction, the voltage divider now has a positive voltage (+2 volts) on one end and a negative voltage (increasing output) on the other end. Therefore the (–) input may still be positive, but it will be decreasing as the output gets more negative. If the output goes sufficiently negative, then the (–) pin (v_D) will become negative. If, however, this pin ever becomes negative then the voltage would be amplified and appear at the output as a positive going signal. So, you see, for a given instantaneous voltage at the input, the output will quickly ramp up or down until the output voltage is large enough to cause v_D to return to its near-0 state. All of this action happens nearly instantaneously so that the output appears to be immediately affected by changes at the input.

We can also see from Figure 2.2 that changes in the output voltage receive greater attenuation than equivalent changes in the input. This is because the output is fed back through a 10-kilohm resistor, but the input is applied to the 1.0-kilohm end of the voltage divider. Thus, if the input makes a 1-volt change, the output will have to make a bigger change in order to compensate and force v_D back to its near-0 value. How much the output must change for a given input change is strictly determined by the ratio of the voltage divider resistors. Therefore, since the ratio of output change to input change is actually the gain of the amplifier, we can say that the gain of the circuit is determined by the ratio of R_F to R_I.

Recall that the internal gain (open-loop gain) of the op amp is not a constant. It varies with different devices (even with the same part number), it is affected by temperature, and it is different for different input frequencies. Now that we have added feedback to our op amp, the overall circuit gain is determined by external components (R_F and R_I). These can be quite stable and relatively unaffected by temperature, frequency, and so on.

If the input signal is too large or the ratio of R_F to R_I is too great, then the output voltage will not be able to go high enough (positive or negative) to compensate for the input voltage. When this occurs, we say the amplifier has reached saturation, and the output is clipped or limited at the $\pm V_{SAT}$ levels. Under these conditions the output is unable to rise enough to force v_D back to its near-0 level. From this you can safely conclude the following important rules regarding negative feedback amplifiers:

1. If the output is below $+V_{SAT}$ and above $-V_{SAT}$, then v_D will be very near 0 volts.
2. If v_D is anything other than near 0 volts, then the amplifier will be at one of the two saturation voltages ($\pm V_{SAT}$).

When the feedback and input resistor combination in Figure 2.2 are viewed as an unloaded voltage divider, it is easy to determine current flow. Since we know that no significant current is allowed to enter or leave the (–) pin of the op amp, we can conclude that any current flowing through R_I must also pass through R_F. The polarity of the input and output voltages will determine the direction of this current, but it is important to realize that the value of current through R_I is the same as the current through R_F.

Since very little current flows in or out of the input terminals of the op amp, we saw that there was essentially no voltage drop across R_B which caused the (+) input terminal to remain at ground potential. Since v_D is always near 0 as long as the amplifier remains unsaturated, this means that the (–) input terminal must also remain very near to ground potential. This is an important concept. Although the (–) input is not actually grounded, it remains very near ground potential. We commonly refer to this point in the circuit as *virtual ground*.

R_B is included to compensate for errors caused by the fact that some bias current does flow in or out of the op amp terminals. Even though this bias current is small, it can cause a slight voltage drop across R_F and R_I. This voltage drop is then amplified and appears at the output of the op amp as an error voltage. By including R_B in series with the (+) terminal and making its value equal to the parallel combination of R_F and R_I, we can generate a voltage that is roughly equal, but the opposite polarity from that caused by the drop across R_F and R_I. The error is generally reduced substantially but will be reduced to 0 only if the bias currents in the two input terminals happen to be equal. We will discuss this in greater detail in Chapter 10.

2.2.2 Numerical Analysis

Let us now learn to analyze the performance of the inverting amplifier circuit. We will calculate all of the following:

1. Voltage gain
2. Input impedance
3. Input current requirement
4. Slew-rate limiting frequency
5. Maximum output voltage swing
6. Maximum input voltage swing
7. Output impedance
8. Output current capability
9. Minimum value of load resistance
10. Bandwidth
11. Power supply rejection ratio

For purposes of our first numerical analysis exercise, let us evaluate the performance of the circuit in Figure 2.3.

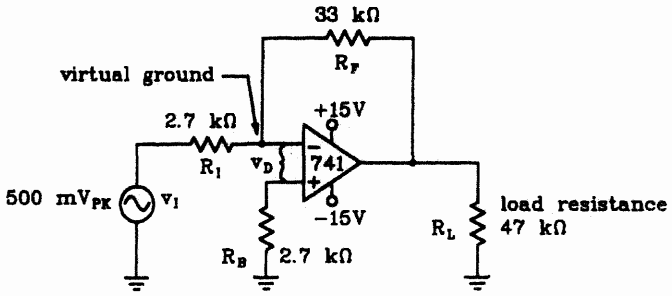


FIGURE 2.3 An inverting amplifier circuit used for a numerical analysis example.

Voltage Gain. You will recall that the voltage gain for this circuit is determined by the ratio of R_F to R_I or simply

$$\boxed{\text{voltage gain} = A_V = -\frac{R_F}{R_I} \qquad (2.6)}$$

The minus sign is used to remind us of the phase inversion since this is an inverting amplifier. Do not interpret the minus as a loss or a reduction in signal strength. For the circuit in Figure 2.3 the voltage gain will be

$$\begin{aligned} A_V &= -\frac{R_F}{R_I} \\ &= -\frac{33\ k\Omega}{2.7\ k\Omega} \\ &= -12.2 \end{aligned}$$

We can express this as a decibel gain by applying Equation (2.2):

$$\begin{aligned} A_V(dB) &= 20 \log_{10} A_V \\ &= 20 \log_{10} 12.2 \\ &= 21.7\ dB \end{aligned}$$

In this conversion, we must be particularly careful not to include the minus sign as part of the voltage gain. First, we will be unable to compute the logarithm. Second, if we tried to put the minus sign in after the calculation the resulting negative decibel answer would be misinterpreted as a loss.

It is important to note that the voltage gain computed in this section is the ideal closed-loop voltage gain of the circuit. The actual circuit gain will roll off as the input frequency is increased. This effect is discussed below as part of the discussion on bandwidth.

Input Impedance. The input impedance of the amplifier shown in Figure 2.3 is that resistance (or impedance) as seen by the source (v_I). You will recall that the voltage between the (+) and (–) terminals of the op amp (v_D) will always be about 0 unless the amplifier is saturated. Since the (+) terminal is connected to ground (via R_B) in the inverting amplifier circuit, it is reasonable to assume that the (–) pin will always be near ground potential even though it is not and cannot be connected directly to ground. But, since the (–) input is essentially at ground potential we call this point in the circuit a *virtual ground.*

Considering that the (–) pin is a virtual ground, it becomes apparent that the input impedance seen by the source is simply R_I. That is, as far as current demand is concerned, resistor R_I is effectively connected across the signal source. The equation for input impedance then is given by Equation (2.7).

$$\boxed{\textit{input impedance} = Z_I = R_I \qquad (2.7)}$$

For the case of the inverting amplifier shown in Figure 2.3, the input impedance is computed as follows:

$$\begin{aligned} Z_I &= R_I \\ &= 2.7\ k\Omega \end{aligned}$$

In general, as long as the (–) pin remains at a virtual ground potential, the input impedance will be equal to the impedance between this pin and the source. If the impedance is more complex (e.g., resistor capacitor combination), then you must use complex numbers to represent the impedance. The basic method, however, remains the same.

Input Current Requirement. Ohm's Law can be used to calculate the amount of current that must be supplied by the source. Recall that essentially no current flows into or out of the (–) terminal of the op amp. Therefore the only current supplied by the source is that drawn by R_I. Since R_I is effectively in parallel with the source due to the effect of the virtual ground, the input current can be computed as follows:

$$\boxed{\textit{input current} = i_I = \frac{V_I}{R_I} \qquad (2.8)}$$

$$\begin{aligned} i_I &= \frac{v_I}{R_I} \\ &= \frac{500\ mV\ peak}{2.7\ k\Omega} = 185.2\ \mu A\ peak \end{aligned}$$

Since this is a sinusoidal waveform, we could easily convert this to an RMS value if desired as shown:

$$i_I(RMS) = i_i(peak) \times 0.7071 \tag{2.9}$$

In our present case, the RMS value is found as follows:

$$\begin{aligned} i_I(RMS) &= i_I(peak) \times 0.7071 \\ &= 185\ \mu A \times 0.7071 \\ &= 130.9\ \mu A \end{aligned}$$

As long as the input source can supply at least this much current without reducing its output, the op amp circuit will not load the source.

Maximum Output Voltage Swing. The output voltage of an op amp is limited by the positive and negative saturation voltages. These can both be approximated as 2 volts less than the DC supply voltage. Since the DC supply in Figure 2.3 is ±15 volts, the saturation voltages will be +13 volts and −13 volts for the positive and negative limits, respectively. Thus, the maximum output voltage swing is computed as follows:

$$v_O(\mathrm{max}) = (+V_{SAT}) - (-V_{SAT}) \tag{2.10}$$

For the circuit in Figure 2.3, the maximum output voltage swing is found as shown:

$$\begin{aligned} v_O(\mathrm{max}) &= (+V_{SAT}) - (-V_{SAT}) \\ &= (+13\ V) - (-13\ V) \\ &= 26\ V \end{aligned}$$

Since both DC supplies are equal, the output can swing equally above and below 0. This is the normal condition.

If you desire to be more accurate in the estimation of output saturation voltage, you may refer to the manufacture's data sheet in Appendix 1. The manufacturer lists minimum and typical output voltage swings for different values of load resistance.

Slew-Rate Limiting Frequency. It should also be noted that the above maximum output is only obtainable for frequencies below the point where slew rate limiting occurs. This frequency can be estimated with the following equation:

$$f_{SRL} = \frac{slew\ rate}{\pi v_O(\mathrm{max})} \tag{2.11}$$

In the case of the circuit being considered, the highest frequency that can produce a full output swing without distortion caused by slew rate limiting is computed as

$$\begin{aligned} f_{SRL} &= \frac{slew\ rate}{\pi v_O(\max)} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 26\ V} \\ &= 6.12\ kHz \end{aligned}$$

If we attempt to amplify frequencies higher than 6.12 kilohertz (and full amplitude) with the circuit shown in Figure 2.3, then the output will be nonsinusoidal. Once the input frequency goes higher than a certain frequency (about 9 kilohertz in this case), then the output amplitude begins to drop in addition to the distorted shape.

Maximum Input Voltage Swing. We have computed the voltage gain of the circuit, and we know the maximum output voltage swing. We, therefore, have enough information to compute the largest input signal that can be applied without driving the amplifier into saturation.

$$v_I(\max) = \frac{v_O(\max)}{A_V} \tag{2.12}$$

Calculations for the present case are shown below:

$$\begin{aligned} v_I(\max) &= \frac{v_O(\max)}{A_V} \\ &= \frac{26\ V}{12.2} \\ &= 2.13\ V\ peak\text{-}to\text{-}peak \end{aligned}$$

Since we are working with sinusoidal waveforms, we might choose to express this value as peak or RMS as shown below:

$$v_I(peak) = \frac{v_I(\max)}{2} \tag{2.13}$$

For our present circuit, we have

$$\begin{aligned} v_I(peak) &= \frac{v_I(\max)}{2} \\ &= \frac{2.13\ V}{2} \\ &= 1.07\ V\ peak \end{aligned}$$

Also,

$$v_I(RMS) = v_I(peak) \times 0.707 \tag{2.14}$$

In the present case,

$$\begin{aligned} v_I(RMS) &= v_I(peak) \times 0.707 \\ &= 1.07\ V \times 0.707 \\ &= 756.5\ mV\ RMS \end{aligned}$$

So, for the amplifier circuit presented in Figure 2.3, input signals as great as 756.5 millivolts RMS can be amplified without saturation clipping. If you attempt to amplify larger signals, then the peaks on the output waveform will be flattened at the output saturation voltage limits.

Output Impedance. You will recall from Chapter 1 that the output impedance of an op amp is generally quite low. The data sheet in Appendix 1 lists 75 ohms as a typical output resistance for a 741 op amp. This value, however, is the open-loop output resistance. When negative feedback is added to the amplifier (as in Figure 2.3) the effective output impedance decreases sharply. The value of effective output impedance can be approximated as shown:

$$r_O = \frac{(R_I + R_F) \times output\ impedance(open\ loop)}{A_{OL} R_I} \tag{2.15}$$

where A_{OL} is the open loop gain of the op amp at the specified frequency. This can be read from the manufacturer's graphical data (see Appendix 1) showing open-loop gain as a function of frequency. Alternatively, you may estimate it as

$$A_{OL} = \frac{unity\ gain\ frequency}{f_{IN}} \tag{2.16}$$

where f_{IN} is the specific input frequency being considered.

For the circuit in Figure 2.3, the closed-loop output impedance can be estimated at 1000 hertz as follows. First we compute the open-loop gain at 1000 hertz by applying Equation (2.16):

$$\begin{aligned} A_{OL} &= \frac{unity\ gain\ frequency}{f_{IN}} \\ &= \frac{1.0\ MHz}{1.0\ kHz} \\ &= 1000 \end{aligned}$$

Next compute the effective output impedance with Equation (2.15):

$$\begin{aligned} r_O &= \frac{(R_I + R_F) \times \mathit{output\ impedance(open\ loop)}}{A_{OL} R_I} \\ &= \frac{(2.7\ k\Omega + 33\ k\Omega) \times 75\ \Omega}{1000 \times 2.7\ k\Omega} \\ &= 0.99\ \Omega \end{aligned}$$

This low value approaches our ideal value of 0 ohms. Now, as an illustration, recompute the value of output impedance at a higher frequency of 5 kilohertz.

First compute A_{OL} with Equation (2.16).

$$\begin{aligned} A_{OL} &= \frac{\mathit{unity\ gain\ frequency}}{f_{IN}} \\ &= \frac{1\ MHz}{5\ kHz} \\ &= 200 \end{aligned}$$

Next compute the effective output impedance with Equation (2.15).

$$\begin{aligned} r_O &= \frac{(R_I + R_F) \times \mathit{output\ impedance(open\ loop)}}{A_{OL} R_I} \\ &= \frac{(2.7\ k\Omega + 33\ k\Omega) \times 75\ \Omega}{200 \times 2.7\ k\Omega} \\ &= 4.96\ \Omega \end{aligned}$$

This value is significantly higher than our first estimate and clearly shows the increase in output resistance as the input frequency is increased.

How does a particular value of output impedance affect the performance of the amplifier circuit? To understand the effects, we can examine the equivalent circuit shown in Figure 2.4. Here we see a voltage source labeled v_O driving a series circuit.

The v_O source is that voltage that would be present at the output of the op amp if the output impedance were truly 0 ohms. You can see that this ideal voltage (v_O) is divided between the output impedance (r_O), which is internal to the op amp, and R_L, which is the op amp load. The voltage reaching the load can be computed with the voltage divider equation.

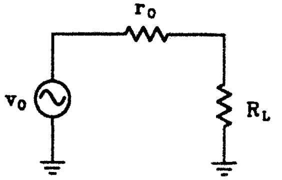


FIGURE 2.4 The equivalent output circuit of an op amp can be used to judge the effects of output impedance (r_O).

$$\text{load voltage} = v_{load} = \frac{v_O R_L}{R_L + r_O} \tag{2.17}$$

Let us compute the actual load voltage in Figure 2.3 at a frequency of 5 kilohertz. First we compute the ideal output voltage Equation (2.1):

$$\begin{aligned} v_O &= v_I A_V \\ &= 500\ mV \times 12.2 \\ &= 6.1\ V\ peak \end{aligned}$$

We have found the value of r_O at 5 kilohertz to be 4.96 ohms. Using the method shown in Figure 2.4, we can now determine the actual load voltage with Equation (2.17).

$$\begin{aligned} v_{load} &= \frac{v_O R_L}{R_L + r_O} \\ &= \frac{6.1\ V_{pk} \times 47\ k\Omega}{47\ k\Omega + 4.96\ \Omega} \\ &= 6.099\ V\ peak \end{aligned}$$

At a frequency of 5 kilohertz when the output resistance has increased to nearly 5 ohms, the effect of nonideal output resistance is minimal. Problems could be anticipated when the output resistance exceeds 1 percent of the value of load resistance.

Although the preceding calculation illustrates the effects of output resistance, it is valid only if we are below the frequency that causes slew rate limiting (f_{SRL}). If f_{SRL} is exceeded, we can expect the actual output to be much lower than the value computed with Equation (2.17), and the output will be nonsinusoidal in shape. Additionally, this method is inappropriate if the output drive capability of the op amp is exceeded.

Output Current Capability. The output of the op amp in Figure 2.3 must supply two currents: the current through the feedback resistor (i_F) and the current to the load resistor (i_L). It is the sum of these currents that flows into or out of the output of the op amp.

The output of many (but not all) op amps is short circuit protected. That is, the output may be shorted directly to ground or to either DC supply voltage without damaging the op amp. For a protected op amp (such as the 741), the output current capability is not determined by the maximum allowable current before damage, but rather depends on the amount of reduced output voltage the application can tolerate.

With no output current being supplied to the load, the output voltage stays at the expected v_O level, and the total output current is equal to i_F. As the load current is increased (load resistance decreased), the actual output voltage begins to drop as shown in the previous section. Finally, if the load resistance is reduced all the way to 0 ohms, the output current will be limited to a safe value. This value can be found in the data sheet (Appendix 1), and is 20 milliamps for the 741 device.

As the load resistance varies from infinity (open) to zero (short), the output current from the op amp varies from i_F to 20 milliamps. The limiting factor is the amount of reduction that can be tolerated on the output voltage.

The amount of current (i_F) flowing through the feedback resistor is easily computed with Ohm's Law as

$$\textit{feedback current} = i_F = \frac{v_L}{R_F} \tag{2.18}$$

On an unprotected op amp, the value of load current plus the value of feedback current must be kept below the stated output current rating. If this value is not supplied in the data sheet, then it can be estimated by using the maximum power dissipation data; recall that *power* = *voltage* × *current*.

Minimum Value of Load Resistance. The minimum value of load resistance is determined by the maximum value of output current (determined in the previous section). The actual computation is essentially Ohm's Law:

$$\textit{minimum load resistance} = R_L(\text{min}) = \frac{v_L}{i_L} \tag{2.19}$$

where i_L is the maximum allowable output current of the op amp minus the current (i_f) flowing through the feedback circuit, and v_L is the minimum acceptable output voltage.

Note that in many, if not most, applications, the value of output current needed for the load is substantially below the limiting value, so no significant loading occurs.

Let us assume that the application shown in Figure 2.3 requires us to have at least 1.19 volts across the load when 100 millivolts is applied to the input terminal. Let us further assume that the frequency of interest is 5 kilohertz. From previous calculations we know that the voltage gain (A_V) is 12.2 (ignoring the effects of bandwidth described in the next section) and that the output resistance at 5 kilohertz is 4.96 ohms.

Figure 2.5 shows the equivalent circuit at this point. The value of i_O can be computed with Ohm's Law.

$$i_O = \frac{v_O - v_L}{r_O} \tag{2.20}$$

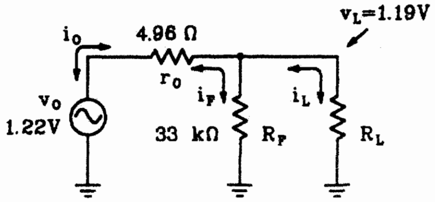


FIGURE 2.5 An equivalent circuit used to compute the minimum allowable load resistor.

More specifically,

$$\begin{aligned} i_O &= \frac{v_O - v_L}{r_O} \\ &= \frac{1.22\ V - 1.19\ V}{4.96\ \Omega} \\ &= 6.05\ \textit{milliamps} \end{aligned}$$

The value of i_F can also be computed using Ohm's Law, Equation (2.18).

$$\begin{aligned} i_F &= \frac{v_L}{R_F} \\ &= \frac{1.19\ V}{33\ k\Omega} \\ &= 36.1\ \mu A \end{aligned}$$

Kirchhoff's Current Law can now be used to determine the value of load current (i_L).

$$\boxed{i_L = i_O - i_F \qquad (2.21)}$$

Calculations for the present example are shown below:

$$\begin{aligned} i_L &= i_O - i_F \\ &= 6.05\ mA - 36.1\ \mu A \\ &= 6.01\ mA \end{aligned}$$

Using Ohm's Law, Equation (2.19), we can now compute the value of R_L.

$$\begin{aligned} R_L &= \frac{v_L}{i_L} \\ &= \frac{1.19\ V}{6.01\ mA} = 198\ \Omega \end{aligned}$$

With this small value of load resistance, we would not be able to provide full-range voltage swings on the output because of excessive loading.

In the foregoing calculations (as with most calculations presented in this book), it is not important to remember all of the equations. Rather, strive to understand the concept and realize that most of what we are discussing is centered on basic electronics principles that you learned when you studied introductory AC and DC circuits.

Bandwidth. Although the bandwidth of an ideal op amp is considered to be infinite, the bandwidth of real op amps and the associate amplifier circuit are definitely restricted. In the case of the circuit shown in Figure 2.3, the lower cutoff frequency is essentially 0. That is, since the op amp responds all the way down to DC, and since there are no reactive components to reject the lower frequencies, the amplifier circuit will operate with frequencies as low as DC.

The upper cutoff frequency is quite a different story. Figure 2.6 shows the open-loop frequency response (upper curve) for a 741 op amp. This is the same curve presented in the manufacturer's data sheet as open-loop voltage gain as a function of frequency. Also drawn on the graph in Figure 2.6 is a line showing a voltage gain of 12.2. This is the ideal closed-loop gain that we calculated for the circuit in Figure 2.3.

Notice that the difference between the open- and closed-loop gain curves is maximum at low frequencies. As the frequency increases, the difference between the two curves becomes less. Near the right side of the graph, the two curves actually intersect. What really happens to the overall circuit gain as the frequency increases?

The derivation of the formula for amplifier voltage gain ($A_V = -R_F/R_I$) was based on the assumption that the op amp had an infinite (or at least a very high) voltage gain. This allowed us to make the assumption that the differential input voltage (v_D) was 0. As you can see from the graph in Figure 2.6, our assumptions are reasonable for low frequencies. That is, the open-loop voltage gain is very high. But as the frequency increases and the open-loop gain rolls off, our assumptions begin to lose their validity. The most obvious proof of this exists beyond the point of intersection of the open- and closed-loop curves. In the region to the right of the intersection point, the open-loop gain is actually lower than our calculated

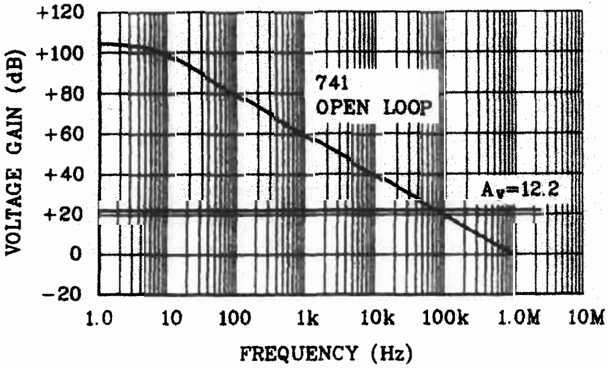


FIGURE 2.6 Frequency response of the standard 741 op amp.

closed-loop gain, thus making it impossible for our circuit to deliver the desired amplification.

It is common to compute bandwidth in a circuit like that shown in Figure 2.3 by applying the following equation:

$$bw = \frac{f_{UG} R_I}{R_I + R_F} \tag{2.22}$$

where f_{UG} is the unity gain frequency of the op amp. Substituting values and computing gives us the following:

$$\begin{aligned} bw &= \frac{1.0\ MHz \times 2.7\ k\Omega}{2.7\ k\Omega + 33\ k\Omega} \\ &= 75.6\ kHz \end{aligned}$$

The actual frequency response for the circuit shown in Figure 2.3 is plotted in Figure 2.7. This represents the circuit's real behavior. Two additional lines are superimposed on the plot for reference: the open-loop frequency response curve of the 741 op amp and the ideal gain curve of the circuit in Figure 2.3.

Power Supply Rejection Ratio. If the DC supply lines (V^+ and V^-) have noise, particularly high-frequency noise, these noise signals may affect the output signal. The degree to which the op amp is affected by the power supply noise is called the *power supply rejection ratio* (PSRR). The manufacturer's data sheet normally expresses this parameter in microvolts per volt. To determine the magnitude of the noise signal on the output for a given amplitude of noise signal on the supply lines, we can use the following calculation:

$$v_{NO} = PSRR v_N \left(\frac{R_F}{R_i} + 1 \right) \tag{2.23}$$

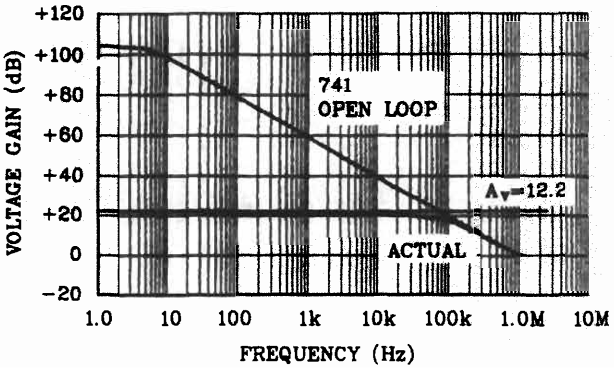


FIGURE 2.7 Actual frequency response of the circuit shown in Figure 2.3.

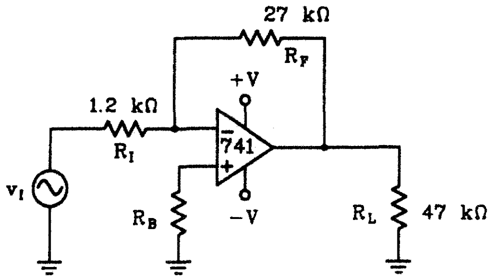


FIGURE 2.8 An inverting amplifier circuit used to demonstrate the effects of the power supply rejection ratio.

where v_{NO}, v_N, R_F, R_I, and *PSRR* are the values of the output noise signal, the noise signal on the DC supply lines, the feedback resistor, the input resistor, and the power supply rejection ratio, respectively. For example, refer to Figure 2.8.

The manufacturer's data sheet in Appendix 1 for a 741 op amp lists the power supply rejection ratio as ranging from 30 to 150 microvolts per volt. Thus, the worst-case effect on the output voltage for the circuit in Figure 2.8 is computed with Equation (2.23) as

$$\begin{aligned} v_{NO} &= PSRR v_N\left(\frac{R_F}{R_i}+1\right) \\ &= 150\ \mu V/V \times v_N\left(\frac{27\ k\Omega}{1.2\ k\Omega}+1\right) \\ &= v_N \times 0.003525 \end{aligned}$$

In other words, the amplitude of the power line noise (v_N) will be reduced by a factor of 0.003525. This means, for example, that if the DC supply lines have noise signals of 100 millivolts peak-to-peak, then we can anticipate a similar signal in the output with an amplitude of about

$$\begin{aligned} v_{NO} &= v_N \times 0.003525 \\ &= 100\ mV \times 0.003525 \\ &= 352.5\ \mu V\ \textit{peak-to-peak} \end{aligned}$$

2.2.3 Practical Design Techniques

The following design procedures will enable you to design inverting op amp circuits for many applications. Although certain nonideal considerations are included in the design method, additional nonideal characteristics are described in Chapter 10.

To begin the design process, you must determine the following requirements based on the intended application:

1. Voltage gain
2. Maximum input current

3. Frequency range
4. Load resistance
5. Maximum input voltage

As an example of the design process, let us design an inverting amplifier with the following characteristics:

1. Voltage gain	12
2. Maximum input current	250 microamperes RMS
3. Frequency range	20 hertz to 2.5 kilohertz
4. Load resistance	100 kilohms
5. Maximum input voltage	500 millivolts RMS, 0-volt reference

Determine an Initial Value for R_I. The minimum value for R_I is determined by the maximum input voltage and the maximum input current and is computed with Ohm's Law as follows:

$$R_I = \frac{v_I}{i_I} \tag{2.24}$$

In this case, the calculations are

$$\begin{aligned} R_I &= \frac{v_I}{i_I} \\ &= \frac{500\ mV}{250\ \mu A} \\ &= 2\ k\Omega \end{aligned}$$

As a general rule, you should avoid designing amplifiers with input resistances of less than 1000 ohms unless you have a specific need for them. In our present case, the computed minimum (2.0 kilohms) is greater than 1000 ohms, so we will use the computed value. It should also be noted that the minimum input impedance is often determined by the needs of the application.

Determine the Value of R_F. R_F can be computed from the voltage gain equation, Equation (2.6):

$$\begin{aligned} A_V &= -\frac{R_F}{R_I}, \textit{ or} \\ R_F &= A_V R_I \end{aligned}$$

Note that the inversion sign is omitted from the equation when computing a resistance value. For the present example, we compute R_F as follows:

$$R_F = A_V R_I$$
$$= 12 \times 2\ k\Omega = 24\ k\Omega$$

Determine the Required Unity Gain Frequency. The minimum unity gain frequency for the op amp can be estimated by applying Equation (2.22). For the present case, we have

$$f_{UG} = \frac{bw(R_F + R_I)}{R_I}$$
$$f_{UG} = \frac{(2.5\ kHz)(24\ k\Omega + 2\ k\Omega)}{2\ k\Omega} = 32.5\ kHz$$

Since this is well below the 1.0-megahertz unity gain frequency of the 741, we should be able to use the 741 in this application (with regard to bandwidth).

Determine the Minimum Supply Voltages. The minimum supply voltages are computed by simply ensuring that the maximum expected output voltage swing is no greater than the $\pm V_{SAT}$ values. The maximum output swing can be found by using the basic equation, Equation (2.1), for voltage gain:

$$A_V = \frac{v_{OUT}}{v_{IN}},\ or$$
$$v_{OUT} = v_{IN} A_V$$

In our particular example, the maximum output voltage will be

$$v_{OUT} = v_{IN} A_V$$
$$= 500\ mV(RMS) \times 12 \times 1.414$$
$$= 8.48\ V\ peak,\ or$$
$$= 2 \times 8.48\ V(peak) = 16.96\ v_{P\text{-}P}$$

Notice the multiplying factor 1.414 to convert our input voltage (given in RMS) to a peak or worst-case value. The manufacturer's data sheet in Appendix 1 indicates that the 741 op amp will produce at least a ±12-volt output swing with a ±15-volt supply voltage as long as the load resistor is at least 10 kilohms. Thus, we can infer that we have a worst-case internal voltage drop of 15 – 12, or 3 volts. This means that the minimum power supply voltage for our circuit must be higher than the maximum output voltage by the amount of the internal voltage drop (V_{INT}). That is,

$$\boxed{\pm V_{MIN} = V_{OUT}(\text{max}) + V_{INT} \qquad (2.25)}$$

For our particular case, the minimum power supply voltages will be

$$\pm V_{MIN} = V_{OUT}(\max) + V_{INT}$$
$$= 8.48\ V + 3\ V = 11.48\ V$$

Anything greater than ±11.48 volts for the DC supply will be adequate; therefore, let us choose the standard values of ±15 volts for our application.

Determine the Required Slew Rate. The required slew rate of the op amp is affected by the highest operating frequency and the maximum output voltage swing. In our present case, the highest input frequency has been specified as 2.5 kilohertz. The maximum peak-to-peak output voltage swing ($v_O(\max)$) was previously computed as 16.96 volts. The minimum required slew rate for the op amp is determined by rearranging Equation (2.11) to yield

$$\mathit{slew\ rate}(\min) = \pi f(\max) v_O(\max)$$
$$= 3.14 \times 2.5\ kHz \times 16.96\ V_{P\text{-}P}$$
$$= 0.133\ v/\mu s$$

Since the slew rate of the 741 exceeds this minimum value, we can continue with our initial op amp selection. If the above calculation indicates a higher requirement than our preliminary op amp selection can deliver, then another op amp must be selected that has a higher slew rate.

Calculate the Value of Compensation Resistor (R_B). The compensation resistor (R_B) reduces the error in the output voltage caused by the voltage drops that result from the op amp's input bias currents. To achieve maximum error reduction, we try to place equal resistances between both op amp input terminals and ground. If we were to apply Thevenin's Theorem to the inverting input circuit, we would see that resistors R_F and R_I are effectively in parallel. This means that the optimum value for R_B is simply the combined value of R_F and R_I in parallel.

$$R_B = \frac{R_F R_I}{R_F + R_I} \tag{2.26}$$

For the present example, we compute R_B as follows:

$$R_B = \frac{R_F R_I}{R_F + R_I}$$
$$= \frac{24\ k\Omega \times 2\ k\Omega}{24\ k\Omega + 2\ k\Omega}$$
$$= 1.8\ k\Omega$$

The final schematic is shown in Figure 2.9.

The actual behavior of the circuit is indicated in Figure 2.10 by an oscilloscope display. The measured performance is compared to the design goals in Table 2.1.

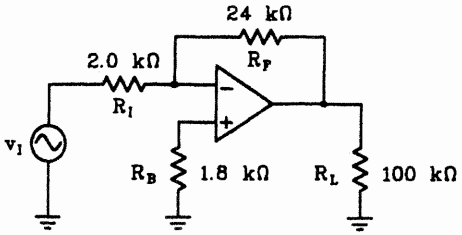
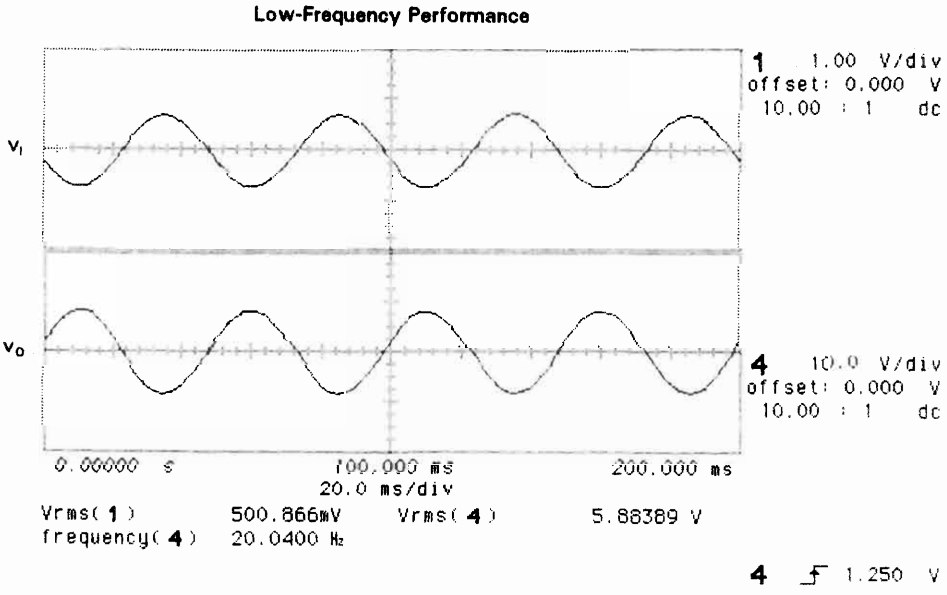


FIGURE 2.9 An inverting amplifier design.

TABLE 2.1

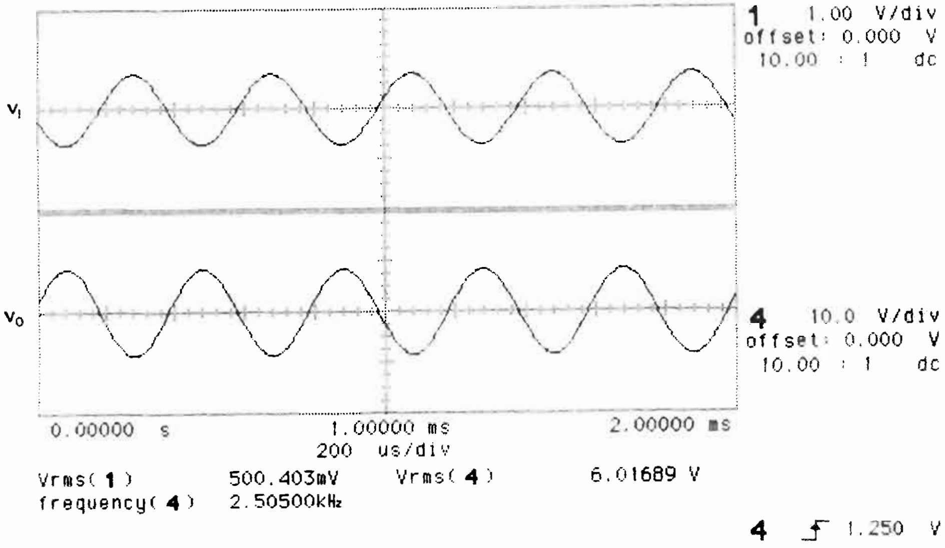
Parameter	*Design Goal*	*Measured Value*
Voltage gain	12	11.7–12
Frequency range	20 Hz–2.5 kHz	<20 Hz–>2.5 kHz


Low-Frequency Performance

(a)

FIGURE 2.10 Oscilloscope displays showing the performance of the inverting amplifier shown in Figure 2.9. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*

High-Frequency Performance


v_I
v_O
1 1.00 V/div
offset: 0.000 V
10.00 : 1 dc
4 10.0 V/div
offset: 0.000 V
10.00 : 1 dc
0.00000 s
1.00000 ms
200 us/div
2.00000 ms
Vrms(1) 500.403mV
Vrms(4) 6.01689 V
frequency(4) 2.50500kHz
4 1.250 V

(b)

FIGURE 2.10 *Continued*

2.3 NONINVERTING AMPLIFIER

2.3.1 Operation

Figure 2.11 shows the schematic diagram of a basic noninverting amplifier. As you might expect, the input signal is applied to the (+), or noninverting, input. Resistor R_B is a compensation resistor similar to that described for the inverting amplifier. Because it has such a tiny current through it, we will ignore its effects for the immediate discussion.

Resistor R_F and resistor R_I form a voltage divider between the output terminal and ground. That portion of the output that appears across R_I will provide the input to the (–) input terminal. The input signal (v_I) supplies the voltage to the (+) input terminal. The difference between these two voltages (v_D) is amplified by the open-loop gain of the op amp. Recall that as long as the output of the op amp is in the linear range (i.e., not saturated), the magnitude of v_D will be very near 0 volts. Since the (+) input terminal is equal to v_I, and since v_D is approximately 0, we can conclude that the voltage on the (–) input terminal must also be nearly equal to v_I. Recall that the source for the (–) input voltage is the output of the op amp. Now we see that the output will go as high as necessary in order to develop enough voltage drop across R_I to equal v_I.

Suppose, for example, that the input voltage (v_I) made a sudden increase from 0 volts to some positive level. At this first instant, the (+) input of the op amp would be positive and the (–) input would still be at its previous 0-volt level. The

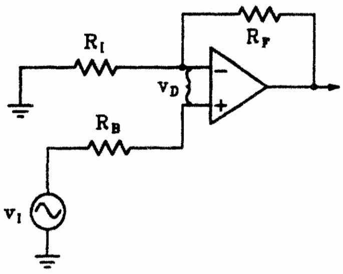


FIGURE 2.11 The basic noninverting amplifier circuit.

voltage v_D would now be amplified. Since the (+) input is more positive, the output rises as quickly as possible in the positive direction. As the output goes positive, a portion is fed back through the R_F and R_I voltage divider to the (–) input. Since the (–) input is becoming more positive, the value of v_D is decreasing. That is, the two input terminal voltages are getting closer together. Finally, the output of the amplifier will stop going in the positive direction whenever the (–) input has come to within a few microvolts of the (+) input.

Now consider how high the output voltage had to go in order to bring the (–) input up to the same voltage as the (+) input. You can see that it is strictly the values of the voltage divider R_F and R_I that determine the amount of output voltage change required. Thus, for a given input voltage change, the output will make a corresponding change. The magnitude of the change is the gain of the amplifier and is largely determined by the ratio of R_F to R_I. This action is explained with mathematics in the following section.

Additionally note that as the input went positive, the output went positive. That is, the amplifier configuration is noninverting.

2.3.2 Numerical Analysis

Much of our analysis for the inverting amplifier is applicable to the noninverting amplifier circuit. We will determine a method to enable us to compute the following circuit characteristics:

1. Voltage gain
2. Input impedance
3. Input current requirement
4. Maximum output voltage swing
5. Slew-rate limiting frequency
6. Maximum input voltage swing
7. Output impedance
8. Output current capability
9. Bandwidth
10. Power supply rejection ratio

For purposes of this discussion, let us analyze the noninverting amplifier circuit shown in Figure 2.12.

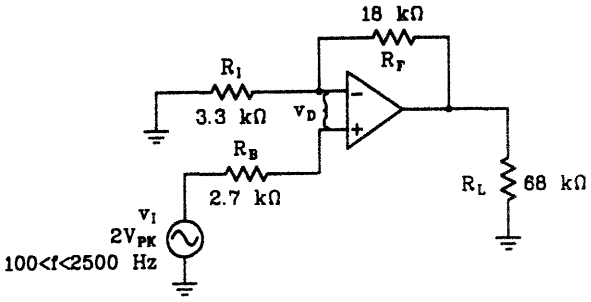


FIGURE 2.12 A noninverting amplifier circuit used for a numerical analysis example.

Voltage Gain. We know by inspection of the circuit in Figure 2.12 that the voltage on the (+) input is approximately equal to v_I. That is, there is no significant voltage drop across R_B because the only current allowed to flow through R_B is the op amp bias current (ideally 0). We also know from previous discussions that the voltage between the (+) and (–) input terminals (v_D) is very near 0 volts. Thus, we may rightly conclude that the voltage on the (–) pin is approximately equal to the value of v_I.

Ohm's Law can be used to compute the current through R_I as follows:

$$\boxed{i_{R_I} = \frac{v_I}{R_I}} \tag{2.27}$$

For the circuit in Figure 2.12, we have

$$\begin{aligned} i_{R_I} &= \frac{v_I}{R_I} \\ &= \frac{2\ V\ (peak)}{3.3\ k\Omega} = 606.1\ \mu A\ peak \end{aligned}$$

Since negligible current flows into or out of the input of the op amp, we will assume that all of the current flowing through R_I continues through R_F, according to Kirchhoff's Current Law. The voltage drop across R_F can be computed by applying Ohm's Law.

$$\begin{aligned} v_{R_F} &= i_{R_F} \times R_F \\ &= 606.1\ \mu A \times 18\ k\Omega \\ &= 10.91\ V\ peak \end{aligned}$$

The output voltage can be determined through application of Kirchhoff's Voltage Law. That is, we know the voltage on the (–) input is 2.0 volts peak. The output voltage will be greater than this by the amount of voltage drop across R_F. It is computed as

$$\begin{aligned} v_O &= v_I + v_{R_F} \\ &= 2\ V + 10.91\ V \\ &= 12.91\ V\ peak \end{aligned}$$

The voltage gain can be computed by the basic gain equation, Equation (2.1), as shown:

$$\begin{aligned} A_V &= \frac{v_O}{v_I} \\ &= \frac{12.91\ V\ peak}{2\ V\ peak} \\ &= 6.45 \end{aligned}$$

Recall from an earlier discussion that the voltage gain of the circuit is largely determined by the ratio of R_F to R_I. More specifically, the low-frequency or ideal voltage gain of the circuit can also be calculated with the following equation:

$$A_V = \frac{R_F}{R_I} + 1 \tag{2.28}$$

In our case, the calculations are

$$\begin{aligned} A_V &= \frac{R_F}{R_I} + 1 \\ &= \frac{18\ k\Omega}{3.3\ k\Omega} + 1 \\ &= 6.45 \end{aligned}$$

This latter method is the most common, but the former provides additional insight into circuit operation and the application of basic electronics principles.

The voltage can be expressed in decibels if desired, as we did with inverting amplifiers. In our present example, the equivalent voltage gain expressed in decibels is:

$$\begin{aligned} A_V(dB) &= 20 \log_{10} A_V \\ &= 20 \log_{10} 6.45 \\ &= 16.2\ dB \end{aligned}$$

Note that the voltage gain computed in this section is the ideal closed-loop voltage gain of the circuit. The actual circuit gain will roll off as the input frequency is increased, just as it did with inverting amplifiers. This effect is discussed below as part of the discussion on bandwidth.

Input Impedance. The input impedance of the noninverting amplifier circuit (refer to Figure 2.12) is essentially equal to the input impedance of the (+) input terminal of the op amp modified by the feedback effects. That is, the only current leaving the source must flow into or out of the op amp as bias current for the (+) input. The manufacturer's data sheet for a 741 is shown in Appendix 1. It indicates that the input resistance is at least 0.3 megohms and is typically about 2.0 megohms. Recall that this is the effective resistance between the two op amp inputs. By considering the output impedance to be near 0, we can sketch the equivalent circuit shown in Figure 2.13(a).

Let us make the following substitution for the value of v_O:

$$v_O = v_I\left(\frac{R_F}{R_I} + 1\right)$$

This, of course, comes from Equation (2.1) and Equation (2.28). If we now apply Thevenin's Theorem to the portion of the circuit to the right of the dotted line, we obtain the equivalent circuit shown in Figure 2.13(b). Notice that the resistance in our equivalent circuit has the same voltage (2 V_{PK}) on both ends, which produces a net voltage of 0. If there is no voltage, there will be no current, so the effective input impedance is infinite. This represents the ideal condition.

In a real op amp circuit, the differential input voltage (v_D) is greater than 0 and increases as the frequency increases. With reference to Figure 2.13(b), as the input frequency increases, the two voltage sources become more and more unequal. This causes a difference in potential across the resistance in the circuit, which in turn produces a current flow. The increasing current corresponds to a decreasing input impedance. Although the actual input impedance is quite high and can normally be assumed to be infinite, it can be approximated by the following equation:

$$\boxed{\textit{input impedance} = Z_I = R_{OP}A_V\left(\frac{R_I}{R_F + R_I}\right) \qquad (2.29)}$$

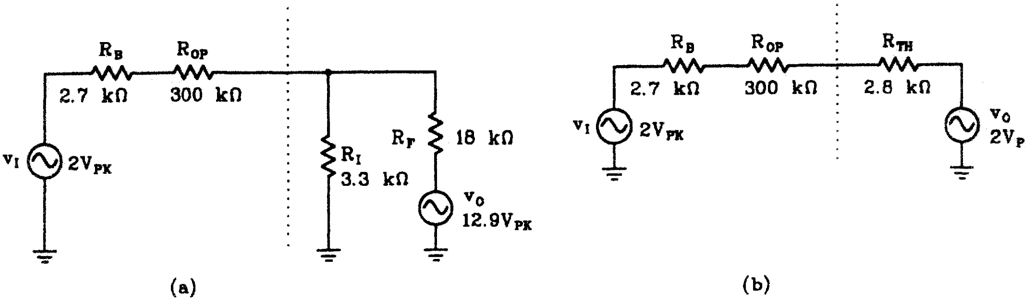


FIGURE 2.13 An equivalent circuit used to estimate the input impedance of the noninverting amplifier shown in Figure 2.12.

where R_{OP} is the value of input resistance provided by the manufacturer and A_V is the open-loop voltage gain of the op amp. For the circuit shown in Figure 2.12, we can estimate input resistance at low frequencies as

$$\begin{aligned} Z_I &= R_{OP}A_V\left(\frac{R_I}{R_F + R_I}\right) \\ &= 300\ k\Omega \times 200{,}000\left(\frac{3.3\ k\Omega}{18\ k\Omega + 3.3\ k\Omega}\right) \\ &= 9296\ M\Omega \end{aligned}$$

If we had used the more typical value of 2.0 megohms for the op amp resistance (R_{OP}), we would have gotten a much higher value for input resistance. In either case, the actual effective input resistance is extremely high. This high input resistance is one of the primary advantages of the noninverting amplifier in many applications.

Input Current Requirement. The input current can be estimated by applying Ohm's Law to the input circuit as follows:

$$\begin{aligned} i_{IN} &= \frac{v_I}{Z_I} \\ &= \frac{2\ V\ peak}{9296\ M\Omega} \\ &= 215\ picoamperes\ peak \end{aligned}$$

Even this is a worst-case value. If we had used the higher typical value for input resistance, we would have computed an even smaller value. For many, if not most, applications, this input current can be considered negligible. If it becomes necessary to consider this current, then additional considerations must be made because the exact value of input resistance varies considerably with temperature and frequency.

Maximum Output Voltage Swing. As we found with the inverting amplifier, the output voltage of an op amp is limited by the $\pm V_{SAT}$ levels. For most applications utilizing a bipolar op amp, the saturation voltages can be estimated at about 2 volts less than the DC supply voltage. In the case of Figure 2.12, we compute the maximum output swing, Equation (2.10), as

$$\begin{aligned} v_O(\text{max}) &= +V_{SAT} - (-V_{SAT}) \\ &= +13\ V - (-13\ V) \\ &= 26\ V \end{aligned}$$

If a more accurate value is desired, the manufacturer's data sheet can be used to find a more precise value for the worst-case saturation voltage.

Slew-Rate Limiting Frequency. The highest frequency that can be amplified without distorting the waveform, because of the slew rate limitation of the op amp, is given by Equation 2.11.

$$\begin{aligned} f_{SRL} &= \frac{slew\ rate}{\pi v_O(\max)} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 26\ V} \\ &= 6.12\ kHz \end{aligned}$$

If it is known for certain that the actual output swing will never be required to reach its limits, then the lower actual output swing can be used in place of $v_O(\max)$ in the above calculation.

Maximum Input Voltage Swing. The maximum input voltage swing is simply the highest input voltage that can be applied without driving the output past the saturation point. It is computed in the same manner as that for the inverting amplifier.

$$\begin{aligned} v_I(\max) &= \frac{v_O(\max)}{A_V} \\ &= \frac{26\ V}{6.45} \\ &= 4.03\ V\ peak\text{-}to\text{-}peak \end{aligned}$$

Since we are working with sinusoidal waveforms, we might choose to express this value as peak, as in Equation (2.13), or RMS, as in Equation (2.14), as shown:

$$\begin{aligned} v_I(peak) &= \frac{v_O(\max)}{2} \\ &= \frac{4.03\ V}{2} = 2.015\ V\ peak \end{aligned}$$

and

$$\begin{aligned} v_I(RMS) &= v_I(peak) \times 0.707 \\ &= 2.015\ V \times 0.707 = 1.425\ V\ RMS \end{aligned}$$

If you attempt to amplify signals larger than 1.425 volts RMS, then the peaks on the output waveform will be flattened at the output saturation voltage limits.

Output Impedance. You will recall from the analysis of the inverting amplifier that the effective output impedance decreases sharply from the open-loop value stated in the manufacturer's data sheets. The value of effective output impedance can be approximated by applying Equation (2.15).

$$r_O = \frac{(R_I + R_F) \times output\ impedance(open\ loop)}{A_{OL} R_I}$$

where A_{OL} is the open-loop gain of the op amp at a particular frequency. For the circuit in Figure 2.12, the open-loop gain at 2500 hertz is computed with Equation (2.16) as

$$\begin{aligned} A_{OL} &= \frac{1.0\ MHz}{2500\ Hz} \\ &= 400 \end{aligned}$$

The output impedance at 2500 hertz can then be estimated as

$$\begin{aligned} r_O &= \frac{(R_I + R_F) \times output\ impedance(open\ loop)}{A_{OL} R_I} \\ &= \frac{(3.3\ k\Omega + 18\ k\Omega) \times 75\ \Omega}{400 \times 3.3\ k\Omega} \\ &= 1.2\ \Omega \end{aligned}$$

In most cases, the output impedance is so low relative to the value of load resistance that the output voltage is essentially unaffected, but you can always be sure by performing the voltage divider calculation outlined in Section 2.2.2.

Output Current Capability. If the output of the op amp is short-circuit protected (as in the 741), then the output current capability is limited by the maximum allowable drop in output voltage for the given application. This can be estimated with Ohm's Law as discussed in the preceding section. Recall from our discussion of inverting amplifiers that the output must supply both load resistor current and the current through the feedback resistor. The feedback current is computed using Ohm's Law. For this particular circuit, the calculations are

$$\begin{aligned} i_F &= \frac{v_O - v_I}{R_F} \\ &= \frac{12.9\ V - 2\ V}{18\ k\Omega} \\ &= 605.6\ \mu A\ peak \end{aligned}$$

With no output current being supplied to the load, the output voltage stays at the expected v_O level and the total output current is equal to i_F. As the load current is increased (load resistance is decreased), the actual output voltage begins to drop because of the voltage divider action described in the previous section. Finally, if the load resistance is reduced all the way to 0 ohms, the output current will be limited to the short circuit value. This value can be found in the data sheet (Appendix 1) and is 20 milliamperes for the 741 device.

As the load resistance varies from infinity (open) to 0 (short), the output current from the op amp varies from i_F to 20 milliamperes. The limiting factor is the amount of reduction that can be tolerated on the output voltage.

On an unprotected op amp, the value of load current plus the value of feedback current must be kept below the stated output current rating. If this value is not supplied in the data sheet, it can be estimated by using the maximum power dissipation data; recall that *power* = *voltage* × *current*.

Bandwidth. The discussion of bandwidth presented for the inverting amplifier circuit is also applicable to the noninverting configuration. That is, as long as the circuit has no reactive components, the frequency response will extend all the way down to DC on the low-frequency end. We can estimate the high-frequency end of the frequency response by applying Equation (2.22):

$$\begin{aligned} bw &= \frac{f_{UG} R_I}{R_F + R_I} \\ &= \frac{1.0\ MHz \times 3.3\ k\Omega}{18\ k\Omega + 3.3\ k\Omega} \\ &= 155\ kHz \end{aligned}$$

Recall that the open-loop gain of the op amp falls off rapidly as the input frequency is increased above a few hertz. As the open-loop gain value approaches the computed closed-loop gain value, the actual circuit gain also begins to drop. Thus, we begin to experience increased errors in our gain calculations as the frequency is increased.

For these equations to be valid, it is important that the op amp output voltage swing be small enough to avoid the effects of slew rate limiting. The highest amplitude that can be amplified at a given frequency without the effects of slew rate limiting is given as

$$\boxed{v_O(\max) = \frac{slew\ rate}{\pi f} \qquad (2.30)}$$

The slew rate is determined by the particular amplifier, f is the frequency of interest, and $v_O(\max)$ is the highest peak-to-peak amplitude in the output before slew rate limiting begins to distort the signal. In the present case, if we try to operate at the upper cutoff frequency (155 kHz), we have to keep the output voltage below the value computed:

$$v_O(\max) = \frac{slew\ rate}{\pi f}$$

$$= \frac{0.5\ V/\mu s}{3.14 \times 155\ kHz}$$

$$= 1.03\ V\ peak\text{-}to\text{-}peak$$

Power Supply Rejection Ratio. The power supply rejection ratio provides us with an indication of the degree of immunity the circuit has to noise voltages on the DC power lines. The change in output voltage (v_O) for a given change in DC power line noise voltage (v_N) is computed with Equation (2.23):

$$v_{NO} = v_N PSRR\left(\frac{R_F}{R_I} + 1\right)$$

where v_O, v_N, R_F, R_I, and $PSRR$ are the values of the output noise signal, the noise signal on the DC supply lines, the feedback resistor, the input resistor, and the power supply rejection ratio (PSRR), respectively. The manufacturer's data sheet in Appendix 1 lists the PSRR as ranging from 30 to 150 microvolts per volt. The worst-case effect on the output voltage for the circuit in Figure 2.12 is then

$$\begin{aligned} v_{NO} &= v_N PSRR\left(\frac{R_F}{R_I} + 1\right) \\ &= v_N \times 150\ \mu V/V\left(\frac{18\ k\Omega}{3.3\ k\Omega} + 1\right) \\ &= v_N \times 0.000968 \end{aligned}$$

In other words, the amplitude of the power line noise (v_N) will be reduced by a factor of 0.000968. This means, for example, that if the DC supply lines had noise signals of 100 millivolts peak-to-peak, we could anticipate a similar signal in the output with an amplitude of about

$$\begin{aligned} v_{NO} &= v_N \times 0.000968 \\ &= 100\ mV \times 0.000968 \\ &= 96.8\ \mu V \end{aligned}$$

2.3.3 Practical Design Techniques

The following design procedures will enable you to design noninverting op amp circuits for many applications. Although certain nonideal considerations are included in the design method, additional nonideal characteristics are described in Chapter 10.

To begin the design process, you must determine the following requirements based on the intended application:

1. Voltage gain
2. Frequency range

3. Load resistance
4. Maximum input voltage

As an example of the design procedure, let us design a noninverting amplifier with the following characteristics:

1. Voltage gain	8
2. Frequency range	DC to 5 kilohertz
3. Load resistance	27 kilohms
4. Maximum input voltage	800 millivolts RMS

Determine an Initial Value for R_I. There are endless combinations of R_F and R_I that will produce the desired circuit voltage gain. The smaller the values of R_F and R_I, the higher the value of feedback current. The feedback current subtracts from the maximum available output current. Thus, we want to avoid extremely small values.

The larger we make R_F and R_I, the more the circuit operation is affected by certain nonideal characteristics. In general, neither resistor should be less than 1.0 kilohms nor more than 680 kilohms unless there is a compelling reason for them to be so. With this rule of thumb in mind, we select R_I as 4.7 kilohms.

Determine the Value of R_F. R_F can be computed from the voltage gain equation, Equation (2.28):

$$A_V = \frac{R_F}{R_I} + 1, \ or$$

$$R_F = R_I(A_V - 1)$$

For the present design example, we compute R_F as follows:

$$\begin{aligned} R_F &= R_I(A_V - 1) \\ &= 4.7\ k\Omega(8 - 1) = 32.9\ k\Omega \end{aligned}$$

We select the nearest standard value of 33 kilohms to use as R_F.

Determine the Required Unity Gain Frequency. You will recall from our discussions on bandwidth that the error between the calculated or ideal gain and the actual gain increases as frequency increases. We can, however, estimate the required unity gain frequency by applying Equation (2.22).

$$\begin{aligned} f_{UG} &= \frac{bw(R_F + R_I)}{R_I} \\ &= \frac{5\ kHz(33\ k\Omega + 4.7\ k\Omega)}{4.7\ k\Omega} \\ &= 40.1\ kHz \end{aligned}$$

Thus, we must select an op amp that has minimum unity gain frequency of at least 40.1 kilohertz. Since the 741 has a 1.0-megahertz unity gain frequency, it should be adequate for this application with respect to bandwidth.

Determine the Minimum Supply Voltages. The minimum supply voltages are computed simply by ensuring that the maximum expected output voltage swing is no greater than the $\pm V_{SAT}$ values. The maximum output swing can be found by using the basic equation for voltage gain, Equation (2.1).

$$A_V = \frac{v_{OUT}}{v_{IN}}, \text{ or}$$

$$v_{OUT} = v_{IN} A_V$$

In our particular example, the maximum output voltage will be

$$\begin{aligned} v_{OUT} &= v_{IN} A_V \\ &= 800\ mV \times 1.414 \times 8 \\ &= 9.05\ V\ peak,\ or \\ v_{OUT} &= v_O(\max) \\ &= 9.05\ V \times 2 \\ &= 18.1\ V\ peak\text{-}to\text{-}peak \end{aligned}$$

Notice the multiplying factor 1.414 to convert our input voltage (given in RMS) to a peak or worst-case value. The manufacturer's data sheet in Appendix 1 indicates that the 741 op amp will produce at least a ±12-volt output swing with a ±15-volt supply voltage and a load resistance of at least 10 kilohms. Thus, we can infer that we have a worst-case internal voltage drop of 15 – 12, or 3 volts. The minimum power supply voltage can be determined with Equation (2.25):

$$\begin{aligned} \pm V_{MIN} &= V_{OUT} + V_{INT} \\ &= 9.05\ V + 3\ V \\ &= 12.05\ V \end{aligned}$$

Anything greater than ±12.05 volts for the DC supply will be adequate, so we choose the standard values of ±15 volts for our application. Realize that this is a worst-case calculation; a more typical internal drop would be 2 volts rather than 3 volts.

Determine the Required Slew Rate. The minimum slew rate for the op amp is computed by transposing Equation (2.11).

$$\begin{aligned} slew\ rate(\min) &= \pi f_{SRL}\, v_O(\max) \\ &= 3.14 \times 5\ kHz \times 18.1\ V \\ &= 0.284\ V/\mu s \end{aligned}$$

Since the slew rate of the 741 exceeds this minimum value, we can continue with our initial op amp selection. If the above calculation indicates a higher requirement than our preliminary op amp selection can deliver, then another op amp must be selected that has a higher slew rate.

Calculate the Value of Compensation Resistor (R_B). The compensation resistor (R_B) reduces the error in the output voltage caused by the voltage drops that result from the op amp's input bias currents. As with the inverting configuration, we achieve maximum error reduction by inserting equal resistances between both op amp input terminals and ground. The resistance between the inverting input to ground is essentially equal to the parallel combination of R_I and R_F. This is easier to appreciate if you remember that the output impedance of an op amp is very low. For purposes of this analysis, assume that the output impedance is actually 0 ohms. In this condition, one end of both R_I and R_F connect to ground and the other ends connect to the inverting input terminal. Thus, they are effectively in parallel. The value of R_B is calculated as in Equation (2.26):

$$\begin{aligned} R_B &= \frac{R_F R_I}{R_F + R_I} \\ &= \frac{33\ k\Omega \times 4.7\ k\Omega}{33\ k\Omega + 4.7\ k\Omega} \\ &= 4.1\ k\Omega \end{aligned}$$

We will choose a standard value of 4.3 kilohms. The final schematic is shown in Figure 2.14.

The actual performance of the circuit is indicated by the oscilloscope plots in Figure 2.15. Additionally, Table 2.2 contrasts the measured performance with the original design goals.

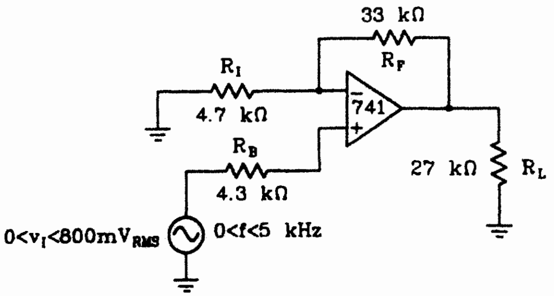
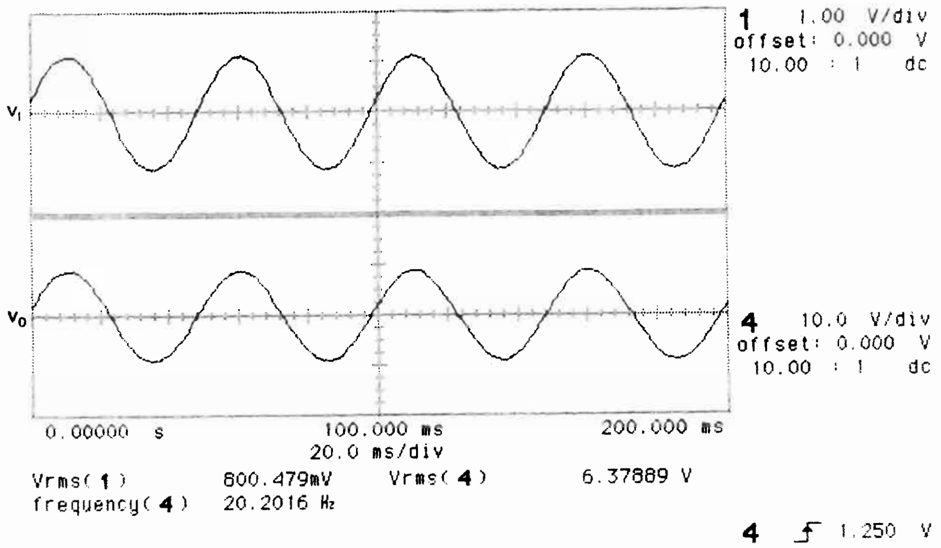


FIGURE 2.14 An example noninverting amplifier design.

TABLE 2.2

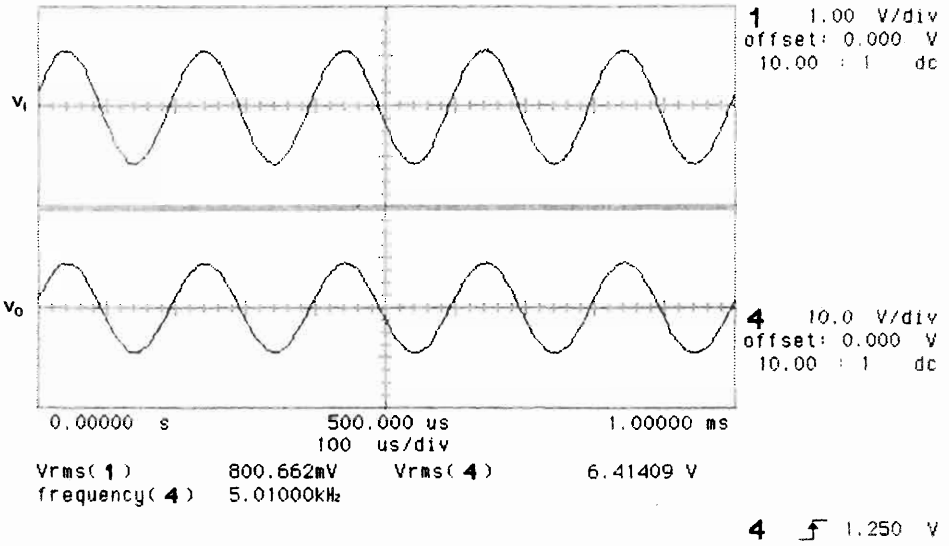
Parameter	*Design Goal*	*Measured Values*
Voltage gain	8	7.9–8.01
Frequency range	DC–5 kHz	DC–>5 kHz

Low-Frequency Performance



(a)

High-Frequency Performance



(b)

FIGURE 2.15 Oscilloscope displays showing the actual performance of the noninverting amplifier shown in Figure 2.14. (Test equipment courtesy of Hewlett-Packard Company.)

A slight phase shift can be seen between input and output waveforms in Figure 2.15. The effect is more pronounced as the input frequency is increased. For many applications, input/output phase relations are not important; in other applications they are critical. Chapter 10 discusses this issue in more detail.

2.4 VOLTAGE FOLLOWER

2.4.1 Operation

A voltage follower circuit using an op amp is shown in Figure 2.16. This is a very simple, but very useful, op amp configuration.

If you compare the voltage follower circuit to the noninverting amplifier previously discussed, you will see that R_I and R_F in the noninverting circuit have become respectively, infinity and 0 to form the follower circuit. Since there is no significant impedance in the path of the (–) input terminal, there is no need for the compensating resistor in the (+) terminal.

The voltage on the (+) input is equal to v_I because of the direct connection. Recall that v_D is approximately 0 volts as long as the amplifier is not saturated. This means that the (–) input terminal will also be approximately equal to v_I. And, since the (–) pin is connected directly to the output, the output must also be equal to v_I. Because the output is essentially equal to the input at all times, the voltage gain is unity (i.e., 1). The circuit is called a voltage follower because the output appears to follow or track the input voltage.

So, what is the value of a circuit that gives us an output voltage that is equal to the input? Well, although the voltage gain is only 1, there are other very important reasons for using a voltage follower. One of the most important uses for the circuit is for impedance transformation. By inspection, you can see that the input impedance is very high, as the only current drawn from the source is the bias current for the (+) terminal. The output impedance, on the other hand, is quite low. As with the other configurations previously studied, the output impedance approaches an ideal value of 0, so the voltage follower circuit can interface a high impedance device or circuit to a lower impedance device or circuit. Although very little current is drawn from the source, a substantial current may be supplied to the load.

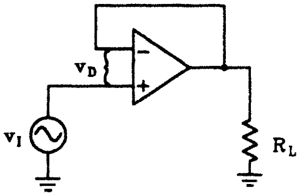


FIGURE 2.16 A basic voltage follower circuit.

2.4.2 Numerical Analysis

The numerical analysis for the voltage follower is simpler than for previous circuits because of the lack of circuit complexity. Let us analyze the circuit shown in Figure 2.16 and determine the following values:

1. Voltage gain
2. Input impedance
3. Input current requirement
4. Maximum output voltage swing
5. Slew-rate limiting frequency
6. Maximum input voltage swing
7. Output impedance
8. Output current capability
9. Bandwidth
10. Power supply rejection ratio

For purposes of the following analyses, let us assume that the op amp in Figure 2.16 is a 741.

Voltage Gain. The ideal voltage gain of a voltage follower circuit is always unity, or 1. This can be further demonstrated by applying the voltage gain equation, Equation (2.28), presented for the noninverting amplifier circuit. Since R_F is now 0 and R_I is infinity, our calculations become

$$\begin{aligned} A_V &= \frac{R_F}{R_I} + 1 \\ &= \frac{0}{\infty} + 1 \\ &= 1 \end{aligned}$$

As with other amplifier configurations, the actual gain of the circuit falls off at high frequencies. This is further discussed, along with bandwidth, in a later section.

Input Impedance. The input impedance of the voltage follower is ideally infinite because it is essentially the input resistance of the (+) input of the op amp modified by the effects of feedback. The value may be estimated by applying Equation (2.29) with the quantity $R_I/(R_F + R_I)$ considered to be unity. Thus, for low frequencies (i.e., near DC) the circuit in Figure 2.16 will have a minimum input impedance of

$$\begin{aligned} Z_I &= R_{OP}A_V \\ &= 0.3\ M\Omega \times 200{,}000 \\ &= 60{,}000\ M\Omega \end{aligned}$$

If we had used typical values for R_{OP}, we would have gotten an even higher value for Z_{IN}. In any case, the value is so high that we can consider it as infinite for most applications.

Input Current Requirement. The input current for the circuit in Figure 2.16 is only the bias current for the (+) input terminal. This is ideally 0 and for most applications may be neglected. If more precision is desired, then the manufacturer's data sheet in Appendix 1 can be referenced. The data sheet indicates that the input bias current will be no higher than 500 nanoamperes, with a more typical value listed as 80 nanoamperes. Even though this current is temperature dependent, the absolute values are so small that they may be neglected in many applications.

Maximum Output Voltage Swing. The maximum output voltage swing for the follower circuit is determined in the same manner, Equation (2.10), as that used with preceding amplifiers. That is,

$$\begin{aligned} v_O(\text{max}) &= +V_{SAT} - (-V_{SAT}) \\ &= +13\ V - (-13\ V) \\ &= 26\ V \end{aligned}$$

If a more accurate value is desired, the manufacturer's data sheet can be used to find a more precise value for the worst-case saturation voltage.

Slew-Rate Limiting Frequency. As with the amplifier configurations discussed previously, the highest frequency that can be amplified with a full output voltage swing and no slew-rate limited distortion is computed as in Equation (2.11):

$$\begin{aligned} f_{SRL} &= \frac{slew\ rate}{\pi v_O(\text{max})} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 26\ V} \\ &= 6.12\ kHz \end{aligned}$$

If it is known for certain that the actual output swing will never be required to reach its limits, then the lower actual output swing can be used to compute the slew-rate limiting frequency.

Maximum Input Voltage Swing. Since the amplifier has a voltage gain of 1, the maximum input voltage swing is equal to the maximum output voltage swing. Thus, in the case of Figure 2.16, we could have an input signal as large as ±13 volts without causing the amplifier to saturate. Again, if you plan to push the amplifier to its limits, you should refer to the manufacturer's data sheet and select the worst-case output saturation voltage at the worst-case temperature. The computations, however, remain similar.

Output Impedance. The output impedance of the voltage follower can be computed as follows:

$$r_O = \frac{output\ impedance(open\ loop)}{A_{OL}} \tag{2.31}$$

where A_{OL} is the open-loop gain of the op amp at the specified frequency. You can determine the value of A_{OL} at the desired operating frequency as in Equation (2.16):

$$A_{OL} = \frac{f_{UG}}{f_{IN}}$$

where f_{IN} is the specific input frequency being considered.

For the circuit in Figure 2.16, the open-loop gain at 5 kilohertz, for example, is

$$\begin{aligned} A_{OL} &= \frac{f_{UG}}{f_{IN}} \\ &= \frac{1.0\ MHz}{5\ kHz} \\ &= 200 \end{aligned}$$

The output impedance then becomes Equation (2.31).

$$\begin{aligned} r_O &= \frac{output\ impedance(open\ loop)}{A_{OL}} \\ &= \frac{75\ \Omega}{200} \\ &= 0.375\ \Omega \end{aligned}$$

As with most op amp circuits, the output impedance is so low relative to any practical load resistance that its effects may be ignored.

Output Current Capability. The total current flowing in or out of the output terminal of the op amp in Figure 2.16 may be delivered directly to the load. That is, the feedback current is extremely small and can be disregarded in nearly all cases. As the load resistance varies from infinity (open) to 0 (short), the output current from the op amp varies from 0 to the short-circuit value of 20 milliamps (given in the data sheet). The limiting factor is the amount of reduction that can be tolerated on the output voltage swing.

On an unprotected op amp, the value of load current must be kept below the stated output current rating. If this value is not supplied in the data sheet, it can be estimated by using the maximum power dissipation data; recall that *power* = *voltage* × *current*.

Bandwidth. The bandwidth (i.e., the upper cutoff frequency) of a voltage follower circuit may be estimated by the following equation:

$$bw = f_{UG} \tag{2.32}$$

For the circuit shown in Figure 2.16, we can compute the upper cutoff frequency and/or bandwidth as follows:

$$bw = f_{UG} = 1.0\ MHz$$

At lower frequencies, the voltage gain will be nearly equal to the calculated value of unity. As the frequency approaches the upper cutoff, the voltage gain begins to decrease. Once the input frequency exceeds 1.0 megahertz (for a 741), the overall circuit gain will decrease dramatically.

Power Supply Rejection Ratio. The change in output voltage (v_O) for a given change in DC power line noise voltage (v_N) is computed for the voltage follower with the following equation:

$$v_{NO} = v_N PSRR \tag{2.33}$$

where v_O, v_N, and $PSRR$ are the values of the output noise signal, the noise signal on the DC supply lines, and the power supply rejection ratio, respectively. The manufacturer's data sheet in Appendix 1 lists the power supply rejection ratio (PSRR) as ranging from 30 to 150 microvolts per volt. The worst-case effect on the output voltage for the circuit in Figure 2.16 is then

$$\begin{aligned} v_{NO} &= v_N PSRR \\ &= v_N \times 150\ \mu V/V \end{aligned}$$

In other words, the amplitude of the power line noise (v_N) will be reduced by a factor of 0.000150. This means, for example, that if the DC supply lines had noise signals of 100 millivolts peak-to-peak, we could anticipate a similar signal in the output with an amplitude of about

$$\begin{aligned} v_{NO} &= v_N \times 150\ \mu V/V \\ &= 100\ mV \times 150\ \mu V/V \\ &= 15\ \mu V\ peak\text{-}to\text{-}peak \end{aligned}$$

2.4.3 Practical Design Techniques

The design of a voltage follower circuit is fairly straightforward because of the lack of circuit complexity. Let us examine the design procedure by designing a voltage follower with the following characteristics:

1. Input voltage range	100 to 500 millivolts RMS
2. Frequency range	DC to 75 kilohertz
3. Load resistance	4.7 kilohms
4. Input resistance	greater than 100 kilohms
5. Source impedance	1.8 kilohms

Select the Op Amp. First, we must select an op amp that can provide unity gain up to the maximum input frequency. That means we will need an op amp with a unity gain bandwidth of at least Equation (2.32):

$$\begin{aligned} f_{UG} &= f_{MAX} \\ &= 75\ kHz \end{aligned}$$

Second, the slew rate of the op amp must be adequate to allow the required output voltage swing at the highest input frequency. The required slew rate is given by Equation (2.11):

$$\begin{aligned} slew\ rate(\text{min}) &= \pi f_{SRL} v_O(\text{max}) \\ &= 3.14 \times 75\ kHz \times 500\ mV \times 1.414 \times 2 \\ &= 0.333\ V/\mu s \end{aligned}$$

Since both the unity gain frequency and the slew rate requirements are within the limits of the 741 (see Appendix 1), let us choose this device for our design.

Select the Power Supply Voltages. Now we must select a power supply voltage that is high enough to prevent saturation on the highest input voltage. The worst-case internal voltage drop on the output for a 741 is listed as 5 volts in Appendix 1 for load resistances between 2 and 10 kilohms. A more typical value is 2 volts. The minimum required power supply voltage can be determined as in Equation (2.25):

$$\begin{aligned} \pm V_{MIN} &= v_I(peak) + V_{INT} \\ &= 500\ mV \times 1.414 + 5\ V \\ &= 5.707\ V \end{aligned}$$

We will choose a more standard value of ±15 volts for our power supply voltages. The complete schematic of our voltage follower circuit is shown in Figure 2.17.

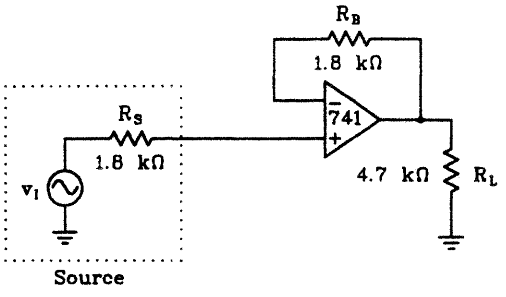


FIGURE 2.17 A voltage follower design that includes a compensation resistor (R_B).

Now let us check to be sure the 741 can supply the required current to our load without causing an appreciable voltage loss in our output. When the output voltage reaches its maximum level, the load current can be computed with Ohm's Law as

$$\begin{aligned} i_L(peak) &= \frac{v_O(peak)}{R_L} \\ &= \frac{500\ mV \times 1.414}{4.7\ k\Omega} \\ &= 150\ \mu A \end{aligned}$$

This should have negligible effect on the output voltage of the op amp because the 741 can supply significantly higher currents.

Figure 2.17 also illustrates the use of a compensating resistor R_B. Recall from the previous amplifier designs that bias current in the op amp can cause output offsets because of the voltage drops across any resistances in line with the bias current. We minimize this offset by providing equal resistances in both (+) and (–) inputs. The resistance in the (+) input is simply the source resistance that was given as 1.8 kilohms. To minimize output errors, we insert an equal value R_B in the feedback loop. Note that no significant signal current flows through R_B. Therefore, the voltage gain is unaffected by the addition of R_B, and it remains constant at unity.

The actual performance of our voltage follower circuit is shown in Figure 2.18 through the use of an oscilloscope plot. The measured performance is compared to the design goals in Table 2.3.

TABLE 2.3

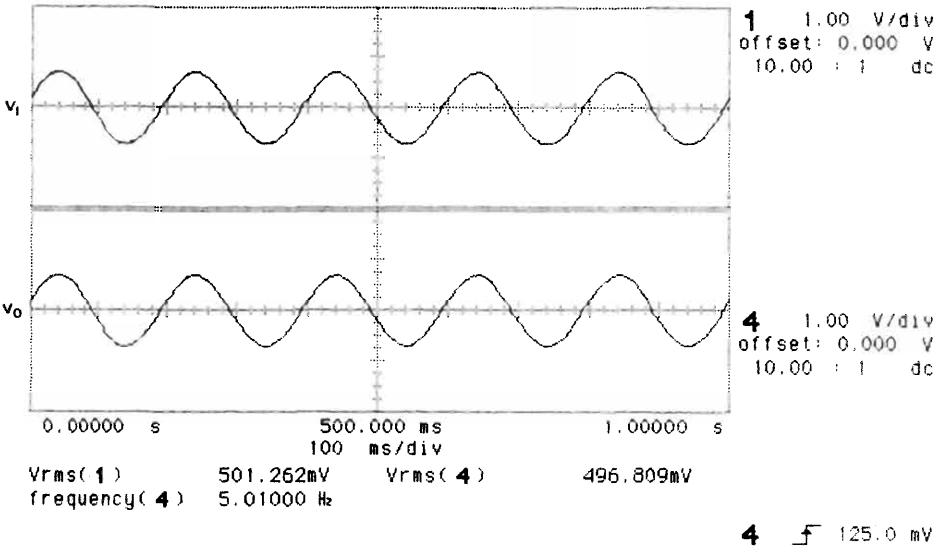
Parameter	*Design Goal*	*Measured Values*
Input resistance	>100 *k*Ω	>100 *k*Ω
Voltage gain	1.0	0.97–0.99
Frequency range	DC–75 *kHz*	DC–>75 *kHz*

2.5 INVERTING SUMMING AMPLIFIER

2.5.1 Operation

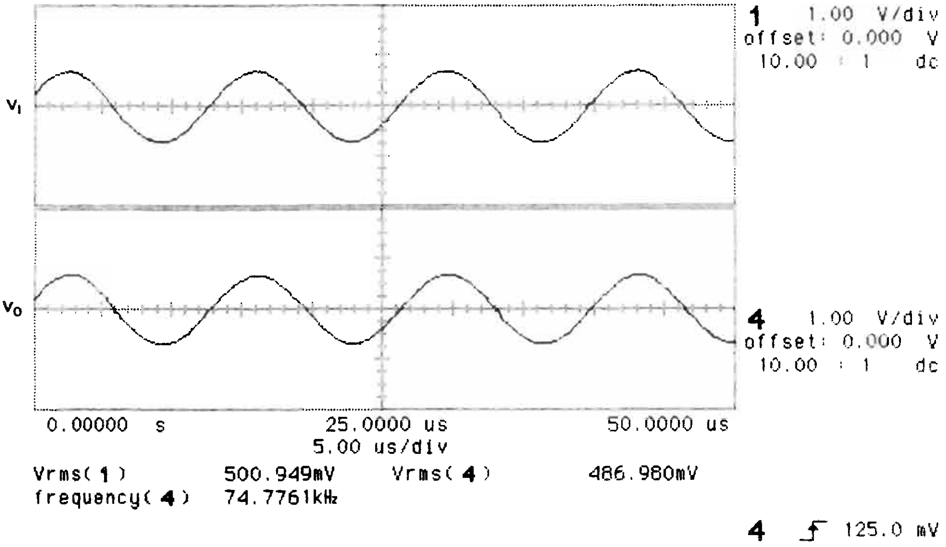
Figure 2.19 shows the schematic diagram for an inverting summing amplifier. The summing amplifier has several inputs—the circuit in Figure 2.19 shows four with the possibility of others indicated. Although the input sources are shown as DC signals (i.e., batteries) the circuit works equally well for AC signals or even a combination of AC and DC signals.

There are several ways to understand the operation of the inverting summing amplifier circuit. One simple method is an application of the Superposition



Low-Frequency Performance

(a)



High-Frequency Performance

(b)

FIGURE 2.18 Oscilloscope displays showing the performance of the voltage follower circuit shown in Figure 2.17. (Test equipment courtesy of Hewlett-Packard Company.)

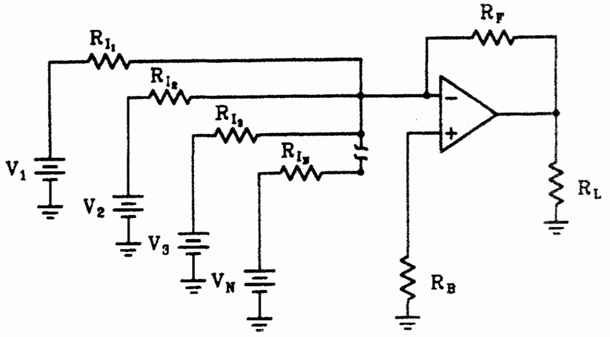


FIGURE 2.19 An inverting summing amplifier circuit.

Theorem. In this case, we consider the effects of each input signal one at a time with all other sources being set to 0. We know from our discussion of the basic inverting amplifier that the (−) input terminal is a virtual ground point. That is, unless the amplifier's output is saturated, the voltage on the (−) input will be within a few microvolts of ground potential. Thus, when we replace all but one source with a short (i.e., set them to 0 volts), the associated input resistors essentially have a ground connection on both ends. In other words, one end of each resistor is connected to ground through the temporary short that we inserted across the battery as part of the application of the Superposition Theorem. The opposite end of each input resistor is connected to the (−) input, which we know is a virtual ground point. As all input resistors but one have ground potential on both sides, there will be no current flow through them and they can be totally disregarded for the remainder of our analysis.

By disregarding all input resistors and sources but one, we are left with a simple single-input inverting amplifier circuit. We already know how this circuit works, so we can now compute voltage gain, input current, output voltage, and so on, for this single input. We can then perform a similar analysis for each of the other inputs one at a time. The actual output voltage of the circuit is the combination or sum of the effects of the individual inputs.

One important point that should be recognized about the circuit shown in Figure 2.19 is that the gains for each input signal are independent. That is, the ratio of R_F to R_{I1} will determine the voltage gain that signal V_1 receives. V_2, on the other hand, is amplified by a factor established by the ratio of R_F and R_{I2}. Thus, we can quickly conclude that the individual gains can be varied by changing the values of the input resistors, while the gains of all signals can be changed simultaneously by varying the value of R_F. Consider, for example, that the circuit is being used as a microphone mixer. The signals from several microphones provide the inputs to the circuit. If the individual input resistors are variable, then they adjust the amplitude (i.e., volume) of one microphone relative to another. If the feedback resistor is also variable, it serves as a master volume control because it varies the amplification of all microphone signals but does not change the strength of one relative to another.

Resistor R_B is a compensating resistor and ensures that both inputs of the op amp have similar resistances to ground. You will recall that this helps minimize problems caused by the op amp's bias currents.

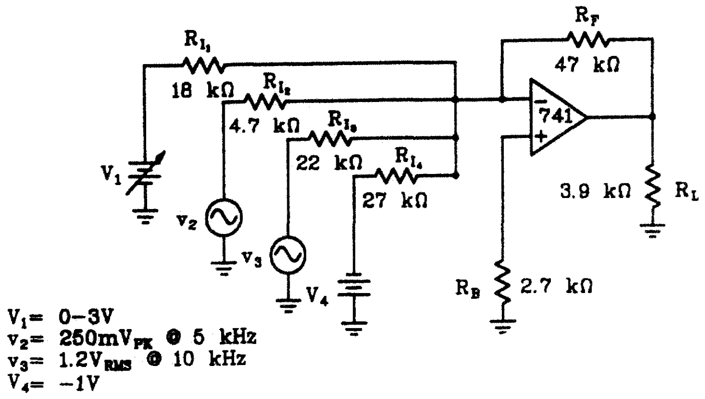


FIGURE 2.20 An inverting summing amplifier circuit used for a numerical analysis example.

2.5.2 Numerical Analysis

We will now analyze the numerical performance of an inverting summing amplifier circuit. The circuit to be analyzed is shown in Figure 2.20. Compute the following characteristics of the circuit:

1. Voltage gain of each input signal
2. Input impedance of each input signal
3. Input current requirement for each input signal
4. Maximum output voltage swing (total)
5. Maximum input voltage swing (individual)
6. Output impedance
7. Output current capability
8. Bandwidth
9. Slew-rate limiting frequency

Voltage Gain. The voltage gain for each input signal in Figure 2.20 must be computed separately. Each gain, however, is computed in the same manner, Equation (2.6), as a simple inverting amplifier circuit. That is,

$$A_V = -\frac{R_F}{R_I}$$

where the minus sign is used to remind us of the phase inversion given to each signal.

The individual voltage gains for the circuit in Figure 2.20 are computed:

$$A_{V_1} = -\frac{R_F}{R_{I_1}} = -\frac{47\ \text{k}\Omega}{18\ \text{k}\Omega} = -2.6$$

$$A_{V_2} = -\frac{R_F}{R_{I_2}} = -\frac{47\ k\Omega}{4.7\ k\Omega} = -10$$

$$A_{V_3} = -\frac{R_F}{R_{I_3}} = -\frac{47\ k\Omega}{22\ k\Omega} = -2.1$$

$$A_{V_4} = -\frac{R_F}{R_{I_4}} = -\frac{47\ k\Omega}{27\ k\Omega} = -1.7$$

Observe that each of these calculations is similar to our analysis on a single-input inverting amplifier and that the gains are independent of each other.

Input Impedance. The input impedance seen by each input is equal to the value of the input resistor on that particular input. That is, since each input resistor connects to a virtual ground point, its respective source sees it as the total input impedance. No calculations are required to determine the input impedance; we simply inspect the input resistors' individual values.

Input Current Requirement. Each source must supply the current for its own input. The amount of current can be determined by Ohm's Law and is simply the input voltage divided by the input resistance, Equation (2.8). For the circuit shown in Figure 2.20, we can compute the following values:

$$i_{I_1} = \frac{V_1}{R_{I_1}} = \frac{3\ V}{18\ k\Omega} = 167\ \mu A$$

$$i_{I_2} = \frac{v_2}{R_{I_2}} = \frac{250\ mV}{4.7\ k\Omega} = 53\ \mu A\ peak$$

$$i_{I_3} = \frac{v_3}{R_{I_3}} = \frac{1.2\ V \times 1.414}{22\ k\Omega} = 77\ \mu A\ peak$$

$$i_{I_4} = \frac{V_4}{R_{I_4}} = \frac{1.0\ V}{27\ k\Omega} = 37\ \mu A$$

In the case of V_1, a variable DC source, we computed the worst-case input current by using the maximum input voltage (3 volts). Similarly, for the alternating voltage sources v_2 and v_3, we used peak values of input voltage. In each of these cases, the source must be capable of supplying the required current.

Maximum Output Voltage Swing. The output voltage of the summing amplifier is limited by the $\pm V_{SAT}$ values. For the purposes of this analysis, we will estimate the values of $\pm V_{SAT}$ to be 2 volts below the DC power supply values. The calculations, Equation (2.10), to determine the maximum output voltage swing are

$$\begin{aligned} v_O(\max) &= +V_{SAT} - (-V_{SAT}) \\ &= +13\ V - (-13\ V) \\ &= 26\ V \end{aligned}$$

As with previous circuits, we can utilize the data sheet supplied by the manufacturer if it becomes necessary to have a more accurate, or perhaps worst-case, value.

Maximum Input Voltage Swing. The maximum input voltage swing of an amplifier is the voltage that causes the amplifier's output to reach saturation. Input voltages that exceed this limit will produce distorted (i.e., clipped) output signals. In the case of the summing amplifier, the situation is more complex than with previous, single-input amplifiers. That is, the instantaneous level of output is determined by the instantaneous values of input voltage on all inputs. First we will consider each input separately to determine the maximum levels of an isolated input. The calculations, from Equation (2.1), are similar to those used with previous circuits.

$$\textit{maximum input voltage swing} = \frac{\textit{maximum output voltage swing}}{A_V}$$

where A_V is the voltage gain received by a particular input. The individual calculations are

$$\begin{aligned}
V_1(\max) &= \frac{-13\ V}{-2.6} = 5\ V\ DC \\
v_2(\max) &= \frac{26\ V}{10} = 2.6\ V\ \textit{peak-to-peak} \\
v_3(\max) &= \frac{26\ V}{2.1} = 12.4\ V\ \textit{peak-to-peak} \\
V_4(\max) &= \frac{13\ V}{-1.7} = -7.6\ V
\end{aligned}$$

Note that the negative and positive saturation limits were used as the maximum output "swing" for V_1 and V_4, respectively, since these two inputs are DC and will only be limited by one saturation barrier.

With reference to v_2 and v_3, we may want to express them in their peak and RMS forms to better compare them with the signals shown in Figure 2.20. These conversions are

$$\begin{aligned}
v_2(\textit{peak}) &= \frac{v_2(p-p)}{2} = \frac{2.6\ V}{2} = 1.3\ V\ \textit{peak} \\
v_3(\textit{RMS}) &= \frac{v_3(p-p)}{2.828} = \frac{12.4\ V}{2.828} = 4.39\ V\ \textit{RMS}
\end{aligned}$$

Since the maximum limits on all inputs (both DC and AC) are greater than the values listed on the schematic, we will assume that no single input can cause the amplifier output to saturate. However, two or more input signals may combine at some instant to drive the output to its saturation limit. Let us determine if this situation can occur in the circuit shown in Figure 2.20. To perform this calculation, we want to determine the worst-case combination of input signals. First observe that V_1 and V_4 are of opposite polarity and thus tend to reduce each other's effect in the output. A worst case would be when V_1 is zero or when V_1 is maximum (3 volts DC). Let us evaluate them with Equation (2.1) to determine the worst-case combination.

$$V_{O_1} = V_1 A_{V_1} = 3\ V \times (-2.6) = -7.8\ V\ DC$$

$$V_{O_4} = V_4 A_{V_4} = -1\ V \times (-1.7) = +1.7\ V\ DC$$

From these calculations we can see that if V_1 were reduced to zero, V_4 would produce +1.7 volts in the output. On the other hand, if V_1 were set for maximum (3 volts DC), the net output voltage would be the difference between the V_1-produced and V_4-produced outputs. This worst-case output voltage is simply –7.8 + 1.7, or –6.1 volts.

Now we must consider the effects of the AC signals v_2 and v_3. The worst-case output condition will occur when these two inputs hit their peak values simultaneously and have the same polarity as V_1. The output voltages produced individually by v_2 and v_3 are

$$v_{O_2} = v_2 A_{V_2} = 250\ mV \times (-10) = -2.5\ V\ peak$$

$$v_{O_3} = v_3 A_{V_3} = 1.2\ V \times 1.414 \times (-2.1) = -3.6\ V\ peak$$

The net effect of V_1, v_2, v_3, and V_4 can be found by adding the individual output values (Superposition Theorem).

$$\begin{aligned} v_O &= V_{O_1} + v_{O_2} + v_{O_3} + V_{O_4} \\ &= -7.8\ V - 2.5\ V - 3.6\ V + 1.7\ V \\ &= -12.2\ V \end{aligned}$$

Since this worst-case value is less than our maximum output voltage limit (±13 volts typically), we should not have a problem. In extreme cases, however, we may have a potential problem. Recall that the output limits of ±13 volts were obtained by using typical performance values for the 741. If worst-case values are used, we will find that the limits fall to ±10 volts under worst-case conditions. If this situation were to occur at the same time our inputs were all at their maximum values, we would drive the amplifier into saturation and produce a clipped output. If this is a serious concern for our particular application, we can reduce R_F slightly to prevent the combined signals from driving the output to saturation.

Output Impedance. The output impedance of the summing amplifier can be estimated as follows:

$$\text{output impedance(closed loop)} = r_O = \frac{\text{output impedance(open loop)}}{A_{OL}Y + 1} \tag{2.34}$$

where A_{OL} is the open-loop gain of the op amp at the specified frequency and Y is computed as follows:

$$Y = \frac{R_{I_1} \| R_{I_2} \| R_{I_3} \| R_{I_4}}{(R_{I_1} \| R_{I_2} \| R_{I_3} \| R_{I_4}) + R_F} \tag{2.35}$$

Now let us compute the output impedance for the circuit in Figure 2.20. First we compute the value of the parallel combination of input resistors (R_X):

$$\begin{aligned} R_X &= \frac{1}{\frac{1}{R_{I_1}} + \frac{1}{R_{I_2}} + \frac{1}{R_{I_3}} + \frac{1}{R_{I_4}}} \\ &= \frac{1}{\frac{1}{18\ k\Omega} + \frac{1}{4.7\ k\Omega} + \frac{1}{22\ k\Omega} + \frac{1}{27\ k\Omega}} \\ &= 2.85\ k\Omega \end{aligned}$$

Then we use this value to compute the factor Y, Equation (2.35):

$$\begin{aligned} Y &= \frac{R_X}{R_X + R_F} \\ &= \frac{2.85\ k\Omega}{2.85\ k\Omega + 47\ k\Omega} \\ &= 0.057 \end{aligned}$$

Next we determine the value of A_{OL} at the frequency of interest, using Equation (2.16). We will use the worst-case value that occurs at the highest input frequency (10 kilohertz):

$$\begin{aligned} A_{OL} &= \frac{f_{UG}}{f_{IN}} \\ &= \frac{1.0\ MHz}{10\ kHz} \\ &= 100 \end{aligned}$$

Finally we compute the estimated value of output resistance, from Equation (2.35):

$$\begin{aligned} r_O &= \frac{\textit{output impedance}(\textit{open loop})}{A_{OL}Y + 1} \\ &= \frac{75\ \Omega}{100 \times 0.057 + 1} \\ &= 11\ \Omega \end{aligned}$$

Since this value was computed at the highest input frequency (worst case), and since it is very low compared to the value of the load resistor, its effects on output voltage can be safely ignored.

Output Current Capability. The maximum value of load current occurs when the output reaches its highest instantaneous value. The maximum voltage was previously computed as 12.2 volts. The worst-case load current can be computed with Ohm's Law:

$$\begin{aligned} i_L(\text{max}) &= \frac{v_O(\text{max})}{R_L} \\ &= \frac{12.2\ V}{3.9\ k\Omega} \\ &= 3.13\ mA \end{aligned}$$

The output of the op amp must also supply the feedback current. In most applications, this current can be ignored because it is generally much smaller than the load current. Our present circuit is no exception. That is, we can see by inspection that the feedback path has over 10 times as much resistance as the load.

The data sheet in Appendix 1 indicates that even under worst-case conditions, the output can maintain at least 10 volts across a 2000-ohm load. By Ohm's Law, we can conclude that this corresponds to an output current of

$$i_O = \frac{v_O}{R_L} = \frac{10\ V}{2\ k\Omega} = 5\ mA$$

Of course, the typical value of current is even higher. In any case, the current capability of the output clearly exceeds our requirements and therefore poses no problem. If our load resistor were smaller, we could anticipate a reduced output voltage.

Bandwidth. For a meaningful discussion on bandwidth, we must consider the response of each input individually. When the responses are considered separately, we can estimate the bandwidth of any given input by applying the bandwidth equation, Equation (2.22), used in previous analyses:

$$bw = \frac{f_{UG}R_I}{R_F + R_I}$$

We know from earlier calculations that the bandwidth will decrease as the closed-loop gain is increased. Let us calculate the bandwidth for the input in Figure 2.20 that has the highest gain. We have already determined the individual gains to be 2.6, 10, 2.1, and 1.7 for inputs V_1 through V_4. We will compute the bandwidth for the v_2 input because its gain is the highest. Incidentally, there would be very little point in computing the bandwidth for inputs V_1 and V_4 because these have DC signals applied. The bandwidth for the v_2 input is

$$\begin{aligned} bw &= \frac{f_{UG}R_L}{R_F + R_I} \\ &= \frac{1.0\ MHz \times 4.7\ k\Omega}{47\ k\Omega + 4.7\ k\Omega} \\ &= 90.9\ kHz \end{aligned}$$

A similar analysis could be made for input v_3, which has a computed gain of 2.1 and a maximum input frequency of 10 kilohertz. For large amplitude output signals, the slew rate will tend to restrict the operation to even lower frequencies. This is discussed in the following section.

Slew-Rate Limiting Frequency. As discussed for previous amplifier configurations, the slew rate also limits the highest operating frequency for larger output voltage excursions. The slew-rate limiting frequency is found as follows, Equation (2.11):

$$\begin{aligned} f_{SRL} &= \frac{slew\ rate}{\pi v_O(\max)} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 26\ V} \\ &= 6.12\ kHz \end{aligned}$$

Thus, although the v_2 input was shown to have a 90.9-kilohertz bandwidth as established by the unity gain frequency, the full-power upper limit is only 6.12 kilohertz. In the given application, however, the applied signal is only 5000 hertz, so this should not hamper the operation of the circuit with respect to the v_2 input.

The v_3 input, on the other hand, operates at 10 kilohertz. This means that we can never get the full 26-volt swing in the output as a result of v_3 signals. The schematic indicates that the highest input voltage is 1.2 volts RMS. The gain for v_3 was previously computed as 2.1. The largest normal output swing from v_3 can be found by applying Equation (2.1):

$$\begin{aligned} v_O(\max) &= V_3(RMS) \times 1.414 \times 2 \times A_V \\ &= 1.2\ V \times 1.414 \times 2 \times 2.1 \\ &= 7.13\ V\ peak\text{-}to\text{-}peak \end{aligned}$$

The actual slew-rate limiting frequency for this input is then estimated with Equation (2.11) as

$$\begin{aligned} f_{SRL} &= \frac{slew\ rate}{\pi v_O(\max)} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 7.13\ V} \\ &= 22.3\ kHz \end{aligned}$$

In the given circuit, the slew rate should not interfere with the expected operation.

2.5.3 Practical Design Techniques

To illustrate the design method for an inverting summing amplifier circuit, let us design a 3-input circuit with the following performance characteristics:

Input 1. 0 to 500 millivolts peak, at a frequency of 2.7 kilohertz. The source resistance is 1.0 kilohms, and the signal is to be amplified by a factor of –3.5.

Input 2. –2 to +2 volts DC. The source resistance is 0.75 ohms, and the voltage is to pass through the circuit without amplification (i.e., inversion only).

Input 3. 0 to 3 volts RMS, at a frequency of 500 hertz. The source resistance is 50 ohms, and the signal is to be amplified by a factor of –2.

Recall that the minus signs preceding the gain factors tell us that the signals are inverted in the process of being amplified. The negative gains **do not** imply voltage reduction.

The output of the amplifier must drive a load resistance that varies from 10 to 50 kilohms.

Determine the Worst-Case Input. Our initial step is to determine which input to design first. If we choose the wrong one, we will end up recalculating some of our values. The proper input can be identified by choosing the one that has the highest product of source resistance multiplied by voltage gain (absolute value). These calculations are shown for comparison:

Input 1. $1000\ \Omega \times 3.5 = 3500$
Input 2. $0.75\ \Omega \times 1 = 0.75$
Input 3. $50\ \Omega \times 2 = 100$

Since input 1 has the highest gain-source-resistance product, we will begin by selecting the input resistor for input 1.

Choose the Value for the First Input Resistor. The source resistance and the input resistor are in series. Their sum in conjunction with R_F will determine the voltage gain of that input. In theory, there is no requirement to have a physical resistor for R_I—the source resistance alone can serve as the input resistor. In practice, however, the source resistance is usually only an estimate and rarely a constant; therefore, it is generally wise to include a separate resistor as R_I and to make this resistor large enough to minimize the effects of changes in the source resistance. The application must dictate the degree of stability needed, but in general, if the input resistor is 10 times as large as the source resistance, then the effects of changes in the source resistance are reduced by about 90%. If greater protection is needed, increase R_I accordingly.

For purposes of our sample design, let us choose R_{I1} to be 10 times the value of source resistance. The value of R_{I1} then is computed as

$$\begin{aligned} R_{I_1} &= 10 \times R_{S_1} \\ &= 10 \times 1.0\ k\Omega \\ &= 10\ k\Omega \end{aligned}$$

Calculate the Required Feedback Resistor (R_F). The feedback resistor is calculated by using a transposed version of the basic voltage gain equation, Equation (2.6), for an inverting amplifier.

$$\begin{aligned} A_V &= -\frac{R_F}{R_I},\ or \\ R_F &= -A_V R_I \end{aligned}$$

In our particular circuit,

$$\begin{aligned} R_F &= -A_V R_I \\ &= -(-3.5) \times 10\ k\Omega \\ &= 35\ k\Omega \end{aligned}$$

We choose the nearest standard (5% tolerance) value of 36 kilohms.

Compute the Remaining Input Resistors. Values for each of the remaining input resistors can be calculated by using yet another transposed version of the basic voltage gain equation, Equation (2.6).

$$\begin{aligned} A_V &= -\frac{R_F}{R_I},\ or \\ R_I &= -\frac{R_F}{A_V} \end{aligned}$$

Using this equation, we can now compute values for R_{I2} and R_{I3} as follows:

$$\begin{aligned} R_{I_2} &= -\frac{R_F}{A_{V_2}} \\ &= -\frac{36\ k\Omega}{-1} \\ &= 36\ k\Omega \end{aligned}$$

and

$$\begin{aligned} R_{I_3} &= -\frac{R_F}{A_{V_3}} \\ &= -\frac{36\ k\Omega}{-2} \\ &= 18\ k\Omega \end{aligned}$$

Compute the Value of R_B. To minimize the effects of op amp bias currents, we want to make the value of R_B equal to the parallel combination of R_F and all of the input/source resistors.

$$R_B = \frac{1}{\dfrac{1}{R_F} + \dfrac{1}{R_{I_1} + R_{S_1}} + \dfrac{1}{R_{I_2} + R_{S_2}} + \dfrac{1}{R_{I_3} + R_{S_3}}} \tag{2.36}$$

In our present case, the value of R_B is computed as

$$\begin{aligned} R_B &= \frac{1}{\dfrac{1}{36\ k\Omega} + \dfrac{1}{10\ k\Omega + 1\ k\Omega} + \dfrac{1}{36\ k\Omega + 0.75\ \Omega} + \dfrac{1}{18\ k\Omega + 50\ \Omega}} \\ &= 4.95\ k\Omega \end{aligned}$$

We select the nearest standard value of 5.1 kilohms.

Determine the Required Power Supply Voltages. The DC power supply voltages must be high enough to prevent saturation under the worst-case input conditions. Generally, the condition to be considered is when all inputs are at the maximum voltage at the same time. The worst-case output voltage, then, is computed by adding the output voltages caused by each of the individual inputs, as in Equation (2.1).

$$\begin{aligned} v_{O_1}(\text{max}) &= v_1(\text{max}) \times A_{V_1} = 500\ mV \times (-3.5) = -1.75\ V \\ v_{O_2}(\text{max}) &= v_2(\text{max}) \times A_{V_2} = 2\ V \times (-1) = -2.0\ V \\ v_{O_3}(\text{max}) &= v_3(\text{max}) \times A_{V_3} = 3\ V \times 1.414 \times (-2) = -8.48\ V \end{aligned}$$

The worst-case output will be

$$\begin{aligned} v_O(\text{max}) &= v_{O_1}(\text{max}) + v_{O_2}(\text{max}) + v_{O_3}(\text{max}) \\ &= (-1.75\ V) + (-2\ V) + (-8.48\ V) \\ &= -12.2\ V \end{aligned}$$

Unless the internal drop on the output of the selected op amp is unusually high, we should be able to use standard ±15-volt supplies. Suppose, for example, we decide to use a 741 op amp. The manufacturer's data sheet in Appendix 1 indicates that the op amp can deliver at least ±12 volts to a load ≥10 kilohms when ±15-volt supplies are used. We will plan to use a 741 unless we encounter problems with bandwidth or slew rate (verified in subsequent sections).

Determine the Required Unity Gain Frequency. The minimum unity gain frequency for each input is computed with Equation (2.22):

$$\begin{aligned} f_{UG_1} &= \frac{bw(R_F + R_{I_1})}{R_{I_1}} = \frac{2.7\ kHz(36\ k\Omega + 10\ k\Omega)}{10\ k\Omega} = 12.4\ kHz \\ f_{UG_2} &= \textit{Not applicable to DC inputs} \\ f_{UG_3} &= \frac{bw(R_F + R_{I_3})}{R_{I_3}} = \frac{500\ Hz(36\ k\Omega + 18\ k\Omega)}{18\ k\Omega} = 1.5\ kHz \end{aligned}$$

In all cases, the required minimum unity gain bandwidth is substantially below the 1.0-megahertz limit of a 741. Therefore, we will initially plan to use a 741 in our design. If the minimum bandwidth requirement were greater than 1.0 megahertz, we would have to select a different op amp.

Determine the Required Slew Rate. The minimum acceptable slew rate for the op amp is given by the following equation, Equation (2.11):

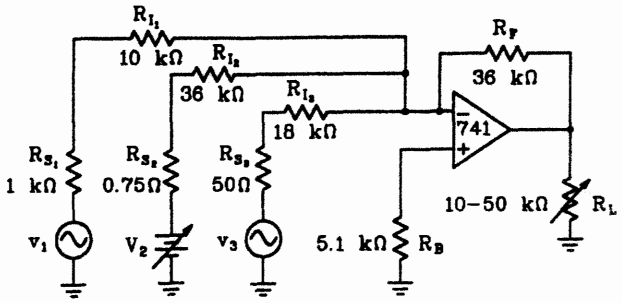
$$\textit{slew rate}(\text{min}) = \pi f_{SRL} v_O(\text{max})$$

Let us determine the minimum slew rate for each input:

$$\begin{aligned} &\textit{slew rate}(\text{min})\ 1 = 3.14 \times 2.7\ kHz \times 3.5\ V = 0.03\ V/\mu S \\ &\textit{slew rate}(\text{min})\ 2 = \textit{DC input} \\ &\textit{slew rate}(\text{min})\ 3 = 3.14 \times 500\ Hz \times 16.97\ V = 0.027\ V/\mu S \end{aligned}$$

In all cases, the required slew rate is substantially below the 0.5-volts-per-microsecond rating of the 741. Therefore, we will select this device as our final choice.

The schematic of our design is shown in Figure 2.21. The actual performance of the circuit is evident from the oscilloscope displays in Figure 2.22. The measured performance is contrasted with the original design goals in Table 2.4.


R_{I_1}
10 kΩ
R_{I_2}
36 kΩ
R_{I_3}
18 kΩ
R_F
36 kΩ
741
R_{S_1}
1 kΩ
R_{S_2}
0.75Ω
R_{S_3}
50Ω
v_1
V_2
v_3
5.1 kΩ
R_B
10–50 kΩ
R_L

v_1 = 0–500mV$_{PK}$ @ 2.7 kHz
V_2 = ±2V
v_3 = 3V$_{RMS}$ @ 500 Hz

FIGURE 2.21 The final design of a 3-input inverting summing amplifier circuit.

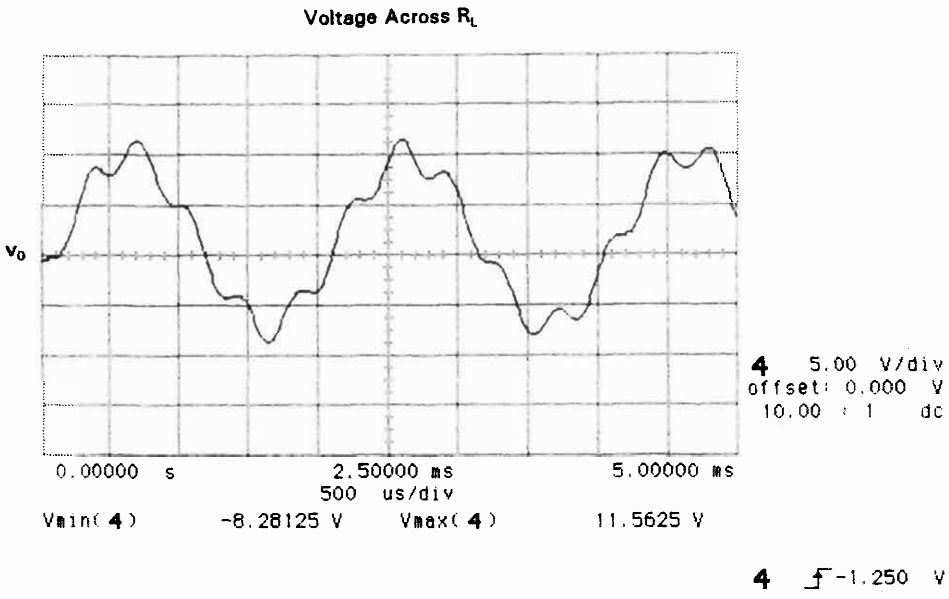


FIGURE 2.22 Oscilloscope display showing the actual performance of the inverting summing amplifier shown in Figure 2.21. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 2.4

Parameter	*Design Goal*	*Measured Value*
Voltage gain 1	–3.5	–3.27
Voltage gain 2	–1.0	–1.0
Voltage gain 3	–2.0	–1.99

2.6 NONINVERTING SUMMING AMPLIFIER

2.6.1 Operation

Figure 2.23 shows a 3-input, noninverting summing amplifier circuit. Its operation is significantly more difficult to analyze than that of the inverting summing amplifier. In the present case, we will need to rely heavily on the use of Thevenin's Theorem to analyze the operation of the circuit. First, though, let us examine the fundamental theory of operation.

Although the network on the (+) input is somewhat difficult to analyze mathematically, we know intuitively that it must be equivalent to some value of voltage and some value of resistance. If we mentally replace the network on the (+) input with a simple voltage source and series resistance, we see that the circuit becomes a simple, familiar noninverting amplifier circuit. The gain of this equivalent circuit is determined by the ratio of R_F to R_I. So, with the single exception of the network on the (+) input, analysis of the circuit is quite straightforward.

2.6.2 Numerical Analysis

Now let us analyze the circuit shown in Figure 2.23 numerically. We will focus our efforts on the network associated with the (+) input terminal. If we can reduce this network to a simpler network consisting of a single voltage source and a single resistor, then we can analyze the rest of the circuit using the method presented for the simple noninverting amplifier.

To reduce the network on the (+) input, we apply Thevenin's Theorem in two stages. First, simplify V_1, V_2, and the associated resistors. Figure 2.24(a) shows the circuit divided between V_2 and V_3. Application of Thevenin's Theorem to the portion of the circuit on the left side of the break point gives us a Thevenin voltage (V'_{TH}) of 2 volts and a Thevenin resistance (R'_{TH}) of 2.78 kilohms. This equivalent circuit is shown in Figure 2.24(b) reconnected to the original V_3/R_3 circuit.

If we apply Thevenin's Theorem to the partially simplified circuit in Figure 2.24(b), we obtain the fully reduced equivalent circuit of Figure 2.24(c). Thus, the network of resistors and voltage sources on the (+) input of the summing amplifier

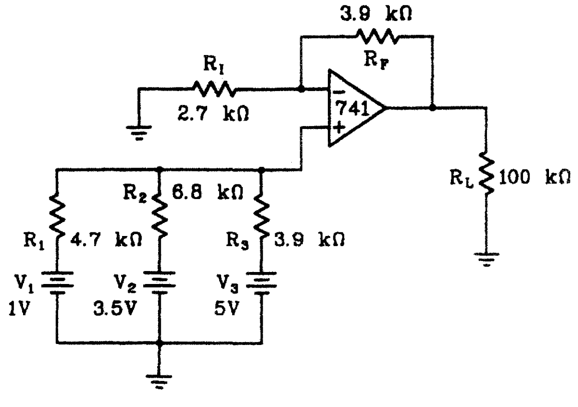
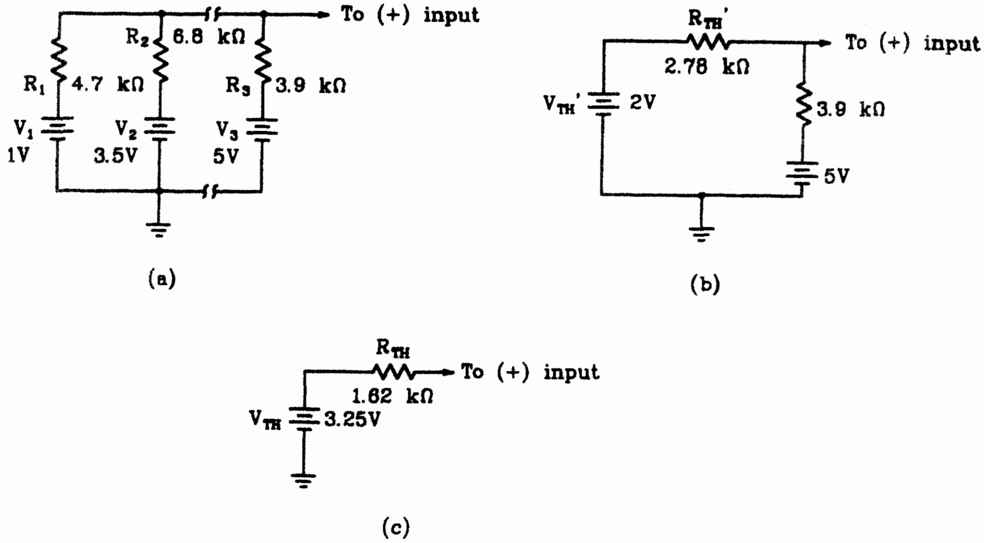


FIGURE 2.23 A 3-input noninverting summing amplifier.


To (+) input
R₂ 6.8 kΩ
R₁ 4.7 kΩ
R₃ 3.9 kΩ
V₁ 1V
V₂ 3.5V
V₃ 5V
R_TH'
2.78 kΩ
To (+) input
V_TH' 2V
3.9 kΩ
5V
R_TH
To (+) input
1.62 kΩ
V_TH 3.25V

(a)

(b)

(c)

FIGURE 2.24 Thevenin's Theorem is used to simplify the summing network for the noninverting summing amplifier.

originally shown in Figure 2.23 can be replaced by the Thevenin equivalent circuit shown in Figure 2.24(c). This substitution is shown in Figure 2.25.

We can now complete our analysis of the simplified circuit by applying techniques presented for the basic noninverting amplifier.

Voltage Gain. The voltage gain of the circuit in Figure 2.25 can be computed with the noninverting amplifier gain formula given in Equation (2.28).

$$\begin{aligned} A_V &= \frac{R_F}{R_I} + 1 \\ &= \frac{3.9\ k\Omega}{2.7\ k\Omega} + 1 \\ &= 2.44 \end{aligned}$$

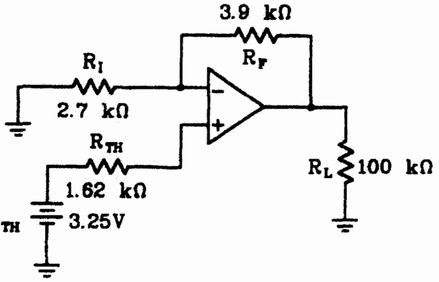

3.9 kΩ
R_F
R_I
2.7 kΩ
R_TH
1.62 kΩ
V_TH 3.25V
R_L 100 kΩ

FIGURE 2.25 The summing network shown in Figure 2.23 can be replaced by its Thevenin equivalent for analysis purposes.

Output Voltage. The output voltage of the circuit in Figure 2.25 can be determined by utilizing the basic gain equation of Equation (2.1):

$$A_V = \frac{v_O}{v_I}$$

Therefore,

$$\begin{aligned} v_O &= A_V v_I \\ &= 2.44 \times 3.25\ V \\ &= 7.93\ V \end{aligned}$$

2.6.3 Practical Design Techniques

The design of a noninverting summing amplifier like that shown in Figure 2.23 is an involved process, and the resulting design is difficult to alter without affecting several parameters. Therefore, many designers who need a noninverting summing amplifier utilize an inverting summing amplifier followed by a simple inverting amplifier. This arrangement is much simpler to design, easier to modify, and costs little more to build. With this in mind, we will not explore the details for designing the generic noninverting summing amplifier. However, we will discuss the design of a special case that uses the same basic circuit when we study adder circuits in Chapter 9.

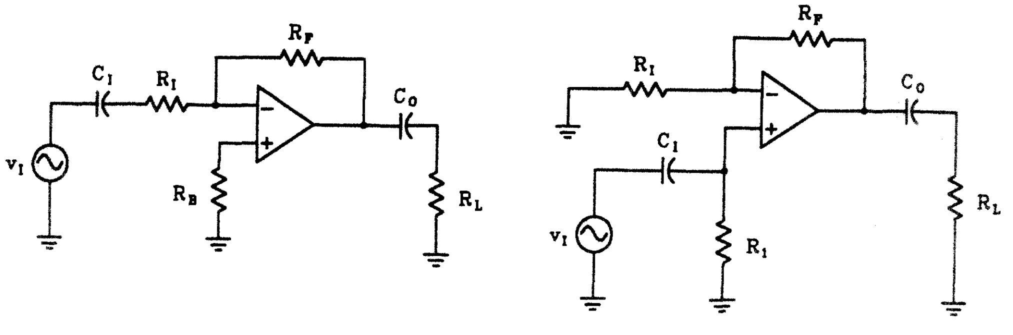
2.7 AC-COUPLED AMPLIFIER

2.7.1 Operation

The term *AC-coupled* identifies the fact that only AC signals are allowed to pass through the amplifier. DC and very-low-frequency AC signals are blocked or at least severely attenuated. The concept of AC coupling is applicable to many amplifier configurations. In the following discussion, we will consider the operation of the basic inverting and noninverting amplifier circuits when they are configured to be AC coupled. Most of the operation, analyses, and design methods are similar to their DC-coupled equivalents, which have been covered in detail. Therefore, we will concentrate on areas that are unique to the AC-coupled circuit.

First let us examine the operation of the AC-coupled inverting amplifier circuit shown in Figure 2.26(a).

You will recall from basic electronics theory that a capacitor blocks DC and passes AC. More specifically, a capacitor's opposition to current flow (capacitive reactance) increases as the applied frequency decreases. As the input frequency in Figure 2.26(a) decreases, the reactance of capacitors C_I and C_O both increase. As the reactance of C_I increases, the combined impedance of C_I and R_I also increases. Since the voltage gain of the inverting amplifier is determined by the ratio of the feedback resistor to the input resistance, and since the input resistance (actually



(a)

(b)

FIGURE 2.26 AC-coupled versions of the basic inverting amplifier (a) and the basic noninverting amplifier (b) circuits.

the combined impedance of C_I and R_I) is increasing, we know that the amplifier gain must be decreasing.

Another way to view the operation of the AC-coupled inverting amplifier is to consider that the output voltage of the amplifier is determined by the magnitude of feedback current. The feedback current that flows through R_F is identical to that which flows through R_I (ignoring the small bias current that flows in or out of the (–) input terminal). The value of current flow through R_I is determined by the magnitude of the input voltage and the impedance of R_I and C_I in combination. As the frequency decreases toward DC, the input current, and therefore the feedback current, must decrease. This lowered feedback current causes a corresponding decrease in output voltage. Because the input voltage is constant but the output voltage is decreasing, we can conclude that the amplifier's gain is dropping as the frequency is lowered.

The output capacitor C_O also affects the frequency response of the circuit. Basically, the output resistance of the op amp, the load resistance, and C_O form a series circuit across which the ideal output voltage is developed. That portion of the output voltage that appears across R_L is the final or effective output voltage of the circuit. The remaining voltage that is dropped across the internal resistance and across C_O is essentially lost. As the frequency in the circuit is decreased, the reactance of C_O increases. This causes a greater percentage of the output voltage to be dropped across C_O and leaves less to be developed across R_L. Thus, the effects of C_O also cause the frequency response to drop off on the low end and, in fact, prohibit the passage of DC signals.

Resistor R_B helps compensate for the effects of op amp bias currents. Its value will generally be the same as that of the feedback resistor, since the input resistor (R_I) is isolated by C_I for DC purposes.

The AC-coupled noninverting amplifier circuit shown in Figure 2.26(b) is nearly identical to its direct-coupled counterpart, which we discussed in an earlier section. Coupling capacitors C_I and C_O allow AC signals to be coupled in and out of the amplifier. Very-low-frequency signals and DC in particular are not coupled through the capacitors and are therefore not allowed to pass through the amplifier.

R_1 and C_I form an RC-coupling circuit on the input. That portion of the input signal that appears across R_1 is actually amplified by the circuit.

2.7.2 Numerical Analysis

Most of the calculations for the basic direct-coupled inverting and noninverting amplifier circuits apply to the AC-coupled inverting and noninverting amplifier, respectively. For purposes of our present analyses, we will determine the following circuit parameters:

1. Voltage gain
2. Input impedance
3. Bandwidth

We will use the circuits shown in Figure 2.27 for our numerical analysis example.

Voltage Gain. We will compute the overall voltage gain of the inverting circuit, Figure 2.27(a), by considering the gain to be made up of two parts. The first part of the gain is determined by all components to the left of C_O. The second part of the overall gain is determined by C_O and R_L. This latter part is actually a loss and tends to reduce the overall gain. Once these individual gains are computed, multiply them together to determine the overall voltage gain.

The voltage gain of the circuit to the left of C_O is computed in basically the same way, Equation (2.6), as a direct-coupled inverting amplifier. That is,

$$A_V = -\frac{R_F}{Z_I} \tag{2.37}$$

The only modification to our original equation is that the denominator must also include the effects of C_I. Therefore, instead of dividing by R_I (as we did with

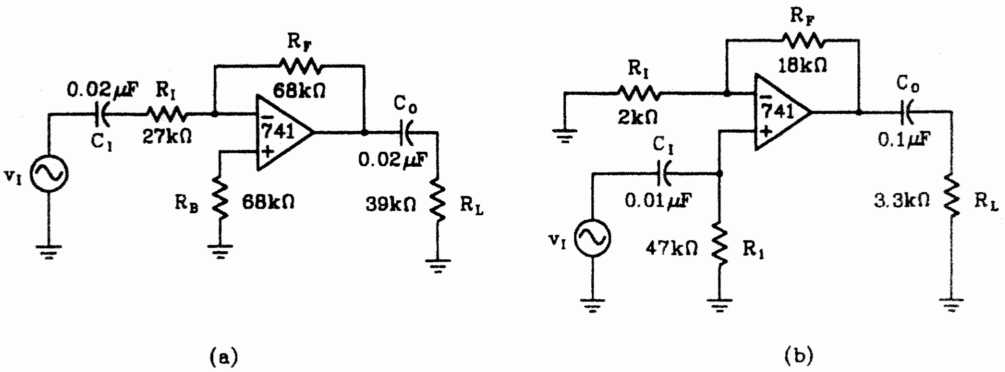


FIGURE 2.27 AC-coupled amplifier circuits used for numerical analysis examples.

the direct-coupled circuit), we simply divide by the net impedance of R_I and C_I (i.e., Z_I). You will recall from basic electronics that the net impedance of a series RC circuit is computed with the following equation:

$$Z = \sqrt{R^2 + X_C^2}$$

where X_C is the capacitive reactance of C_I. We already know that the gain of an op amp varies with frequency, but now we have introduced an even more obvious frequency-sensitive factor (X_C). Thus, when we speak of voltage gain, we must refer to a specific frequency in order to have a meaningful discussion. In most cases, we are interested in the lowest input frequency because this is where the capacitors will have their greatest effect (i.e., gain will be the lowest).

For the portion of the circuit in Figure 2.27(a) left of C_O, we can compute the voltage gain as shown. First, we need to determine the capacitive reactance with our basic electronics formula for X_C.

$$X_C = \frac{1}{2\pi fC}$$

For illustrative purposes, we will assume an input frequency of 800 hertz. The first step, then, is to calculate the reactance of C_I at the frequency of interest.

$$X_{C_I} = \frac{1}{6.28 \times 800\ Hz \times 0.02\ \mu F} = 9.95\ k\Omega$$

Now we can compute the impedance of R_I and C_I:

$$\begin{aligned} Z &= \sqrt{R^2 + X_C^2} \\ &= \sqrt{(27\ k\Omega)^2 + (9.95\ k\Omega)^2} \\ &= 28.8\ k\Omega \end{aligned}$$

Substituting this into the voltage gain equation, Equation (2.37), we can compute the gain of the circuit to the left of C_O.

$$\begin{aligned} A_{V_1} &= -\frac{R_F}{Z_I} \\ &= -\frac{68\ k\Omega}{28.8\ k\Omega} \\ &= -2.4 \end{aligned}$$

Recall that the minus sign indicates a phase inversion, but in no way implies a reduction in signal amplitude.

Our next step is to compute the effects of C_O and R_L. These two components form an RC voltage divider. You may apply your favorite circuit analysis method to determine the percentage of voltage that appears across R_L. This percentage is the effective "gain" of the RC-coupling circuit. For our purposes, we will use the following method, which is based on the resistive voltage divider formula:

$$A_V = \frac{R_L}{Z} \tag{2.38}$$

where Z is the net impedance of C_O and R_L.

First we compute the reactance of C_O at the frequency of interest (800 hertz in this case):

$$\begin{aligned} X_C &= \frac{1}{2\pi f C} \\ &= \frac{1}{6.28 \times 800\ Hz \times 0.02\ \mu F} \\ &= 9.95\ k\Omega \end{aligned}$$

Next we compute the net impedance of R_L and C_O:

$$\begin{aligned} Z &= \sqrt{R^2 + X_C^2} \\ &= \sqrt{(39\ k\Omega)^2 + (9.95\ k\Omega)^2} \\ &= 40.2\ k\Omega \end{aligned}$$

Finally, substituting this value into Equation (2.38), we compute our gain as

$$\begin{aligned} A_{V_2} &= \frac{R_L}{Z} \\ &= \frac{39\ k\Omega}{40.2\ k\Omega} \\ &= 0.97 \end{aligned}$$

That is to say, about 97% of the signal amplitude that appears at the output terminal of the op amp will be developed across R_L. The RC-coupling circuit appears to be working well at 800 hertz, since very little voltage is being lost across C_O.

The overall voltage gain for the circuit is found by multiplying these two gains as computed.

$$A_V(overall) = A_{V_1} \times A_{V_2} \tag{2.39}$$

For our example, we compute overall voltage gain as

$$A_V(overall) = -2.4 \times 0.97 = -2.33$$

Notice that the method described for computing overall voltage gain does not include the effects of the variations in open-loop gain at different frequencies. Although this additional consideration could be included as with the direct-coupled amplifier, it is not normally necessary because our calculations are accomplished at the lowest input frequency. If you want to compute the gain at some relatively high frequency, then you should include the effects of reduced op amp internal gain.

Another point that you may wish to consider involves phase shift. In addition to the 180-degree phase shift provided by the op amp itself, the signal also receives a phase shift from the two RC networks. The preceding calculations compute only the amplitude of the signal. If the phase is also an important consideration, then the same basic equations still apply but you can express the values as complex numbers. The final answer, then, not only will include the magnitude of the gain as computed, but will also reveal the amount of phase shift given to the signal.

The voltage gain calculation for the noninverting circuit shown in Figure 2.27(b) is similar, but will be considered as three separate gains that are multiplied together to find the overall gain. The three individual gains are

1. R_1/C_I network gain (actually a loss)
2. R_L/C_O network gain (actually a loss)
3. The gain of the op amp circuit as determined by R_F and R_I

The gains of the input and output RC circuits are computed in the same way that we computed the gain of the output RC circuit in Figure 2.27(a). Let us first calculate the input RC circuit gain. Our initial step is to compute the reactance of C_I at the lowest frequency (assumed to be 800 hertz).

$$\begin{aligned} X_C &= \frac{1}{2\pi fC} \\ &= \frac{1}{6.28 \times 800\ Hz \times 0.01\ \mu F} \\ &= 19.9\ k\Omega \end{aligned}$$

Next we find the net impedance of R_1 and C_I.

$$\begin{aligned} Z &= \sqrt{R^2 + X_C^2} \\ &= \sqrt{(47\ k\Omega)^2 + (19.9\ k\Omega)^2} \\ &= 51\ k\Omega \end{aligned}$$

Finally we compute the voltage gain (loss) of the RC network with Equation (2.38).

$$A_{V_1} = \frac{R_1}{Z}$$

$$A_{V_1} = \frac{47\ k\Omega}{51\ k\Omega}$$

$$= 0.922$$

Similar calculations for the output RC network of Figure 2.27(b) can now be accomplished. First we find the reactance of C_O.

$$X_C = \frac{1}{2\pi f C}$$

$$= \frac{1}{6.28 \times 800\ Hz \times 0.1\ \mu F}$$

$$= 1.99\ k\Omega$$

Next we compute the net impedance of R_L and C_O.

$$Z = \sqrt{R^2 + X_C^2}$$

$$= \sqrt{(3.3\,k\Omega)^2 + (1.99\,k\Omega)^2}$$

$$= 3.85\,k\Omega$$

Finally, the effective voltage gain (loss) of the $R_L C_O$ network can be computed, Equation (2.38).

$$A_{V_2} = \frac{R_L}{Z}$$

$$= \frac{3.3\ k\Omega}{3.85\ k\Omega}$$

$$= 0.857$$

The third portion of our overall gain calculation is the gain of the op amp circuit as determined by R_F and R_I. We compute this using the gain formula of Equation (2.28) presented for the direct coupled amplifier.

$$A_{V_3} = \frac{R_F}{R_I} + 1$$

$$= \frac{18\ k\Omega}{2\ k\Omega} + 1$$

$$= 10$$

The effective overall gain at 800 hertz is found by multiplying the three individual gains, as in Equation (2.39).

$$\begin{aligned} A_V(overall) &= A_{V_1} \times A_{V_2} \times A_{V_3} \\ &= 0.922 \times 0.857 \times 10 \\ &= 7.9 \end{aligned}$$

As with the AC-coupled inverting amplifier, we have chosen to ignore the frequency-dependent effects of open-loop op amp gain. This is generally a reasonable approach because our calculations are performed at the lowest input frequencies, where the open-loop gain is the closest to its ideal value.

Input Impedance. The input impedance for the AC-coupled inverting amplifier circuit shown in Figure 2.27(a) is equal to the net impedance of R_I and C_I. Recall that the (–) input of the op amp is a virtual ground point. The source, therefore, sees the input impedance offered by C_I and R_I. Because this is a frequency-dependent value, we must discuss input impedance at a particular frequency of interest. For purposes of our present discussion, let us compute the highest and lowest values for input impedance if the input frequency range is 800 hertz to 3 kilohertz. The following input impedance at 800 hertz is computed. First we find the reactance of C_I at 800 hertz.

$$\begin{aligned} X_C &= \frac{1}{2\pi fC} \\ &= \frac{1}{6.28 \times 800\ Hz \times 0.02\ \mu F} \\ &= 9.95\ k\Omega \end{aligned}$$

Now we can compute the impedance of R_I and C_I.

$$\begin{aligned} Z(\text{max}) &= \sqrt{R^2 + X_C^2} \\ &= \sqrt{(27\ k\Omega)^2 + (9.95\ k\Omega)^2} \\ &= 28.8\ k\Omega \end{aligned}$$

The minimum value for input impedance occurs at the highest input frequency. In most cases, the input impedance approaches the value of R_I; however, the computations are similar to those as shown:

$$\begin{aligned} X_C &= \frac{1}{2\pi fC} \\ &= \frac{1}{6.28 \times 3\ kHz \times 0.02\ \mu F} \\ &= 2.65\ k\Omega \end{aligned}$$

Now we can compute the impedance of R_I and C_I.

$$\begin{aligned} Z(\text{min}) &= \sqrt{R^2 + X_C^2} \\ &= \sqrt{(27\ k\Omega)^2 + (2.65\ k\Omega)^2} \\ &= 27.1\ k\Omega \end{aligned}$$

The input impedance for the AC-coupled noninverting amplifier circuit shown in Figure 2.27(b) is essentially equal to the impedance offered by R_1 and C_I. Technically, the input impedance of the (+) input terminal appears in parallel with R_1. We can generally ignore this impedance, however, since it is usually an extremely high value. For our present example, we begin by finding the reactance of C_I at the lowest input frequency.

$$\begin{aligned} X_C &= \frac{1}{2\pi fC} \\ &= \frac{1}{6.28 \times 800\ Hz \times 0.01\ \mu F} \\ &= 19.9\ k\Omega \end{aligned}$$

Next we find the net impedance of R_1 and C_I.

$$\begin{aligned} Z(\text{max}) &= \sqrt{R^2 + X_C^2} \\ &= \sqrt{(47\ k\Omega)^2 + (19.9\ k\Omega)^2} \\ &= 51\ k\Omega \end{aligned}$$

The minimum value for input impedance occurs at the highest input frequency, as it did with the inverting circuit. In most cases, the input impedance approaches the value of R_1. The following computations, however, are shown:

$$\begin{aligned} X_C &= \frac{1}{2\pi fC} \\ &= \frac{1}{6.28 \times 3\ kHz \times 0.01\ \mu F} \\ &= 5.31\ k\Omega \end{aligned}$$

Now we can compute the impedance of R_1 and C_I:

$$\begin{aligned} Z(\text{min}) &= \sqrt{R^2 + X_C^2} \\ &= \sqrt{(47\ k\Omega)^2 + (5.31\ k\Omega)^2} \\ &= 47.3\ k\Omega \end{aligned}$$

Bandwidth. Bandwidth can be defined as that range of frequencies that pass through a circuit with a voltage amplitude of at least 70.7 percent of the maximum output voltage—in other words, the range of frequencies between the two half-power points. These two frequencies can be readily determined in at least three ways:

1. Numerical analyses involving higher mathematics
2. Computer-aided analysis
3. Direct measurements in the lab

You may be able to employ all three of these methods. However, none of them are suitable for use in this reference book, so we will examine yet another, less direct approach. Let us begin by making some observations. First, since the op amp has a frequency response that extends all the way to DC, the lower cutoff frequency will be unaffected by the op amp. That is, the input and output RC circuits will determine the lower cutoff frequency. Second, in a practical circuit, the upper cutoff frequency will be determined by the op amp itself. The RC circuits act as high-pass filters and will not restrict the gain at the higher input frequencies.

Calculation of the upper cutoff frequency was discussed in previous sections. We estimate it with Equation (2.40).

$$\boxed{f_U = \frac{f_{UG} R_I}{R_F + R_I} \qquad (2.40)}$$

In the case of Figure 2.27(a), our ideal upper cutoff frequency is computed as

$$f_U = \frac{1.0\ MHz \times 27\ k\Omega}{68\ k\Omega + 27\ k\Omega} = 284\ kHz$$

Next we calculate the lower cutoff frequency, which is determined by the input and output RC networks. The cutoff frequency of each individual RC network is determined with the following equation:

$$\boxed{f_C = \frac{1}{2\pi RC} \qquad (2.41)}$$

The lower cutoff frequency for the entire circuit is determined by the ratio of the cutoff frequencies for the RC circuits.

Let us now compute the lower cutoff frequency for the circuit in Figure 2.27(a). First we compute the individual cutoff frequencies for the two RC networks. The input circuit calculations, as in Equation (2.41), are

$$\begin{aligned} f_{C_1} &= \frac{1}{2\pi RC} \\ &= \frac{1}{6.28 \times 27\ k\Omega \times 0.02\ \mu F} \\ &= 295\ Hz \end{aligned}$$

A similar computation, Equation (2.41), for the output RC circuit is

$$\begin{aligned} f_{C_2} &= \frac{1}{2\pi RC} \\ &= \frac{1}{6.28 \times 39\ k\Omega \times 0.02\ \mu F} \\ &= 204\ Hz \end{aligned}$$

Computing the ratio of the two cutoff frequencies (using the higher frequency as the numerator) gives us the index needed for the lookup operation in Table 2.5.

$$index = \frac{f_{C_1}}{f_{C_2}} \tag{2.42}$$

For our particular case, the index is computed as

$$index = \frac{295\ Hz}{204\ Hz} = 1.45$$

Finally, we use the lookup table shown in Table 2.5 to get our multiplying factor *k*. In this case, the value of *k* is about 1.32 (estimating the value between 1.34 and 1.306). The overall lower cutoff frequency can now be found by multiplying our factor *k* by the **higher** of the two individual cutoff frequencies.

$$f_L = f_C \times k \tag{2.43}$$

Thus, the lower cutoff frequency for the circuit in Figure 2.27(a) is estimated as

$$f_L = 295\ Hz \times 1.32 = 389\ Hz$$

The approximate bandwidth of the circuit in Figure 2.27(a) can now be expressed as Equation (2.5):

$$\begin{aligned} bw &= f_U - f_L \\ &= 284\ kHz - 389\ Hz \approx 283.6\ kHz \end{aligned}$$

TABLE 2.5

	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
1	1.554	1.485	1.427	1.380	1.340	1.306	1.277	1.252	1.230	1.211
2	1.194	1.790	1.166	1.154	1.143	1.134	1.125	1.117	1.110	1.103
3	1.097	1.092	1.087	1.082	1.078	1.074	1.070	1.066	1.063	1.060
4	1.058	1.055	1.053	1.050	1.048	1.046	1.044	1.042	1.041	1.039
5	1.038	1.036	1.035	1.034	1.033	1.032	1.031	1.030	1.028	
6	1.027	1.026	1.025	1.024		1.023	1.022		1.021	1.020
7	1.020	1.019		1.018		1.017		1.016		
8	1.015			1.014			1.013			1.012
9	1.012			1.011				1.010		
10	1.000	Use $k = 1.0$ for ratios greater than 10								

The bandwidth of the noninverting circuit shown in Figure 2.27(b) is computed in the same way that it was for the inverting circuit. First we estimate the upper cutoff frequency, which is determined by the behavior of the op amp, from Equation (2.22).

$$\begin{aligned} f_U &= \frac{f_{UG} R_I}{R_F + R_I} \\ &= \frac{1.0\ MHz \times 2\ k\Omega}{18\ k\Omega + 2\ k\Omega} \\ &= 100\ kHz \end{aligned}$$

Next we compute the individual cutoff frequencies for the input and output RC circuits, as in Equation (2.41).

$$\begin{aligned} f_{C_1} &= \frac{1}{2\pi RC} \\ &= \frac{1}{6.28 \times 47\ k\Omega \times 0.01\ \mu F} \\ &= 339\ Hz \end{aligned}$$

A similar computation for the output RC circuit is Equation (2.41):

$$\begin{aligned} f_{C_2} &= \frac{1}{2\pi RC} \\ &= \frac{1}{6.28 \times 3.3\ k\Omega \times 0.1\ \mu F} \\ &= 483\ Hz \end{aligned}$$

Computing the ratio of the two cutoff frequencies (using the higher frequency as the numerator) gives us the index, from Equation (2.42), needed for the lookup operation in Table 2.5:

$$index = \frac{f_{C_2}}{f_{C_1}} = \frac{483}{339} = 1.425$$

Using this value as the index into Table 2.5 gives us an approximate value of 1.33 for k. The lower cutoff frequency for the entire circuit in Figure 2.27(b) can now be estimated with Equation (2.43):

$$\begin{aligned} f_L &= f_C \times k \\ f_L &= 483\ Hz \times 1.33 \\ &= 642\ Hz \end{aligned}$$

At this point, the bandwidth of the circuit can be estimated with Equation (2.5):

$$\begin{aligned} bw &= f_U - f_L \\ &= 100\ kHz - 642\ Hz \\ &= 99.36\ kHz \end{aligned}$$

Slew-Rate Limitations. The slew rate of the op amp will limit the upper cutoff frequency for high-amplitude output signals. The slew-rate limiting frequency is calculated in the same manner as described for previous amplifier configurations.

2.7.3 Practical Design Techniques

The design of either the inverting or the noninverting AC-coupled amplifier is a relatively easy process. Following are the sequential steps:

1. Design the basic amplifier circuit according to the guidelines presented for the direct-coupled inverting or noninverting amplifier circuits.
2. Compute the values for the input and output RC coupling components.

As an example, let us design a noninverting AC-coupled amplifier that has the following characteristics:

1. Midpoint voltage gain of 12
2. Lower cutoff frequency of 500 hertz
3. Upper cutoff frequency of at least 15 kilohertz
4. Input impedance of at least 3000 ohms

Determine the Value of R_I. We will select R_I as 6.8 kilohms. Although this selection is somewhat arbitrary, we are keeping within the guidelines of choosing resistance between 1000 ohms and 680 kilohms. Additionally, the selection of R_I

will have a major effect on the final input impedance, as R_1 will be close to the same value as R_I, and it is R_1 that determines the input impedance of the amplifier. Thus, in order to meet the requirements for an input impedance of at least 3000 ohms, we must choose a value for R_I that is larger than 3000 ohms.

Determine the Value of R_F. R_F can be computed from the voltage gain equation shown in Equation (2.28):

$$A_V = \frac{R_F}{R_I} + 1, \; or$$

$$R_F = R_I(A_V - 1)$$

For the present design example, we compute R_F as follows:

$$R_F = 6.8\ k\Omega \times (12 - 1) = 74.8\ k\Omega$$

We select the nearest standard value of 75 kilohms to use as R_F.

Determine the Required Unity Gain Frequency. We can compute the minimum unity gain frequency for our op amp with Equation (2.22):

$$f_{UG} = \frac{bw(R_F + R_I)}{R_I} = \frac{15\ kHz(75\ k\Omega + 6.8\ k\Omega)}{6.8\ k\Omega} = 180\ kHz$$

where f_{UG} is the minimum required unity gain frequency for the op amp and *bw* is the highest operating frequency. Thus, we must select an op amp that has a minimum unity gain frequency of at least 180 kilohertz. Because the 741 has a 1.0-megahertz unity gain frequency, it should be fine for our purposes. Now let us determine the slew-rate requirement.

Determine the Required Slew Rate. The minimum acceptable slew rate for the op amp is given by the following equation, Equation (2.11):

$$slew\ rate(\text{min}) = \pi f_{SRL} v_O(\text{max})$$

In our case, let us assume that we want to deliver a full output swing (±13 V) at the highest frequency (15 kHz). The minimum slew rate is computed as follows:

$$slew\ rate(\text{min}) = 3.14 \times 15\ kHz \times 26\ V = 1.2\ V/\mu s$$

The 741 has a slew rate of 0.5 volts per microsecond, so it will not be adequate for this application. There are many alternatives, but let us choose the MC1741SC op amp (Appendix 4). It has a unity gain frequency similar to that of the 741, but it offers a slew rate of 10 volts per microsecond.

Select R_1. R_1 is chosen to be the same value as the parallel combination of the feedback resistor (R_F) and the input resistor (R_I). This following value is computed:

$$\begin{aligned} R_1 &= \frac{1}{\dfrac{1}{R_I} + \dfrac{1}{R_F}} \\ &= \frac{1}{\dfrac{1}{6.8\ k\Omega} + \dfrac{1}{75\ k\Omega}} \\ &= 6.23\ k\Omega \end{aligned}$$

We will use a standard value of 6.2 kilohms.

Compute the Value of C_I. To simplify subsequent calculations, we will choose a value for C_I that produces a reactance that is much less than the resistance R_1. We will design for a reactance of one-tenth R_1, or 620 ohms in this case, at the lower cutoff frequency. The value for C_I is computed from the capacitive reactance equation.

$$\begin{aligned} X_C &= \frac{1}{2\pi f C}, \textit{ or} \\ C &= \frac{1}{6.28 f X_C} \end{aligned}$$

In our present case,

$$C_I = \frac{1}{6.28 \times 500\ Hz \times 620\ \Omega} = 0.514\ \mu F$$

We will select the next higher standard value of 0.56 microfarad.

Select the Value of R_L. In many cases, R_L is the input resistance of a subsequent stage. In these cases, R_L is not selected; it is already defined by the nature of the problem. For our example design, we will choose R_L as 27 kilohms. This is sufficiently large to eliminate any concerns of output loading on the op amp, but it is low enough to facilitate coupling to a subsequent op amp circuit if needed.

Compute the Value of C_O. By following the guidelines given for the selection of the R_1C_I combination, we have assured ourselves that the lower cutoff frequency will be primarily determined by the R_LC_O network. We use the fundamental formula for capacitive reactance to compute a value for C_O that produces a reactance equal to the value of R_L at the lower cutoff frequency (500 Hz).

$$\begin{aligned} C_O &= \frac{1}{2\pi f X_C} \\ &= \frac{1}{6.28 \times 500\ Hz \times 27\ k\Omega} \\ &= 0.012\ \mu F \end{aligned}$$

The resulting circuit for our noninverting AC-coupled amplifier is shown in Figure 2.28. The actual performance of the circuit is reflected in the oscilloscope waveforms shown in Figure 2.29. The design goals are compared to the measured performance in Table 2.6.

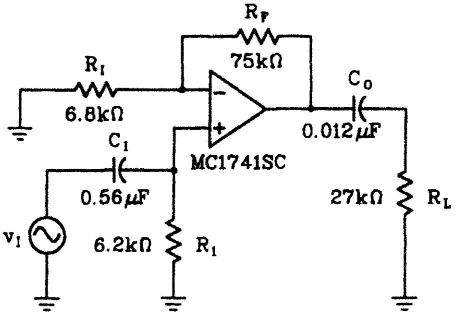
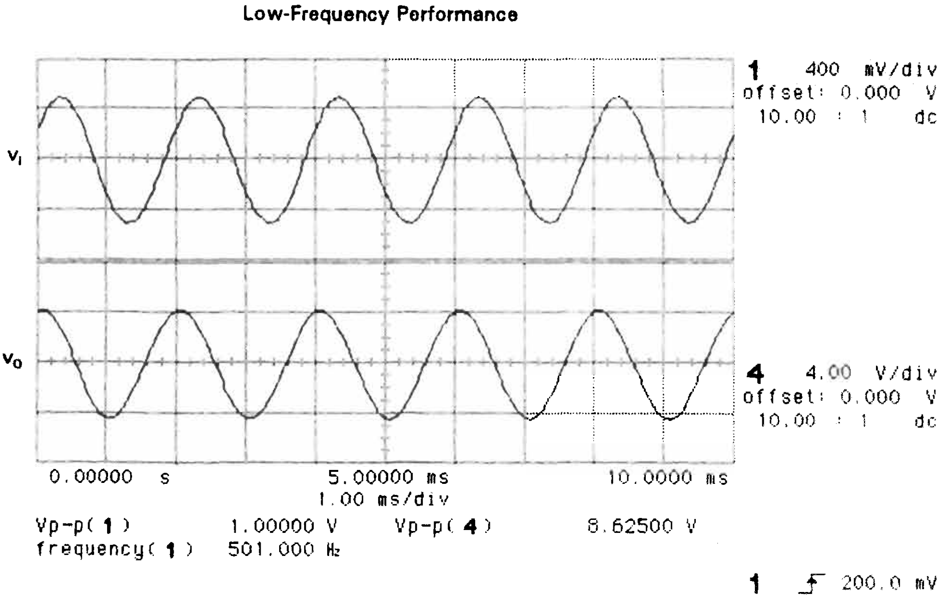


FIGURE 2.28 A noninverting AC-coupled amplifier design.

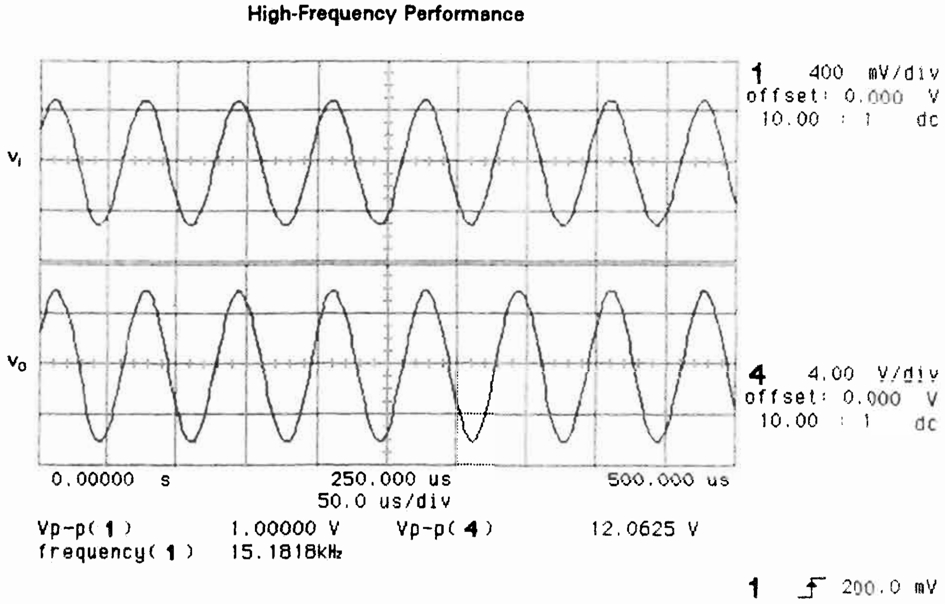
TABLE 2.6

Parameter	*Design Goal*	*Measured Values*
Midpoint voltage gain	12	11.9
Frequency range	500 Hz–15 kHz	475 Hz–79.5 kHz



(a)

FIGURE 2.29 Oscilloscope displays showing the actual performance of the AC-coupled amplifier shown in Figure 2.28. (Test equipment courtesy of Hewlett-Packard Company.)



High-Frequency Performance

(b)

FIGURE 2.29 *Continued*

2.8 CURRENT AMPLIFIER

2.8.1 Operation

Figure 2.30 shows the schematic diagram of a basic current amplifier. This circuit, as its name implies, accepts a current source as its input and delivers an amplified version of that current to the load. The load, in the case of Figure 2.30, is not directly referenced to ground. A current source is normally designed to drive into a very low (ideally 0) impedance. In the case of the circuit in Figure 2.30, the (–) input of the op amp is a virtual ground point. Thus, the current source sees a very low input resistance.

All of the current that leaves the source must flow through resistor R_2, since we know that no current flows in or out of the op amp input (except for bias current). The current flowing through R_2 produces a voltage drop that is determined by the value of R_2 (a constant) and the value of the input current. Once the circuit has been designed, the voltage drop across R_2 is strictly determined by the amount of input current (i_I). Notice that resistors R_2 and R_1 are essentially in parallel, because R_2 is connected to a virtual ground point. Because the two resistors are in parallel, we know that the voltage across them must be the same. That is, the voltage across R_1 will be the same as the voltage across R_2 and is determined by the value of input current. The current through R_1 can be determined by Ohm's Law. If the value of R_1 is smaller than the value of R_2 (the normal case), then current i_1 will be proportionally larger than i_I (recalling that the voltages across the parallel resistors are equal).

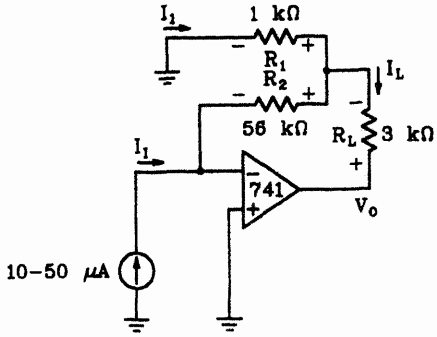


FIGURE 2.30 A basic current amplifier circuit.

Kirchhoff's Current Law would show us that the current i_I and i_1 must combine to produce the load current i_L. The value of i_L is strictly determined by the input current, but its value will be larger by the amount of current (i_1) flowing through R_1. Thus, we have current gain or current amplification. The larger we make i_1 as compared to i_I, the higher the current amplification. Examination of the circuit will confirm that the circuit can accept current of either polarity as long as the op amp is operating from a dual power supply.

2.8.2 Numerical Analysis

Now analyze the current amplifier shown in Figure 2.30, and compute the following values:

1. Current gain
2. Load current
3. Range of acceptable input currents
4. Maximum load resistance
5. Input resistance
6. Output resistance

Current Gain. The current gain (A_I) can be initially described with the basic gain equation, Equation (2.1):

$$A_I = \frac{output\ current}{input\ current} = \frac{i_L}{i_I}$$

Current i_L is composed of the two currents, i_1 and i_I. That is,

$$i_L = i_1 + i_I$$

The voltage across R_1 is equal to the voltage across R_2 and is computed by Ohm's Law as

$$v_1 = v_2 = i_I R_2$$

The value of current (i_1) can also be computed by Ohm's Law as

$$i_1 = \frac{v_1}{R_1} = \frac{i_I R_2}{R_1}$$

Substituting this into the equation for load current produces

$$i_L = i_1 + i_I$$
$$i_L = \frac{i_I R_2}{R_1} + i_I$$

Factoring i_I gives us the equation for I_L:

$$\boxed{i_L = i_I\left(\frac{R_2}{R_1} + 1\right)} \qquad (2.44)$$

In this form, it is easy to see that we do indeed have a current amplifier. That is, the input current (i_I) is multiplied by a constant ($R_2/R_1 + 1$) to produce the output or load current. The constant is the current gain of the circuit, shown below.

$$\boxed{\textit{current gain} = A_I = \frac{R_2}{R_1} + 1} \qquad (2.45)$$

In the case of the circuit in Figure 2.30, the current gain is calculated as shown:

$$A_I = \frac{56\ k\Omega}{1\ k\Omega} + 1 = 57$$

It is especially important to note that the value of load current is independent of the value of load resistor. That is, the op amp circuit is acting as a current source.

Although many current sources are essentially DC (e.g., transducers), there may be an application requiring current amplification at higher frequencies. As the frequency of operation is increased, the actual current gain will begin to decrease from the low frequency value calculated. This effect is caused by the reduction in open-loop op amp gain as the input frequency is increased. The higher the value of current gain (A_I), the more significant the effects of op amp voltage gain variations.

Load Current. The input current (i_I) for the circuit in Figure 2.30 is indicated to be in the range of 10–50 microamps. The output current can be found by transposing the basic current gain equation, Equation (2.1).

$$A_I = \frac{i_O}{i_I}, \text{ or}$$

$$i_O = i_I A_I$$

In our case, the minimum load current is computed as

$$\begin{aligned} i_L(\text{min}) &= i_I(\text{min}) \times A_I \\ &= 10\ \mu A \times 57 \\ &= 570\ \mu A \end{aligned}$$

The highest load current is found in a similar manner as

$$\begin{aligned} i_L(\text{max}) &= i_I(\text{max}) \times A_I \\ &= 50\ \mu A \times 57 \\ &= 2.85\ mA \end{aligned}$$

Range of Acceptable Input Currents. In order for the circuit in Figure 2.30 to operate as a current source whose value is proportional to input current, it is essential that the output voltage (v_O) be less than the saturation voltage in either polarity. This, then, is the factor that restricts the range of acceptable input currents. The output voltage can be expressed as a sum of two voltages by using Kirchhoff's Voltage Law.

$$v_O = v_{R_2} + v_{R_L}$$

Substituting current and resistance values (i.e., $V = IR$) produces

$$\begin{aligned} v_O &= i_I R_2 + i_I\left(\frac{R_2}{R_1} + 1\right)R_L \\ &= i_I\left(R_2 + \frac{R_2 R_L}{R_1} + R_L\right) \end{aligned}$$

To calculate the amount of input current needed to drive the output to saturation, we transpose this equation to find i_I and substitute the value of V_{SAT} for v_O. For our example, let us assume that the saturation voltage is determined from the manufacturer's data sheet to be 13 volts. The maximum input current, then, is computed as

$$\boxed{i_I(\text{max}) = \frac{R_1 V_{SAT}}{R_1(R_2 + R_L) + R_2 R_L} \qquad (2.46)}$$

More specifically, for our present circuit we have

$$
\begin{aligned}
i_I(\text{max}) &= \frac{1\ k\Omega \times 13\ V}{1\ k\Omega(56\ k\Omega + 3\ k\Omega) + (56\ k\Omega \times 3\ k\Omega)} \\
&= 57.3\ \mu A
\end{aligned}
$$

The lower range is computed in a similar manner by using the other saturation limit. In most cases (i.e., balanced dual power supply circuits), the values of $\pm V_{SAT}$ will be the same. If this were true for the circuit in Figure 2.30, we could have a range of input currents that extended from –57.3 microamps to +57.3 microamps—the polarity, of course, telling us the direction of current flow.

Maximum Load Resistance. Another way to view the preceding calculations is to consider a known range of input currents and a variable value for R_L. Again, the output voltage must be kept from reaching the saturation limits. We can transpose Equation (2.46) for i_I(maximum) to get the following result:

$$
R_L(\text{max}) = \frac{V_{SAT}}{A_I i_I} - \frac{R_2}{A_I}
$$

where i_I is the highest expected input current. In the case of Figure 2.30, we can determine the maximum value for the load resistance as

$$
R_L(\text{max}) = \frac{13\ V}{57 \times 50\ \mu A} - \frac{56\ k\Omega}{57} = 3.58\ k\Omega
$$

Input Resistance. Although the input resistance of the circuit in Figure 2.30 is ideally 0, there may be applications that require us to know a more accurate value for it. The following equation can be used to estimate the input resistance of the current amplifier in Figure 2.30:

$$
\boxed{R_{IN} = \frac{R_2(R_X + R_L)}{R_X(1 + A_V) + R_L} \qquad (2.47)}
$$

where R_X is the resistance of R_1 and R_2 in parallel (i.e., $R_1R_2/(R_1 + R_2)$) and A_V is the open-loop gain of the op amp at a particular frequency.

In the case of Figure 2.30, let us compute the input resistance for DC conditions. First, the open-loop gain at DC can be found in the data sheet (Appendix 1) to be at least 50,000. The value for R_X is calculated as

$$
\begin{aligned}
R_X &= \frac{R_1R_2}{R_1 + R_2} \\
&= \frac{1.0\ k\Omega \times 56\ k\Omega}{1.0\ k\Omega + 56\ k\Omega} \\
&= 982\ \Omega
\end{aligned}
$$

The input resistance can now be calculated, Equation (2.47), as shown:

$$\begin{aligned} R_{IN} &= \frac{R_2(R_X + R_L)}{R_X(1 + A_V) + R_L} \\ &= \frac{56\ k\Omega(982\ \Omega + 3\ k\Omega)}{982\ \Omega(1 + 50{,}000) + 3\ k\Omega} \\ &= 4.54\ \Omega \end{aligned}$$

As you might expect, the input resistance approaches the ideal value (to be driven by a current source) of 0 ohms.

If the input frequency is higher than DC, the input resistance will deviate more from the ideal value of 0. For example, if our input frequency were raised to 1 kilohertz, the input resistance would increase to about 226 ohms. Additionally, we would need to consider the effects of bandwidth and slew rate limitations.

Output Resistance. The output resistance of the circuit in Figure 2.30 as viewed by the load resistor is ideally infinite, as the circuit acts like a current source. A more accurate value for the output resistance can be computed with the following equation:

$$R_O = A_V R_X \tag{2.48}$$

where A_V is the open-loop voltage gain of the op amp at a particular frequency and R_X is the value of R_1 and R_2 in parallel. In the case of Figure 2.30, let us estimate the output resistance at DC:

$$R_O = 50{,}000 \times 982\ \Omega = 49.1\ M\Omega$$

As evidenced in the equation, this value becomes less ideal as the frequency of operation is increased.

2.8.3 Practical Design Techniques

A practical current amplifier circuit can be designed by applying the equations discussed in the preceding paragraphs. Depending on the application, you will know some combination of the following parameters:

1. Input current range
2. Output current range
3. Current gain
4. Load resistance

For purposes of a design example, let us build a current amplifier that satisfies the following requirements:

1. Output current of 10 milliamps (constant)
2. Input current of 500 microamps
3. Load resistance of < 500 ohms
4. Available power supply of ±15 volts
5. 741 op amp used if practical

Compute the Required Current Gain. The required current gain of our circuit can be computed with the basic current gain equation, Equation (2.1):

$$\begin{aligned} A_I &= \frac{i_O}{i_I} \\ &= \frac{10\ mA}{500\ \mu A} \\ &= 20 \end{aligned}$$

Determine the Maximum Value for R_2. The maximum value for R_2 can be found by applying a transposed version of the equation we used for computing the maximum value for R_L:

$$\begin{aligned} R_L(\text{max}) &= \frac{V_{SAT}}{A_I i_I} - \frac{R_2}{A_I},\ or \\ R_2(\text{max}) &= \frac{V_{SAT}}{i_I} - A_I R_L(\text{max}) \\ &= \frac{12\ V}{500\ \mu A} - (20 \times 500\ \Omega) \\ &= 14\ k\Omega \end{aligned}$$

We will select a standard value less than this—for purposes of our design, a 12-kilohm resistor for R_2. Notice that we use the worst-case value of 12 volts as the saturation voltage for the op amp.

Compute the Value of R_1. R_1 can be computed by applying a transposed version of the current gain equation, Equation (2.45).

$$\begin{aligned} A_I &= \frac{R_2}{R_1} + 1,\ or \\ R_1 &= \frac{R_2}{(A_I - 1)} \\ &= \frac{12\ k\Omega}{20 - 1} \\ &= 632\ \Omega \end{aligned}$$

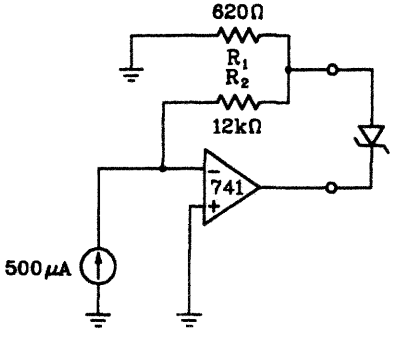


FIGURE 2.31 A current amplifier design being used to deliver a constant current to a zener load.

We will select the nearest standard value of 620 ohms. If it is essential to have a precise value of load current, then we put a variable resistance in series with R_2.

The schematic of our completed design is shown in Figure 2.31. The load resistor has been replaced with a zener diode to illustrate a possible application. By forcing the zener current to be a known value, we can measure the zener voltage and compute the zener resistance. As long as the effective zener resistance is below our established limit for R_L, the circuit will work fine. The measured performance of the circuit is contrasted with the design goals in Table 2.7.

TABLE 2.7

Parameter	*Design Goal*	*Measured Values*
Input current	500 *μA*	500 *μA*
Output current	10 *mA*	9.97 *mA*
Current gain	20	19.9

2.9 HIGH-CURRENT AMPLIFIER

2.9.1 Operation

A general-purpose op amp can supply only a few milliamps to a load. The 741, for instance, has a short-circuit output current of 20 milliamps. Some applications require substantially higher currents. The circuit in Figure 2.32 illustrates one common method for increasing the available current at the output of an op amp circuit. This technique is illustrated for a simple inverting amplifier, but is applicable to most voltage amplifier circuits.

The bulk of the circuit operation is identical to that discussed with reference to the basic inverting amplifier circuit and will not be repeated here. Recall that resistors R_F and R_I determine the voltage gain of the circuit. Resistor R_B is to compensate for op amp bias currents. Potentiometer R_P has been added to the basic inverting amplifier and will be used to force an offset in the output.

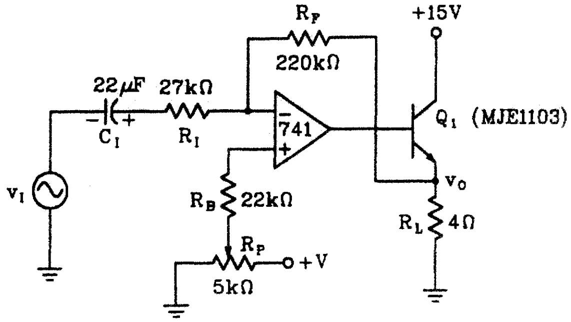


FIGURE 2.32 An inverting voltage amplifier with additional current amplification.

The output voltage of the op amp appears on the base of Q_1. A similar voltage appears on the emitter of Q_1, which is connected as a voltage follower. The actual voltage on the emitter is less than the base voltage by a small amount ($\approx$0.7 volts). In general, the output voltage across R_L is essentially the same as the output voltage of the op amp. The output current of the op amp provides base current to the transistor. The load current, on the other hand, is provided by the transistor's emitter current. You will recall that the transistor emitter current and the base current are related by a current gain factor called β or h_{FE}, which can range from about twenty up to several thousand. With the circuit connected as shown, the load can draw β times as much current as the basic op amp supplies.

In order for the circuit to operate properly, the base voltage on Q_1 must always be positive with reference to ground, since the load is returned to ground. Ordinarily, an AC signal applied to a split-supply op amp would produce bipolar signals on its output. To prevent this situation, we adjust R_P to establish a positive bias on the base of Q_1 that is approximately equal to half of the positive saturation voltage. The output signal can then swing from near 0 up to near saturation. Recognize that this swing is only half of the swing available with previous amplifiers and represents a disadvantage of the circuit shown in Figure 2.32. An alternative is to return the load to the negative 15-volt supply (emitter bias).

One very important characteristic of the circuit in Figure 2.32 is that output voltage is unaffected by changes in V_{BE}. We know V_{BE} is approximately 0.7 volts for silicon transistors, but we also know it changes with temperature and varies from one transistor to another. By connecting the feedback resistor (R_F) to the emitter rather than directly to the output of the op amp, we include the base-emitter junction in the feedback circuit. Changes in the base-emitter voltage are now effectively compensated by the op amp.

Since the (+) input on the op amp is at some positive level, the (−) pin will also be at a similar level. If the input signal were centered on 0 volts, this could cause an undesired DC offset in the output. Capacitor C_I is included to isolate the DC level on the (−) pin from the DC level associated with the signal source. If it is sufficiently large, it has no effect on the gain calculations in the circuit. If its reactance at the lowest input frequency exceeds one-tenth the resistance of R_I, then the gain of the circuit should be computed in the same manner as the AC-coupled amplifiers discussed in a previous section.

2.9.2 Numerical Analysis

Let us now numerically analyze the behavior of the circuit shown in Figure 2.32. Appendix 1 shows the data sheet for the 741 op amp, and Appendix 2 shows the specifications for an MJE1103 transistor. First, we know from our basic transistor theory that the impedance looking into the base will be approximately equal to β times the resistance in the emitter circuit. Thus, the op amp sees the load resistance as

$$R_L' = \beta R_L \tag{2.49}$$

In the case of Figure 2.32, the emitter resistance appears as

$$R_l' = 750 \times 4\ \Omega = 3000\ \Omega$$

We can now refer to the 741 data sheet and determine the worst-case saturation voltage when using a ±15-volt supply and driving a 3000-ohm load. This value is listed as 10 volts.

The transistor data sheet indicates that the base-emitter voltage drop is 2.5 volts or less. Thus, the highest (worst-case) voltage that we can expect at the load is

$$v_O(peak) = V_{SAT} - V_{BE} \tag{2.50}$$

For the circuit in Figure 2.32, we have

$$v_O(peak) = 10\ V - 2.5\ V = 7.5\ V$$

The unusually high value of V_{BE} stems from the fact that the MJE1103 is a high-current Darlington pair. With Ohm's Law, we can calculate the maximum instantaneous (i.e., peak) load current as

$$\begin{aligned} i_L(peak) &= \frac{v_O(peak)}{R_L} \\ &= \frac{7.5\ V}{4\ \Omega} \\ &= 1.88\ A \end{aligned}$$

The op amp must supply a current that is smaller than load current by a factor of β. That is,

$$i_O(op\ amp) = \frac{i_L}{\beta} \tag{2.51}$$

In our case, the calculations are

$$i_O(op\ amp) = \frac{1.88\ A}{750} = 2.51\ mA$$

This current is well within the range of op amp output currents, even though the load current itself is nearly two amps.

In order to ensure that we have a maximum symmetrical swing for the output signal, we will establish a positive DC offset in the output. The value of this offset should be midway between the two extremes. One extreme is the value of V_{SAT}, or +10 volts. The other extreme is the minimum turn-on voltage for Q_1 and is 2.5 volts. The DC level on the output of the op amp must then be

$$\boxed{V_{BIAS}(output) = \frac{V_{SAT} + V_{BE}}{2} \qquad (2.52)}$$

In the present case, we have

$$V_{BIAS}(output) = \frac{10\ V + 2.5\ V}{2} = 6.25\ V$$

The maximum voltage swing at the output of the op amp will be

$$\begin{aligned} v_O(op\ amp) &= V_{SAT} - V_{BE} \\ &= 10\ V - 2.5\ V \\ &= 7.5\ V\ peak\text{-}to\text{-}peak \end{aligned}$$

We will get this same swing at the load, but the DC level will be reduced by the amount of V_{BE}.

If the output of the op amp is allowed to go more positive than $+V_{SAT}$ (estimated here as +10 volts), the waveform will be clipped on its positive peaks. This clipped waveform will also appear across the load.

If the output of the op amp is allowed to go below the minimum turn-on voltage for Q_1 (estimated here as +2.5 volts), the waveform will be clipped on its negative peaks. The load voltage will also have a clipped waveform.

If the amplitude of the input signal remains fixed, but the DC offset voltage in the output of the op amp is changed, then similar waveform clipping can occur. That is, if the instantaneous value of the combined AC and DC voltages on the output of the op amp goes more positive than $+V_{SAT}$ or less positive than the turn-on voltage for Q_1, the output waveform will be distorted.

The sketch in Figure 2.33 clarifies the relationships between the output waveforms (op amp and load), the bias level, and the clipping levels.

In order to establish the 6.25-volt DC bias at the output of the op amp, we need to adjust potentiometer R_P to the necessary level. Although this would have

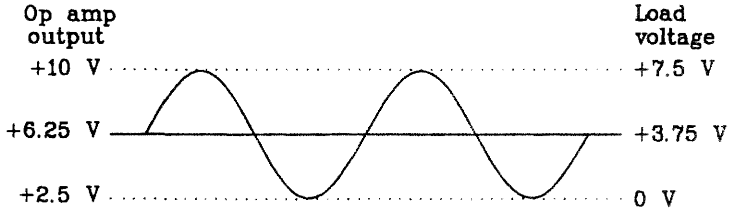


FIGURE 2.33 The bias level affects the clipping levels on the output of the op amp.

to be done in a lab environment, we can compute the required value of voltage at the (+) input of the op amp. Since capacitor C_I acts as an open to DC, the op amp is essentially configured as a voltage follower with reference to the DC offset voltage at potentiometer R_P. Therefore, to obtain a 6.25-volt offset in the output, we will need a 6.25-volt offset on the noninverting (+) input of the op amp.

We have already determined that the maximum output voltage swing is 7.5-volts peak-to-peak. We can determine the maximum input swing before distortion by applying the voltage gain formula, Equation (2.6), for an inverting amplifier.

$$\begin{aligned} A_V &= -\frac{R_F}{R_I} \\ &= -\frac{220\ k\Omega}{27\ k\Omega} \\ &= -8.15 \end{aligned}$$

This can now be used with the basic voltage gain equation, Equation (2.1), to compute the maximum allowable input swing.

$$\begin{aligned} A_V &= \frac{v_O}{v_I},\ or \\ v_I(\max) &= \frac{v_O(\max)}{A_V} \\ &= \frac{7.5\ V}{8.15} \\ &= 0.92\ V\ peak\text{-}to\text{-}peak \end{aligned}$$

This can be more conveniently discussed as an RMS value, so we will convert it using our basic electronics conversion factor:

$$v_I(RMS) = 0.707\left(\frac{peak\text{-}to\text{-}peak}{2}\right)$$

$$= 0.707\left(\frac{0.92\ V}{2}\right)$$
$$= 0.325\ V\ RMS$$

If we drive the amplifier with a signal greater than 0.325 volts RMS, we can expect clipping to occur in the output.

The input impedance of the circuit is approximately equal to the value of R_I. We can apply Ohm's Law to compute the current supplied by the AC input source under maximum input voltage conditions.

$$\begin{aligned} i_I(peak) &= \frac{v_I(peak)}{R_{IN}} \\ &= \frac{0.46\ V}{27\ k\Omega} \\ &= 17\ \mu A \end{aligned}$$

The usefulness of the circuit should become very apparent after this last calculation. A signal source delivering a peak current of 17 microamps is driving a load resistance that requires 1.88 amps peak current.

2.9.3 Practical Design Techniques

Much of the design procedure was covered in our numerical analysis discussion in the preceding section. Let us now design a high-current amplifier that will perform according to the following:

1. Input voltage of 1.0 volt RMS
2. Input resistance > 10 kilohms
3. Input frequency range between 10 hertz and 2.0 kilohertz
4. Load resistance of 50 ohms
5. ±15-volt supplies to be used
6. 741 op amp to be used if practical

Select the Output Transistor. There are basically five transistor parameters that must be reviewed to select a transistor:

1. Forward current transfer ratio (h_{FE}) or current gain (β)
2. Base-emitter voltage drop (V_{BE})
3. Emitter-collector breakdown voltage
4. Maximum collector current
5. Power dissipation

In some cases, the frequency characteristics of the transistor must be evaluated, but in most cases the transistor performance exceeds that of the op amp and can be ignored.

In our case, we need an emitter-collector breakdown voltage greater than 15 volts. The exact collector current will be computed later, but we need to estimate a worst-case value so that we can select the transistor. For this purpose, we can assume that the entire +15 volts of the supply are felt across the 50-ohm load. Ohm's Law tells us the value of load current.

$$\begin{aligned} i_L(estimate) &= \frac{V_{CC}}{R_L} \\ &= \frac{15\ V}{50\ \Omega} \\ &= 300\ mA \end{aligned}$$

The actual collector current will be less than this, but this is a good value to use for initial transistor selection.

Now we need to determine the required current gain (β) of the transistor. In data sheets, this is generally labeled as h_{FE}. We can again make a rough estimate for purposes of transistor selection. If we divide the load current computed above by half of the short-circuit output current of the op amp, we will have a good place to start. The following computation gives us the minimum value of β that our transistor should have.

$$\beta(\min) = \frac{i_L(estimate)}{0.5 I_{SC}} \tag{2.53}$$

The short-circuit current for a 741 is listed as 20 milliamps, and so in the present case we have

$$\beta(\min) = \frac{300\ mA}{0.5 \times 20\ mA} = 30$$

The power dissipation of the transistor can be estimated with the following equation:

$$P_D(estimate) = \frac{V_{CC}^2}{4R_L} \tag{2.54}$$

where V_{CC} is the positive supply voltage. For the present case, the estimated power dissipation of the transistor is

$$\begin{aligned} P_D(estimate) &= \frac{V_{CC}^2}{4R_L} \\ &= \frac{(15\ V)^2}{4 \times 50\ \Omega} \\ &= 1.125\ W \end{aligned}$$

By scanning a transistor data book (selector guides in particular), a transistor that satisfies the above requirements can be found. For illustration purposes, let us select a 2N3440 transistor. The data sheet for this common device is presented as Appendix 9. Its critical parameters follow:

1. β or h_{FE}	160
2. Base-emitter voltage drop (V_{BE})	1.3 volts (maximum)
3. Emitter-collector breakdown voltage	250 volts (minimum)
4. Maximum collector current	1.0 amps
5. Power dissipation	10 watts
6. Thermal resistance, junction to case (θ_{JC})	17.5°C/W
7. Thermal resistance, junction to air (θ_{JA})	175°C/W
8. Maximum junction temperature	200°C

These values exceed our rough, worst-case requirements. Now let us extend our estimate to include the determination of a heat sink (see Appendix 10 for a more complete discussion). We will assume that 50°C will be the highest expected ambient temperature. The required thermal resistance (θ_{JA}) can be estimated as follows:

$$\begin{aligned}\theta_{JA}(req'd) &= \frac{T_J(\max) - T_A}{P_D} \\ &= \frac{200° - 50°}{1.125\ W} \\ &= 133.33°C/W\end{aligned}$$

Since the required value of θ_{JA} is greater than the transistor's θ_{JC}, this transistor can be used for this application. However, since the required value of thermal resistance (θ_{JA}) is less than the θ_{JA} for the transistor, a heat sink will be needed to ensure safe operation. The required thermal resistance (θ_{SA}) of the heat sink can be estimated as follows:

$$\begin{aligned}\theta_{SA} &= \theta_{JA}(req'd) - \theta_{JC} - \theta_{CS} \\ &= 133.33°C/W - 17.5°C/W - 2°C/W \\ &= 113.8°C/W\end{aligned}$$

Note that the case-to-sink thermal resistance (θ_{CS}) was estimated as 2°C/W. Since the required thermal resistance is only slightly lower than the transistor's own thermal rating, it should be easy to find or make a satisfactory heat sink. There are many transistor/heat sink combinations that are adequate for a given application. Final selection must include cost and availability considerations.

Determine the Maximum Output Voltage of the Op Amp. The maximum op amp output voltage is simply V_{SAT}. Appendix 1 lists the data sheet for a 741. The worst-case saturation voltage is listed as 10 volts for resistive loads of 2 to 10 kilohms. If the load on the op amp is over 10 kilohms, the saturation voltage is listed as 12 volts minimum. The load as seen by our op amp is computed by applying a basic transistor equation, Equation (2.49).

$$
\begin{aligned}
R_L' &= \beta R_L \\
&= 160 \times 50\ \Omega \\
&= 8.0\ k\Omega
\end{aligned}
$$

Thus, the maximum available voltage at the output of the op amp will be considered to be 10 volts. In practice, it will likely be higher.

Determine the Minimum Output Voltage of the Op Amp. The lower limit on op amp output voltage is determined by the V_{BE} value of the transistor. The worst-case value for the 2N3440A is given as 1.3 volts. Thus, our op amp output voltage can swing as low as 1.3 volts without fear of clipping.

Determine the Required Bias Voltage at the Output. The output of the op amp should be biased halfway between its two limits (V_{SAT} and V_{BE}). This is computed as shown using Equation (2.52):

$$
\begin{aligned}
V_{BIAS}(output) &= \frac{V_{SAT} + V_{BE}}{2} \\
&= \frac{10\ V + 1.3\ V}{2} \\
&= 5.65\ V
\end{aligned}
$$

Determine the Maximum AC Swing at the Output. The output of the op amp is centered at the bias level and can swing between V_{SAT} and V_{BE}. The RMS value of output voltage is computed as

$$
v_O(RMS) = 0.707\left(\frac{V_{SAT} - V_{BE}}{2}\right) \tag{2.55}
$$

For the present circuit, we have

$$
v_O(RMS) = 0.707\left(\frac{10\ V - 1.3\ V}{2}\right) = 3.08\ V
$$

Compute the Required Voltage Gain. The required voltage gain of the amplifier circuit is determined by applying the basic voltage gain equation, Equation (2.1).

$$
A_V = \frac{v_O}{v_I}
$$

$$= -\frac{3.08\ V}{1.0\ V}$$
$$= -3.08$$

Note that the negative value simply indicates an inversion.

Determine the Value of R_I. The value of the input resistor is chosen to establish the required input resistance of the circuit. In our case, anything greater than 10 kilohms should suffice. Let us choose a standard value of 18 kilohms.

Calculate the Value of R_F. R_F is calculated with the inverting amplifier gain equation, Equation (2.6).

$$\begin{aligned} A_V &= -\frac{R_F}{R_I},\ or \\ R_F &= -A_V R_I \\ &= -(-3.08 \times 18\ k\Omega) \\ &= 55.4\ k\Omega \end{aligned}$$

We will select a standard value of 56 kilohms.

Determine the Required Unity Gain Frequency. The required unity gain frequency is computed in a manner similar to that in previous discussions, using Equation (2.22).

$$\begin{aligned} f_{UG} &= \frac{bw(R_F + R_I)}{R_I} \\ &= \frac{2\ kHz(56\ k\Omega + 18\ k\Omega)}{18\ k\Omega} \approx 8.2\ kHz \end{aligned}$$

Select a Value for R_P. The value of the potentiometer R_P is essentially arbitrary. As it is made smaller, its power rating requirement becomes higher, and the current draw from the supply becomes greater. If R_P is made excessively large, then the effects of bias currents that flow through R_P are more pronounced. As a guideline, select R_P to be approximately equal to $R_F/10$, but consider 1.0 kilohm to be the minimum practical value. In our case, we have

$$\begin{aligned} R_P &= \frac{R_F}{10} \\ &= \frac{56\ k\Omega}{10} \\ &= 5.6\ k\Omega \end{aligned}$$

Compute the Value of R_B. The optimum value for R_B varies as the wiper arm of R_P is moved. However, the preceding method for selecting R_P reduces this dependency. We will compute the value of R_B needed when the wiper arm of R_P is at midpoint. R_B is computed as shown.

$$R_B = R_F - \frac{R_P}{2} \tag{2.56}$$

In our case, we compute R_B as

$$R_B = 56\ k\Omega - \frac{5.6\ k\Omega}{2} = 53.2\ k\Omega$$

We will choose a standard value of 51 kΩ.

Compute the Value of C_I. The purpose of the input coupling capacitor is to isolate the DC levels between the signal source and the (–) pin on the op amp. It should be selected to have a reactance of less than one-tenth of R_I at the lowest input frequency (10 hertz in this case). The calculations are

$$\begin{aligned} C_I &= \frac{1}{2\pi f X_C} \\ &= \frac{1}{6.28 \times 10\ Hz \times 1.8\ k\Omega} \\ &= 8.85\ \mu F \end{aligned}$$

We will choose a standard value of 10 microfarad.

Bandwidth and Slew Rate Considerations. Since our application requires only modest performance, neither slew rate nor bandwidth limitations should pose problems. If the application were more demanding, these restrictions would have to be considered. The methods described for previous amplifier circuits can be utilized to evaluate the effects of bandwidth and slew rate limitations.

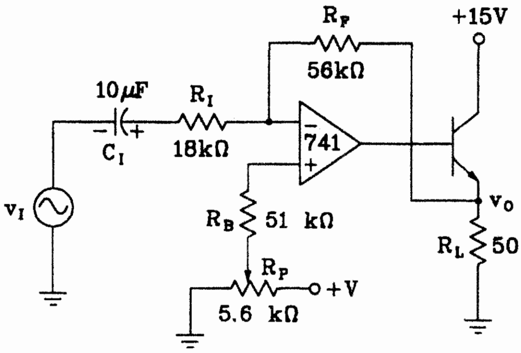
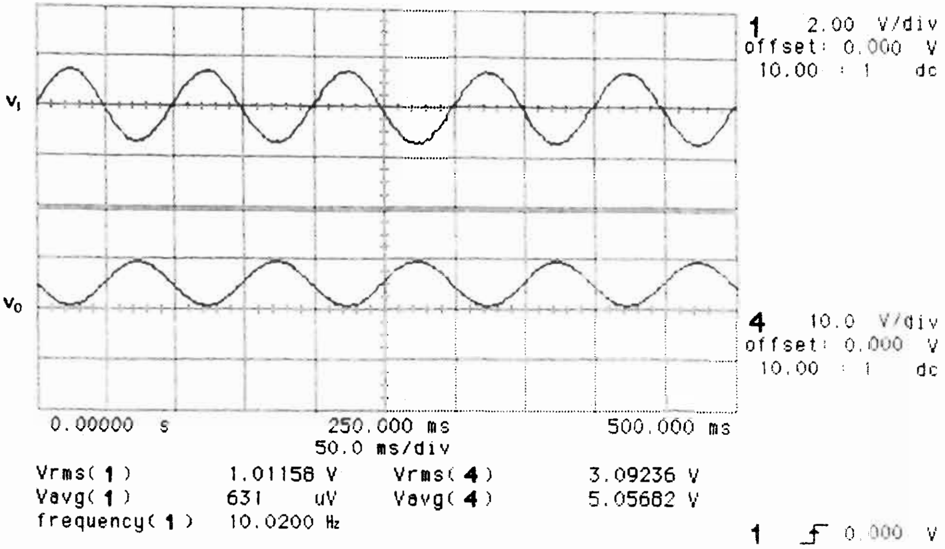


FIGURE 2.34 A high-current amplifier design.

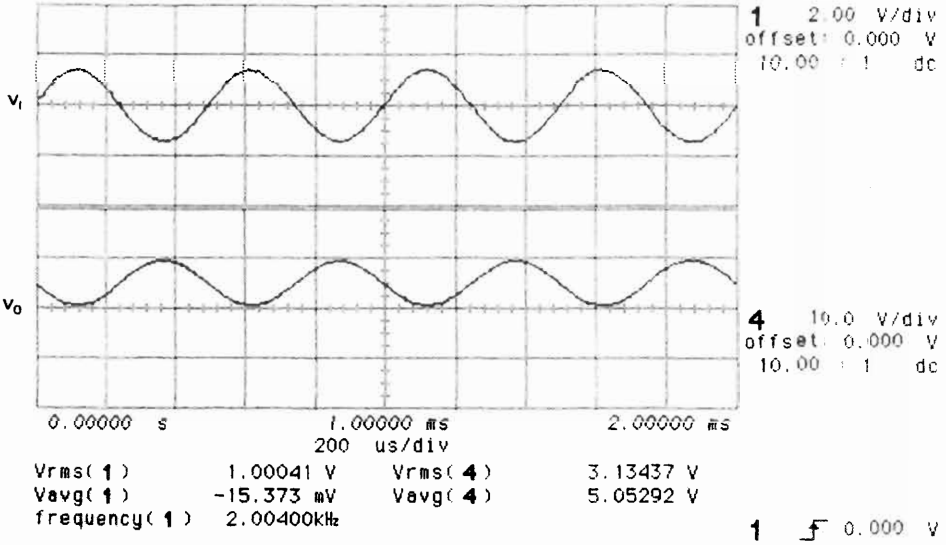
The schematic of our completed design is shown in Figure 2.34. Actual performance of the circuit is indicated by the oscilloscope display shown in Figure 2.35.

Low-Frequency Performance



(a)

High-Frequency Performance



(b)

FIGURE 2.35 Oscilloscope displays showing the actual performance of the high-current amplifier shown in Figure 2.34. (Test equipment courtesy of Hewlett-Packard Company.)

2.10 TROUBLESHOOTING TIPS FOR AMPLIFIER CIRCUITS

In order for an amplifier to operate properly, it must be biased in its linear range of operation. That is, the output must be between the two saturation limits with no signal applied. Many, if not most, of the problems encountered when troubleshooting op amps configured as linear amplifiers result in the output being driven to one of the saturation limits. Your task, then, is to recognize the symptoms and to locate the defective component.

If the amplifier circuit is properly designed (i.e., capable of achieving the desired performance), you can generally diagnose the problem by comparing the actual to ideal op amp behavior. The following are two critical characteristics to remember when troubleshooting amplifier circuits utilizing op amps:

1. The output should be between the saturation limits.
2. The differential input voltage (v_D) should be very near 0.

2.10.1 Basic Troubleshooting Concepts

When troubleshooting any type of circuit, it is important to use a logical, systematic technique. Although there are several accepted methods, the following sequence of activities is a common and effective procedure:

1. Observation
2. Signal injection/tracing
3. Voltage measurements
4. Resistance measurements

Observation. This is probably the most important step in the process if done effectively. Observation means more than just looking at the circuit. It includes all of the following actions:

1. Interrogate the owner, user, or operator for clues regarding how the trouble developed.
2. Operate the user controls and observe the behavior for clues.
3. Use your senses. Do you see any visible damage? Do you smell burned components? Do you hear suspicious sounds?
4. Be alert to similarities between observable symptoms on the defective unit and the symptoms of previously diagnosed circuits.

Many problems can be identified during the observation stage. How many of us have "successfully" traced a malfunction throughout a complex circuit until we located a suspected switch or variable resistor on the schematic? Then, when we physically locate the suspected component on the system, it turns out to be a front panel control! Had we applied the preceding procedure faithfully, we could have reduced our efforts dramatically.

Signal Injection/Tracing. All electronic circuits can be diagnosed to some extent by signal injection, signal tracing, or a combination of the two methods. The underlying goal for this process is to reduce the number of possible culprits down from a set consisting of every component in the system to a smaller set consisting of only a few components.

Signal injection requires us to inject a known, good signal at some point in the circuit and observe the effects. If the circuits that utilize this signal then appear to operate normally, we can infer that the malfunction is located ahead of our injection point. We then move our injection point closer to the source of the trouble and inject another signal. Again, the behavior of the subsequent circuits will provide guidance as to our next injection point. Two common types of test equipment for signal injection are signal generators and logic pulsers.

Signal tracing is similar in concept, except we put a known good signal at the input and verify (trace) its presence throughout the circuit. If we lose the signal (or it becomes distorted) at a certain point, then we can infer that the trouble lies ahead of the monitored point. The oscilloscope and logic probe are two common types of signal tracing equipment.

Both signal tracing and signal injection can be enhanced by using the split-half method of troubleshooting. By selecting your injection or monitor point to be approximately halfway through the suspected range of components, each measurement effectively reduces the number of possible components by half.

Voltage Measurements. Voltage measurements normally occur after you have isolated the problem down to a particular stage consisting of up to perhaps 10 components. The voltage checks contrasted with normal values should result in the narrowing of suspects down to one or two possibilities. Distinction between the signal tracing and voltage measuring phases often becomes blurred when an oscilloscope is used. The concept remains valid, however.

Resistance Measurements. Resistance checks are performed last because accurate measurements often require desoldering of a component. Desoldering not only is time consuming but also risks damage to an expensive printed circuit board in many cases. The resistance checks are done to verify that you have in fact located the defective component. Component testers can also be used at this point if available and appropriate.

2.10.2 Specific Techniques for Op Amps

Through observation and signal injection/tracing, the technician can normally isolate the problem down to a specific circuit. For this discussion, we will assume the problem has been isolated to an amplifier circuit built around an op amp. The following sequence of activities will normally isolate the defective component:

1. Verify the power supply voltage on the op amp.
2. Measure output voltage.
3. Measure differential input voltage (v_D).
4. Compare the results of steps 2 and 3. If the results violate basic theory (e.g., noninverting input is more positive than inverting input, but output is

negative), then the op amp is probably bad. If no basic theory principles are violated, check the following:

a. Correct input (especially the DC level)
b. Feedback path
c. Input path

Your most powerful troubleshooting tool when diagnosing op amp circuits is a solid grasp of the basic theory of operation. Although the performance of op amps can deteriorate in some ways, it is far more common for the device to exhibit catastrophic failure.

REVIEW QUESTIONS

1. A certain amplifier has a voltage gain of 100. Express this gain in decibels.
2. Suppose the amplifier circuit shown in Figure 2.3 is altered to have the following values:

$$R_I = 39\ k\Omega$$

$$R_F = 470\ k\Omega$$

$$R_B = 36\ k\Omega$$

$$R_L = 68\ k\Omega$$

   What is the voltage gain of the circuit with the new values? What happens to the voltage gain if R_L is decreased to 27 kilohms?
3. Refer to the amplifier circuit described in question 2. Compute the input impedance of the circuit. Does the input impedance change if R_L is reduced to 27 kilohms?
4. If a 741 op amp is powered by a ±15-volt supply, what is the largest voltage swing that can be guaranteed on the output if the load is 18 kilohms? Repeat this question for a 2.0-kilohm load.
5. A certain op amp application requires a 5-volt RMS output voltage swing and operates at a maximum sinewave frequency of 21.5 kilohertz. What is the minimum slew rate for the op amp that will allow the signal to pass without substantial slew rate distortion?
6. A simple noninverting amplifier (similar to Figure 2.12) has the following component values:

Op amp	741
R_I	$4.7\ k\Omega$
R_F	$68\ k\Omega$
R_L	$18\ k\Omega$
R_B	$4.3\ k\Omega$

   Compute the small signal bandwidth of the amplifier (ignore slew rate considerations).

7. The value of C_I in Figure 2.26(a) is the primary factor that sets the upper cutoff frequency. (True or False) Explain why or why not.
8. If capacitor C_O in Figure 2.26(b) becomes open, what effect will this have on circuit operation to the left of capacitor C_O?
9. If capacitor C_I in Figure 2.26(b) becomes open, what happens to the DC voltage on the output pin of the op amp? What happens to the DC voltage across R_L?
10. Refer to Figure 2.32. As the wiper arm of R_P is moved to the right, what happens to the average current through R_L?
11. Refer to Figure 2.32. If the wiper arm of R_P is moved too far to the left, the output waveform will start to clip. Explain which peak (positive or negative) is clipped and why.
12. Refer to Figure 2.21. What happens to the average (i.e., DC) current through R_L if R_{I1} becomes open?
13. What is another name for a noninverting amplifier with a voltage gain of 1?
14. Can a standard 741 op amp be used to amplify a 33-kilohertz signal if the desired voltage gain is 5 and the maximum peak output voltage swing is 11 volts? Explain your answer.
15. While troubleshooting the circuit shown in Figure 2.27(a), you discover that the voltage on the inverting (–) pin of the op amp is approximately 0 volts (with a normal signal applied at the input). If you think this is normal, explain why. If you think it is abnormal, what is the most likely defect?

CHAPTER THREE

Voltage Comparators

3.1 VOLTAGE COMPARATOR FUNDAMENTALS

A voltage comparator circuit compares the values of two voltages and produces an output to indicate the results. The output is always one of two values (i.e., the output is digital). Suppose, for example, we have two voltage comparator inputs labeled A and B. The circuit can be designed so that if input A is a more positive voltage than input B, the output will go to $+V_{SAT}$. Similarly, if input A is less positive than input B, the output will go to $-V_{SAT}$. In general, the voltage comparator circuit accepts two voltages as inputs and produces one of two distinct output voltages depending on the relative values of the two inputs.

During the preceding discussion, we were careful not to consider what happens when the two input voltages are equal. In a simple voltage comparator, this condition can produce indeterminate operation. That is, the output may be at either of the two normal output voltage levels or, more probably, oscillating between the two output levels. This erratic behavior is easily overcome by adding positive feedback to the comparator. With positive feedback, the circuit has *hysteresis*. In the simple comparator circuit, output switching occurs when the two input voltages are equal. Hysteresis causes the circuit to have two different switching points. This important concept will be explained in greater detail in Section 3.3.

Voltage comparator circuits are widely used in analog-to-digital converter applications and for various types of alarm circuits. In the alarm application, one input to the comparator is controlled by the monitored signal (e.g., the voltage produced by a pressure transducer). The second input is connected to a reference voltage representing the safe level. If the pressure in the device being monitored exceeds the safe limit, the comparator output will change states and sound an alarm. Figure 3.1 illustrates a voltage comparator circuit used in conjunction with a pressure sensor and a potentiometer. If the pressure being monitored exceeds a certain prescribed value, the voltage generated by the pressure sensor exceeds the preset voltage on the potentiometer. This causes the output voltage to change states and to sound the alarm.

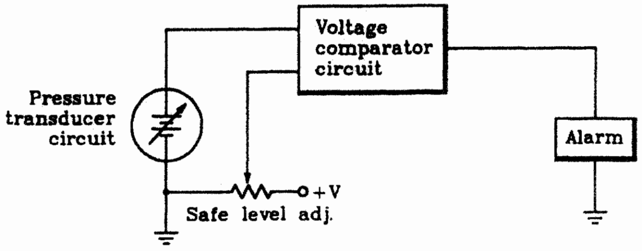


FIGURE 3.1 The voltage comparator is often used in alarm applications. In this figure, the alarm sounds when the voltage from the pressure sensor exceeds the voltage set by the potentiometer.

3.2 ZERO-CROSSING DETECTOR

3.2.1 Operation

Figure 3.2 shows the schematic of a simple inverting voltage comparator being used as a zero-crossing detector. That is, the output of the comparator switches every time the input signal passes through (i.e., crosses) zero volts. As simple as it is, this circuit has practical applications.

One way to view the operation of the circuit in Figure 3.2 is to consider it to be an open-loop amplifier. That is, with no feedback, the gain of the amplifier is simply the open-loop gain of the op amp itself. Since this gain value is very high (at least at low frequencies), we know the output will be driven to either $+V_{SAT}$ or $-V_{SAT}$ if the input is more than perhaps 1 microvolt or so above or below ground potential.

Since the output voltage is at one of the two saturation levels at all times (except during the short switching time), the circuit essentially converts the sinewave input into a square wave. The resulting square wave will have the same frequency as the input, but the amplitude will always swing between $\pm V_{SAT}$ regardless of the value of the input voltage. Figure 3.3 illustrates the relationship between the input and output waveforms.

The output of a voltage comparator switches between two voltage limits ($\pm V_{SAT}$ in the case of the simple comparator in Figure 3.2). In a real op amp, it takes a small but definite amount of time for the output to switch between the two voltage levels. The maximum rate at which the output can change states is called the slew rate of the op amp and is specified in the manufacturer's data sheet. If the input frequency is too high (i.e., changes too quickly), then the output of the op

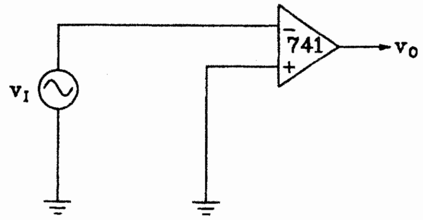


FIGURE 3.2 A simple inverting voltage comparator circuit used as a zero-crossing detector.

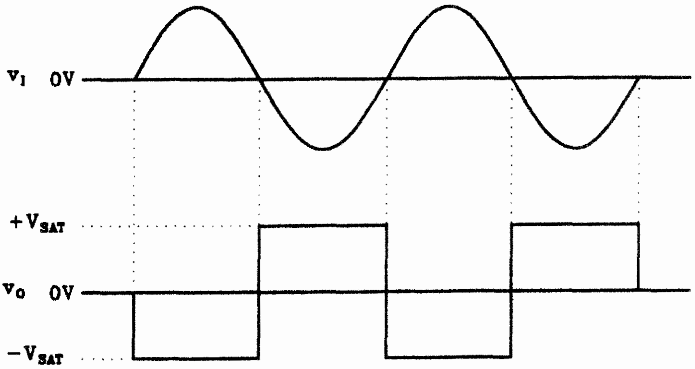


FIGURE 3.3 The input/output relationships for the zero-crossing detector shown in Figure 3.2

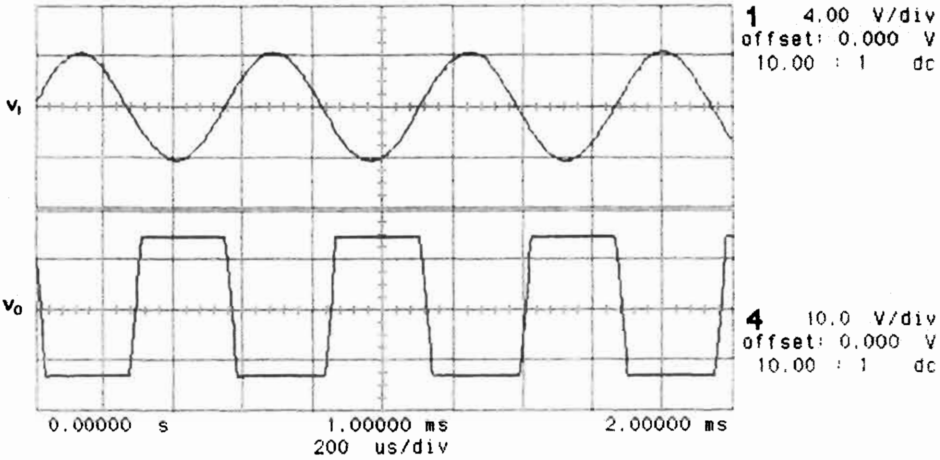


FIGURE 3.4 Oscilloscope displays showing the effect of slew rate on the output of a zero-crossing detector circuit. (Test equipment courtesy of Hewlett-Packard Company.)

amp cannot change fast enough to keep up with the input. The initial effects of slew rate become evident by nonideal rise and fall times on the output waveshape. If the frequency continues to increase, the rise and fall times—which are established by the slew rate—become a significant part of the output waveform. Figure 3.4 illustrates the effects of slew rate on the output of the simple comparator circuit.

3.2.2 Numerical Analysis

For purposes of numerical analysis of the circuit shown in Figure 3.2, let us assume the following input signal characteristics:

1. Input frequency	1.8 kilohertz
2. Input voltage	3 volts RMS
3. Input reference	0 volts

Minimum Input Impedance. The input impedance is established by the differential input resistance of the op amp. The input resistance of the 741 (R_D) is listed in the manufacturer's data sheet (Appendix 1) as at least 300 kilohms. The minimum input resistance, then, is computed as

$$\boxed{R_{IN} = R_D \qquad (3.1)}$$

In this particular case,

$$R_{IN} = R_D = 300\ k\Omega$$

It is important to note that without feedback the (–) input does not behave as a virtual ground.

Maximum Input Current. The maximum input current can be calculated by application of Ohm's Law:

$$\begin{aligned} i_I(\text{max}) &= \frac{v_I}{R_{IN}(\text{min})} \\ &= \frac{3\ V}{300\ k\Omega} \\ &= 10\ \mu A\ RMS \end{aligned}$$

Since this is a sinusoidal waveform, we can convert it to a peak value if desired:

$$\begin{aligned} i_I(peak) &= i_I(RMS) \times 1.414 \\ &= 10\ \mu A \times 1.414 \\ &= 14.14\ \mu A\ peak \end{aligned}$$

Output Voltage. The limits of the output voltage in the circuit shown in Figure 3.2 are simply the values of $\pm V_{SAT}$. For ±15-volt power supplies and a load resistance of greater than 10 kilohms, the manufacturer's data sheet in Appendix 1 lists a minimum output swing of ±12 volts. If we loaded the circuit with a resistance of less than 10 kilohms, we could expect the output levels to decrease.

3.2.3 Practical Design Techniques

For low-frequency noncritical applications, the simple circuit shown in Figure 3.2 can be very useful. For purposes of a design example, let us develop a circuit to satisfy the following requirements:

1. Input voltage	500 millivolts peak
2. Input frequency	1 to 10 kilohertz

3. Input reference	0 volts
4. Minimum output voltage	±10 volts
5. Load resistance	68 kilohms

Op Amp Selection. We must select an op amp that can satisfy the output voltage requirements, survive the input voltage swings, and respond to the input frequencies. The manufacturer's data sheet in Appendix 1 confirms that a 741 is capable of delivering a ±10-volt output. More specifically, the minimum output voltage with ±15-volt supplies and a load of greater than 10 kilohms is ±12 volts.

Additionally, the data sheet indicates that input voltage levels may be as high as the value of supply voltage. So far, the 741 seems like a good choice. Now let us consider the frequency effects.

The open-loop voltage comparator application requires the output voltage of the op amp to change from one extreme to the other. This change requires a finite amount of time. For DC or low-frequency applications, this amount of time is generally insignificant. As the input frequency increases, however, the switching time becomes a greater portion of the total time for one alternation of the input signal. In the extreme case, if the input alternation were shorter than the time required for the output to change states, then the comparator would cease to function properly. That is, the output voltage would not have time to reach its limits.

The slew rate of the op amp determines the maximum rate of change in the output voltage. The minimum acceptable rate of change is determined by the application. For purposes of example and as a good rule of thumb, let us design our circuit to have rise and fall times of no greater than 10 percent of the time for an alternation of the input signal. For our present design, the highest input frequency was specified as 10 kilohertz. The time for one alternation can be calculated from our basic electronics theory as

$$\boxed{t(alternation) = \frac{t(period)}{2} \qquad (3.2)}$$

where $t(period) = 1/frequency$. In our case,

$$t(period) = \frac{1}{frequency} = \frac{1}{10\ kHz} = 100\ \mu s$$

and

$$t(alternation) = \frac{100\ \mu s}{2} = 50\ \mu s$$

Our maximum rise and fall times will then be computed as

$$t_R(\text{max}) = t_F(\text{max}) = 0.1 \times t(\textit{alternation}) \tag{3.3}$$

In the present case, we have

$$t_R(\text{max}) = t_F(\text{max}) = 0.1 \times 50\ \mu s = 5\ \mu s$$

The minimum acceptable slew rate for our op amp can be computed with the following equation:

$$\textit{slew rate}(\text{min}) = \frac{+V_{SAT} - (-V_{SAT})}{t_R(\text{max})} \tag{3.4}$$

In our present example, the minimum acceptable slew rate is computed as

$$\textit{slew rate}(\text{min}) = \frac{12\ V - (-12\ V)}{5\ \mu s} = 4.8 \times 10^6\ V/s$$

It is common to divide this result by 10^6 and express the slew rate in terms of volts per microsecond. In our case,

$$\frac{4.8 \times 10^6\ V/s}{10^6} = 4.8\ V/\mu s$$

The slew rate for a 741 op amp is listed in the data sheet as 0.5 volts per microsecond. Clearly, this is too slow for our application. If we use the 741, our output signal will look more like a triangle wave than a square wave. Appendix 4 shows the data for another alternative.

The MC1741SC op amp should satisfy the voltage specifications of our design. Additionally, the minimum slew rate is listed as 10 volts per microsecond. We will use the MC1741SC for our design.

Figure 3.5 shows the resulting design. The oscilloscope displays in Figure 3.6 reveal the actual performance of the circuit.

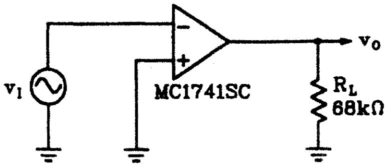
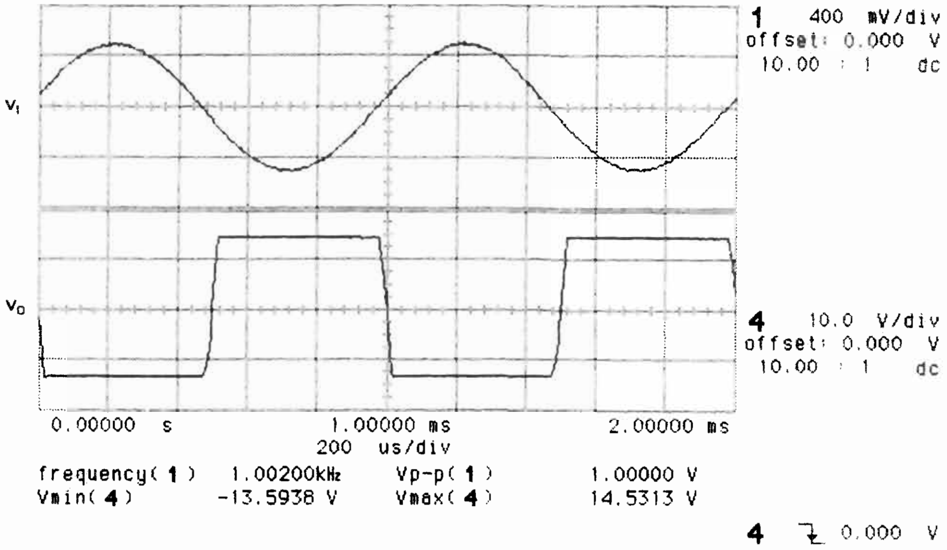


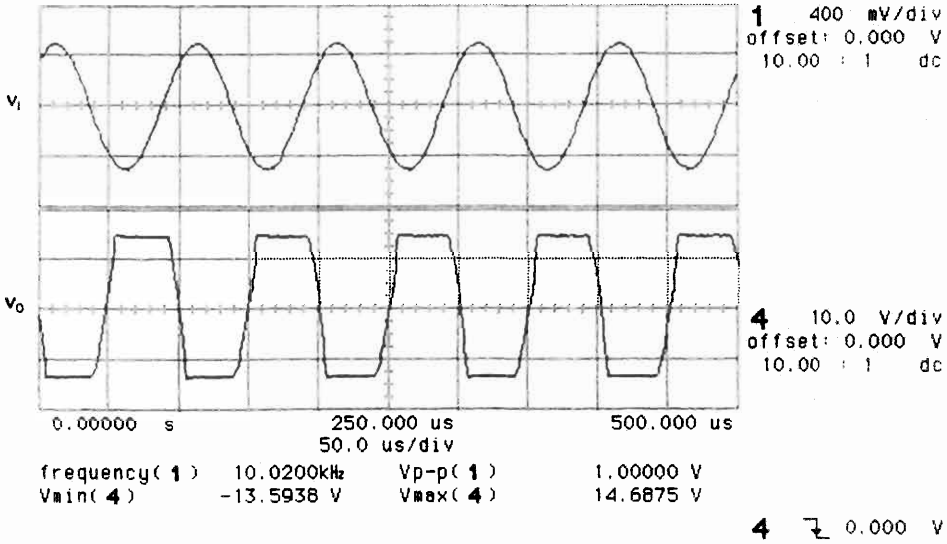
FIGURE 3.5 A simple zero-crossing detector designed around an MC1741SC op amp.

Low-Frequency Performance



(a)

High-Frequency Performance



(b)

FIGURE 3.6 Oscilloscope displays showing the actual performance of the circuit in Figure 3.5. (Test equipment courtesy of Hewlett-Packard Company.)

3.3 ZERO-CROSSING DETECTOR WITH HYSTERESIS

3.3.1 Operation

Figure 3.7 shows the schematic diagram of a zero-crossing detector with hysteresis. At first glance, the configuration may resemble a basic amplifier circuit similar to those discussed in Chapter 2. A more careful examination, however, will reveal that the feedback is applied to the (+) input terminal. That is, the circuit is using positive feedback.

Resistors R_F and R_1 form a voltage divider for the output voltage. The portion of the output voltage that appears across R_1 is felt on the (+) input of the op amp. This voltage establishes what is called the threshold voltage. When the output is positive, the voltage on the (+) input is called the positive, or upper, threshold voltage (V_{UT}). The voltage on this same input when the output is negative is called the lower, or negative, threshold voltage (V_{LT}). For the circuit in Figure 3.7, these two threshold levels will be the same magnitude but opposite polarity. In some circuits, it is desirable to have different values and/or different polarities for the upper and lower thresholds.

To examine the operation of the circuit, let us assume that the input voltage is at its most negative value and that the output is driven to its positive saturation level. A portion of the positive output voltage will be developed across R_1 and appear on the (+) input. This is our upper threshold voltage. As long as the input voltage is below the value of the upper threshold voltage, the circuit will remain in its present condition (positive saturation).

Once the input voltage exceeds (i.e., becomes more positive than) the upper threshold voltage, the (–) pin becomes more positive than the (+) pin of the op amp. Basic op amp operation tells us that the amplifier will produce a negative output voltage. In our case, the output will drive all the way to its negative saturation limit.

Once the output reaches its negative limit, the (+) input has a different voltage—the negative, or lower, threshold voltage—on it. The circuit will remain in this stable condition as long as the input voltage is more positive than the lower threshold voltage.

Notice the voltages at which output switching occurs. When the input signal is rising, the switching point is determined by the upper threshold voltage. When the signal returns to a lower voltage, however, the output does not switch states as

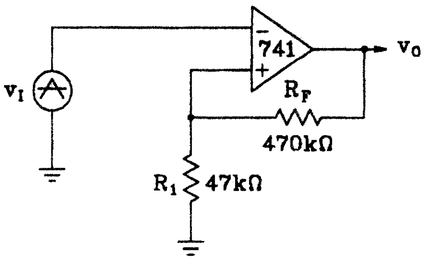


FIGURE 3.7 Positive feedback adds hysteresis to the zero-crossing detector.

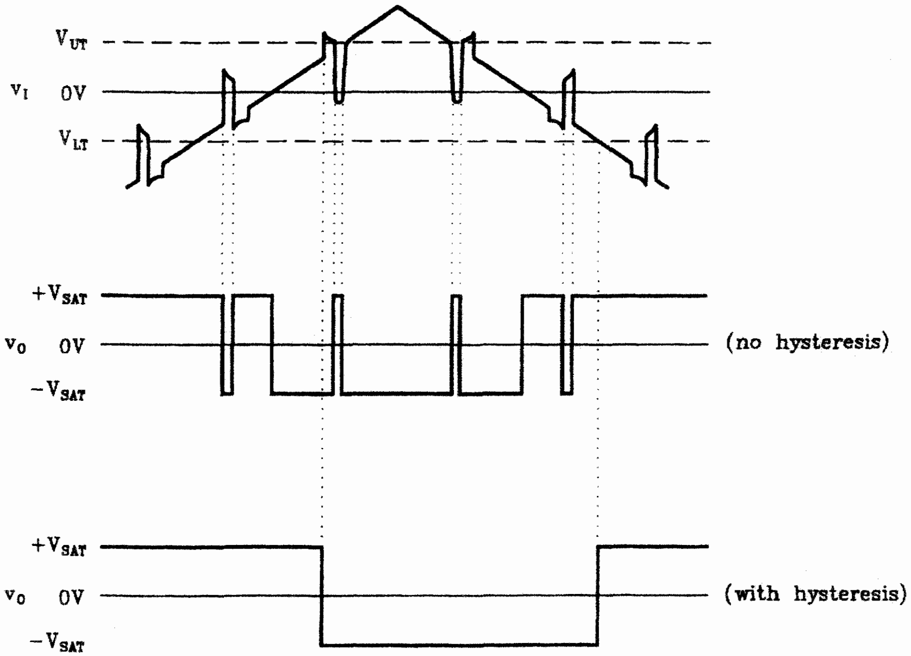


FIGURE 3.8 Hysteresis makes the zero-crossing detector less sensitive to noise.

the upper threshold voltage is passed. Rather, the input voltage must go all the way down to below the lower threshold before the output will change states.

The difference between the two threshold voltages is called the *hysteresis.* The amount of hysteresis is determined by the values of the voltage divider consisting of R_F and R_1 and by the levels of output voltage ($\pm V_{SAT}$ in the present case).

Positive feedback makes the circuit more immune to noise. To understand this effect, consider the drawings in Figure 3.8, which represent a dual-ramp input voltage with superimposed noise pulses. The output voltage waveform (v_O) for a circuit without hysteresis shows a response every time the combination of input voltage and noise crosses 0. For the circuit with hysteresis, however, once the output has changed states, the combination of input ramp and noise voltage must extend all the way to the opposite threshold voltage before the output will show a response.

3.3.2 Numerical Analysis

Let us now analyze the circuit shown in Figure 3.7. We shall determine the following values:

1. Upper threshold voltage
2. Lower threshold voltage
3. Hysteresis
4. Maximum frequency of operation

Upper Threshold Voltage. The upper threshold voltage is the value of voltage that appears across R_1 when the output is at its maximum positive level. In our present circuit, the maximum output is essentially $+V_{SAT}$. We will use the lowest value given in Appendix 1 (10 volts) for $+V_{SAT}$. The value of threshold voltage is computed by applying the basic voltage divider formula.

$$V_{R_1} = V_T\left(\frac{R_1}{R_1 + R_F}\right) \tag{3.5}$$

where V_T is the total voltage across the series resistors R_1 and R_F. In our case, we have

$$V_{UT} = 10\ V\left(\frac{47\ k\Omega}{47\ k\Omega + 470\ k\Omega}\right) = 0.91\ V$$

This calculation reveals a significant limitation for this circuit. The value of threshold voltage is directly affected by the value of V_{SAT}. That value, however, is far from constant. Appendix 1 indicates that V_{SAT} can vary from a low value of 10 volts (with a heavy load) to as high as 14 volts when lightly loaded. The resulting variation in threshold voltage may be objectionable in some applications. If so, the feedback voltage can be regulated (e.g., by using a pair of zener diodes) for more consistent performance.

Lower Threshold Voltage. The lower threshold voltage for the circuit shown in Figure 3.7 is computed using the same method, Equation (3.5), discussed for the upper threshold. The value is computed as

$$\begin{aligned} V_{LT} &= -V_T\left(\frac{R_1}{R_1 + R_F}\right) \\ &= -10\ V\left(\frac{47\ k\Omega}{47\ k\Omega + 470\ k\Omega}\right) = -0.91\ V \end{aligned}$$

The lower threshold suffers from the same variations described for the upper threshold. Also notice that in this particular circuit, the upper and lower threshold voltages are equal in magnitude and positioned on either side of 0 volts. Other circuits may have dissimilar magnitudes for the two thresholds. Additionally, the thresholds are not necessarily centered around 0 in all detector circuits.

Hysteresis. The hysteresis of the circuit shown in Figure 3.7 is simply the difference between the two threshold voltages. That is,

$$V_H = V_{UT} - V_{LT} \tag{3.6}$$

In the present case, we have

$$V_H = +0.91\ V - (-0.91\ V) = 1.82\ V$$

The higher the value of hysteresis, the more noise immunity offered by the circuit. In the present case, once the input voltage has crossed one of the threshold levels, it will take a noise pulse of the opposite polarity and with a magnitude of at least 1.82 volts before the output will respond.

In the case of equal $\pm V_{SAT}$ voltages, the hysteresis may be computed directly with the following equation:

$$\boxed{V_H = 2V_{SAT}\left(\frac{R_1}{R_1 + R_F}\right) \qquad (3.7)}$$

Maximum Frequency of Operation. Since the output voltage of the zero-crossing detector switches between two extreme voltages, the upper frequency limit is more appropriately determined by considering the effects of slew rate rather than the falling amplification. You will recall that the slew rate of an op amp limits the rate of change of output voltage. For purposes of this calculation, we will determine the highest operating frequency that allows the output to switch fully between $\pm V_{SAT}$. If we exceed this frequency, the output amplitude will begin to diminish. The reduced output voltage will produce a similar reduction in threshold voltages and the hysteresis voltage.

Appendix 1 lists the slew rate of a 741 op amp as 0.5 volts per microsecond. The output must change from one saturation level to the other during the time for half of the input period (assuming a symmetrical output signal). For purposes of worst-case design, let us assume that the saturation voltages are at their highest magnitudes (listed as ±14 volts in Appendix 1). The minimum time required to switch between these two limits is computed as shown:

$$\boxed{t_S(\text{min}) = \frac{+V_{SAT} - (-V_{SAT})}{slew\ rate} \qquad (3.8)}$$

In the case of equal magnitudes of $\pm V_{SAT}$ voltages, this can be expressed as

$$\boxed{t_S(\text{min}) = \frac{2V_{SAT}}{slew\ rate} \qquad (3.9)}$$

In our present case, the minimum switching time is determined as shown:

$$t_S(\text{min}) = \frac{2 \times 14\ V}{0.5\ V/\mu s} = 56\ \mu s$$

Since this corresponds to half of the period of the highest input frequency, we can determine the upper frequency as shown:

$$f(\text{max}) = \frac{1}{2t_S(\text{min})} \tag{3.10}$$

In our case, we have

$$f(\text{max}) = \frac{1}{2 \times 56\ \mu s} = 8.9\ kHz$$

The above equation represents a worst-case situation. It should be noted, however, that the output waveform under these extreme conditions will more closely resemble a triangle waveform than a square wave. Whether or not this is objectionable is totally dependent upon the application. In cases where output rise and fall times must be short compared to the pulse width, the following equation can be used to determine the highest operating frequency for a particular ratio (ρ) of switching time (t_S) to stable time (t_P).

$$f(\text{max}) = \frac{\rho}{2t_S(\rho + 1)} \tag{3.11}$$

In the case of Figure 3.7, we have already computed t_S as 56 microseconds. Now suppose we want the switching times (rise and fall) to be one-tenth (0.1) of the stable time (t_P). This establishes our ratio ρ as 0.1. The highest frequency is then computed as

$$\begin{aligned} f(\text{max}) &= \frac{\rho}{2t_S(\rho + 1)} \\ &= \frac{0.1}{2 \times 56\ \mu s(0.1 + 1)} \\ &= 811.7\ Hz \end{aligned}$$

If the input waveform is such that the output will not be symmetrical, then t_S establishes the shortest (either positive or negative) alternation of the output waveform. The highest frequency of operation, however, can be obtained when the output waveform is symmetrical.

3.3.3 Practical Design Techniques

Let us now design a zero-crossing detector circuit similar to that shown in Figure 3.7. We will design to achieve the following:

1. Upper threshold +0.5 volts
2. Lower threshold −0.5 volts

3.	Hysteresis	1.0 volts
4.	Highest operating frequency	15 kilohertz
5.	Maximum ratio (ρ) of switching time to stable time	0.2
6.	Power supply voltages	±15 volts

Determine the Required Slew Rate. In this type of application, slew rate is probably the most critical parameter with regard to op amp selection. The slew rate must be high enough to allow the output to switch between saturation levels within the allowed switching time (t_S). The switching time is computed by using a transposed version of the $f(\max)$ equation. That is,

$$\boxed{t_S = \frac{\rho}{2(\rho + 1) \times f(\max)} \qquad (3.12)}$$

For the present circuits, we have

$$t_S = \frac{0.2}{2(0.2 + 1) \times 15\ kHz} = 5.56\ \mu s$$

For purposes of op amp selection, we can assume that the output swings between the two power supply limits. That is, assume that $\pm V_{SAT} = \pm V_{CC}$. The required slew rate can then be computed as

$$\boxed{slew\ rate(\min) = \frac{2V^+}{t_S} \qquad (3.13)}$$

For the present circuit, we have

$$slew\ rate(\min) = \frac{2 \times 15\ V}{5.56\ \mu s} = 5.4\ V/\mu s$$

Select an Op Amp. Appendix 1 indicates that the slew rate for a 741 is only 0.5 volts per microsecond, which clearly eliminates this device as an option because we will require a slew rate of at least 5.4 volts per microsecond. Appendix 4, however, shows that the MC1741SC op amp has a minimum slew rate of 10 volts per microsecond. This will satisfy our present requirements nicely, and it is compatible with our power supply requirements. We will build our design around the MC1741SC op amp.

Determine R_F and R_1. The ratio of R_F and R_1 is dependent on the ratio of V_{SAT} voltage to hysteresis voltage. Appendix 4 indicates that the unloaded output swing will be approximately ±13 volts. We use this value for our computations. If the circuit is expected to drive a greater load (smaller load resistor), then the output will be correspondingly smaller. The ratio of R_F to R_1 is computed as follows:

$$\frac{R_F}{R_1} = \frac{2V_{SAT}}{V_H} - 1 \tag{3.14}$$

More specifically, for the present circuit we have

$$\frac{R_F}{R_1} = \frac{2 \times 13\ V}{1\ V} - 1 = 25$$

Many combinations of R_F and R_1 will produce a 25:1 ratio. We will select R_1 and calculate the value of R_F. If possible, we generally want both resistors in the range of 1.0 kilohm to 1.0 megohm, although these do not represent absolute limits. For purposes of this example, we select R_1 to be 4.7 kilohms. Having done this, we can now compute R_F by simply multiplying R_1 by the R_F/R_1 ratio.

$$R_F = \left(\frac{R_F}{R_1}\right) R_1 \tag{3.15}$$

And, in the present case,

$$R_F = 25 \times 4.7\ k\Omega = 118\ k\Omega$$

We will select a standard value of 120 kilohms.

This completes the design of the simple zero-crossing detector circuit. The schematic is shown in Figure 3.9. The circuit performance is shown by the oscilloscope displays in Figure 3.10. The original design goals are contrasted with the measured performance in Table 3.1.

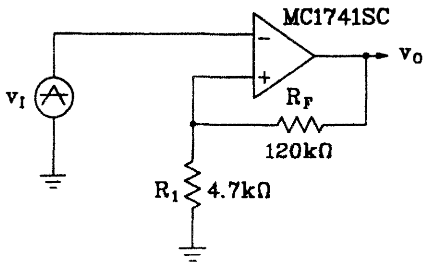
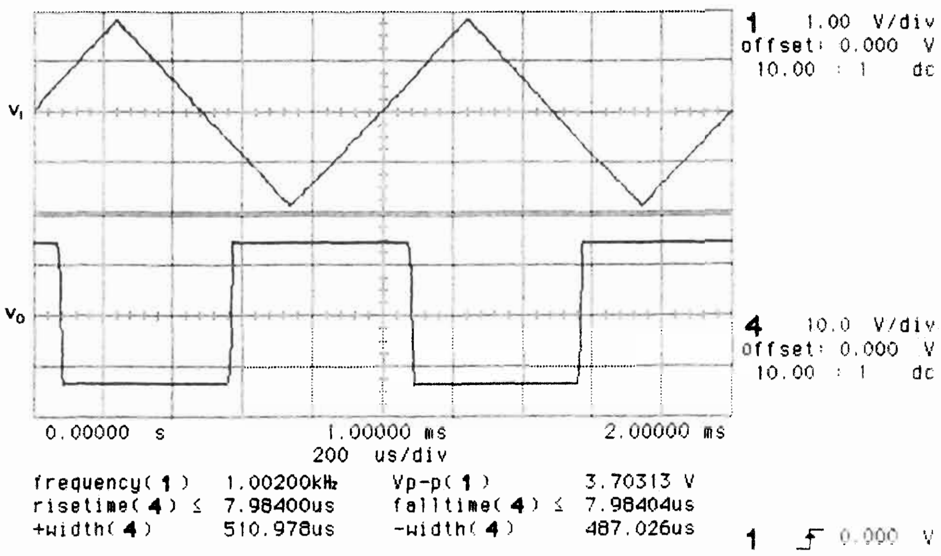
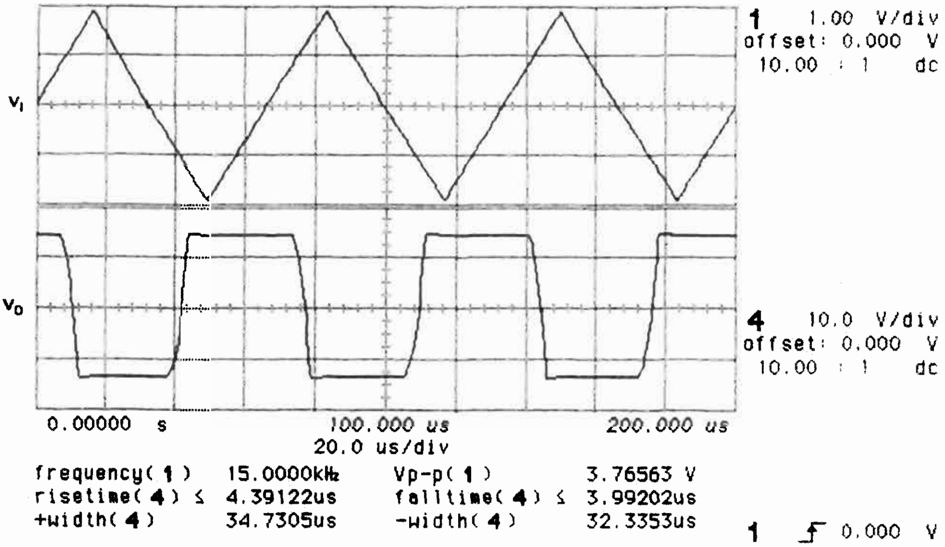


FIGURE 3.9 A zero-crossing detector designed for 1.0 volt hysteresis and operation up to 15 kilohertz.


Low-Frequency Performance

```
frequency( 1 )   1.00200kHz    Vp-p( 1 )        3.70313 V
risetime( 4 ) ≤  7.98400us     falltime( 4 ) ≤  7.98404us
+width( 4 )      510.978us     -width( 4 )      487.026us
```

(a)


High-Frequency Performance

```
frequency( 1 )   15.0000kHz    Vp-p( 1 )        3.76563 V
risetime( 4 ) ≤  4.39122us     falltime( 4 ) ≤  3.99202us
+width( 4 )      34.7305us     -width( 4 )      32.3353us
```

(b)

FIGURE 3.10 Waveforms showing the actual circuit performance of the zero-crossing detector shown in Figure 3.9. (Test equipment courtesy of Hewlett-Packard Company).

TABLE 3.1

	Design Goal	*Measured Values*
Upper threshold	+0.5 volts	+0.54 volts
Lower threshold	–0.5 volts	–0.51 volts
Hysteresis	1.0 volts	1.05 volts
Maximum switching ratio	0.2	0.126

3.4 VOLTAGE COMPARATOR WITH HYSTERESIS

3.4.1 Operation

Figure 3.11 is a schematic of an inverting voltage detector with hysteresis. The operation of this circuit is similar to that of the zero-crossing detector discussed in the last section, but the upper and lower thresholds are on either side of a reference voltage (V_{REF}) rather than on either side of 0. The reference voltage can be either positive or negative. Note that if the reference is 0 volts, then the circuit is identical to the zero-crossing detector previously discussed.

To begin the discussion, let us assume that the input voltage is at its most negative value and that the output of the op amp is driven to its $+V_{SAT}$ level. The $+V_{SAT}$ output is divided between R_F and R_1 in normal voltage divider fashion. The voltage appearing across R_1 plus the value of the reference voltage determines the voltage on the (+) input terminal. This is the upper threshold voltage. The circuit will remain in this condition as long as the input voltage is below the voltage on the (+) terminal.

Now suppose that the input voltage is allowed to exceed the upper threshold voltage that is present on the (+) input. If this happens, the output will quickly go to the $-V_{SAT}$ level. R_F and R_1 will divide the negative output voltage. The portion across R_1 plus the value of the reference voltage determines the voltage on the (+) input terminal. This is the lower threshold voltage. The circuit will remain in this stable condition until the input voltage falls below the negative threshold voltage.

In many practical comparator circuits, the reference voltage is provided by a zener diode (see, for example, Figure 3.12 further on) or other voltage regulator circuit.

3.4.2 Numerical Analysis

We will now analyze the circuit shown in Figure 3.11 to determine the following:

1. Upper threshold voltage
2. Lower threshold voltage
3. Hysteresis
4. Maximum frequency of operation

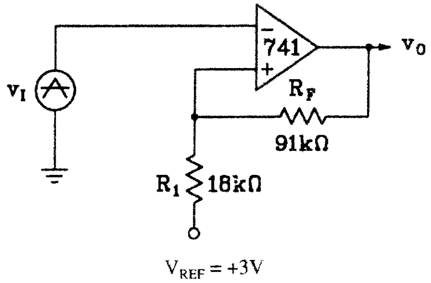


FIGURE 3.11 A voltage comparator with hysteresis.

Upper Threshold Voltage. The upper threshold voltage is the value of the voltage that appears across R_1 when the output is at its maximum positive level, plus the value of the reference voltage. Appendix 1 lists a minimum value of 10 volts for $+V_{SAT}$. The value of the threshold voltage is computed by applying the basic voltage divider formula to R_F and R_1 and then adding the result to the reference voltage (V_{REF}).

$$V_{UT} = +V_{SAT}\left(\frac{R_1}{R_1 + R_F}\right) + V_{REF} \tag{3.16}$$

For this particular circuit, we have

$$V_{UT} = 10\ V\left(\frac{18\ k\Omega}{18\ k\Omega + 91\ k\Omega}\right) + 3\ V = 4.65\ V$$

As with the zero-crossing detector previously discussed, the threshold voltages vary with V_{SAT}. If this variation is objectionable, then the output can be regulated by zeners, as discussed in Section 3.6.

Lower Threshold Voltage. The lower threshold voltage for the circuit shown in Figure 3.11 is computed using the same method discussed for the upper threshold:

$$V_{LT} = -V_{SAT}\left(\frac{R_1}{R_1 + R_F}\right) + V_{REF} \tag{3.17}$$

or, more specifically,

$$V_{LT} = -10\ V\left(\frac{18\ k\Omega}{18\ k\Omega + 91\ k\Omega}\right) + 3\ V = 1.35\ V$$

The lower threshold suffers from the same variations described for the upper threshold. Also, notice that in this particular circuit, the upper and lower threshold voltages are both above 0 volts but equally spaced on either side of the reference voltage. The thresholds in some circuits are not equally spaced around the reference.

Hysteresis. The hysteresis of the circuit shown in Figure 3.11 is simply the difference, as given by Equation (3.6), between the two threshold voltages. That is,

$$\begin{aligned} V_H &= V_{UT} - V_{LT} \\ &= +4.65\ V - 1.35\ V \\ &= 3.3\ V \end{aligned}$$

Recall that the value of hysteresis primarily determines the noise immunity offered by the circuit. In the present case, once the input voltage has crossed one of the threshold levels, it will take a noise pulse of the opposite polarity and with a magnitude of at least 3.3 volts before the output will respond.

The hysteresis in this circuit may also be computed directly with Equation (3.7).

Maximum Frequency of Operation. The upper frequency of operation is limited in the same manner as the zero-crossing detector discussed previously. This frequency is estimated with Equation (3.10):

$$f(\text{max}) = \frac{1}{2t_S(\text{min})}$$

where t_S is computed with Equation (3.8) as shown:

$$t_S(\text{min}) = \frac{+V_{SAT} - (-V_{SAT})}{\textit{slew rate}}$$

Or, in the usual case of symmetrical power supplies, we can simply use Equation (3.9) as follows:

$$t_S(\text{min}) = \frac{2V_{SAT}}{\textit{slew rate}}$$

In our present case, let us determine the minimum switching time with Equation (3.9):

$$\begin{aligned} t_S(\text{min}) &= \frac{2V_{SAT}}{\textit{slew rate}} \\ &= \frac{2 \times 10\ V}{0.5\ V/\mu s} \\ &= 40\ \mu s \end{aligned}$$

Substituting this value into the maximum frequency formula, Equation (3.10), gives us

$$
\begin{aligned}
f(\max) &= \frac{1}{2t_S(\min)} \\
&= \frac{1}{2 \times 40\ \mu s} \\
&= 12.5\ kHz
\end{aligned}
$$

The above equation represents a worst-case situation for a symmetrical output waveform. As noted in the zero-crossing circuit, the output waveform under these extreme conditions will more closely resemble a triangle waveform than a square wave. In cases where output rise and fall times must be short compared to the pulse width, Equation (3.11) can be used to determine the highest operating frequency for a particular ratio (ρ) of switching time (t_S) to stable time (t_P). In the case of Figure 3.11, we have already computed t_S as 40 microseconds. Now suppose we want the switching times (rise and fall) to be one-eighth (0.125) of the stable time (t_P). This establishes our ratio ρ as 0.125. The highest frequency is then computed with Equation (3.11) as

$$f(\max) = \frac{0.125}{2 \times 40\ \mu s(0.125 + 1)} = 1.39\ kHz$$

3.4.3 Practical Design Techniques

Now let us design a voltage comparator circuit with hysteresis and obtain the following performance:

1. Upper threshold	–4.25 volts
2. Lower threshold	–7.75 volts
3. Hysteresis	3.5 volts
4. Highest operating frequency	60 hertz
5. Maximum ratio (ρ) of switching time to stable time	0.1
6. Power supply voltages	±15 volts

Determine the Required Slew Rate. The slew rate must be high enough to allow the output to switch between saturation levels within the allowed switching time (t_S). The switching time is computed with Equation (3.12) as follows:

$$
\begin{aligned}
t_S &= \frac{\rho}{2(\rho + 1) \times f(\max)} \\
&= \frac{0.1}{2 \times 60\ Hz(0.1 + 1)} \\
&= 758\ \mu s
\end{aligned}
$$

For purposes of op amp selection, we can assume that the output swings between the two power supply limits. That is, assume that $\pm V_{SAT} = \pm V_{CC}$. The required slew rate can then be computed with Equation (3.13) as

$$\begin{aligned} \textit{slew rate}(\text{min}) &= \frac{2V^+}{t_S} \\ &= \frac{2 \times 15\ V}{758\ \mu s} \\ &= 0.04\ V/\mu s \end{aligned}$$

These calculations assume a 50-percent duty cycle on the output waveform. If the output is asymmetrical, then the shortest allowable alternation is given as

$$t_{MIN} = t_S\left(\frac{\rho + 1}{\rho}\right)$$

Select an Op Amp. Appendix 1 indicates that the slew rate for a 741 is 0.5 volts per microsecond, which exceeds our requirement of at least 0.04 volts per microsecond. The power supply requirements are also compatible with our stated design requirements. We will build our design around the 741 op amp.

Determine R_F and R_1. The ratio of R_F and R_1 is dependent on the ratio of V_{SAT} voltage to hysteresis voltage. Appendix 1 indicates that the lightly loaded ($R_L >$ 10 $k\Omega$) output swing will be typically ±14 volts. We will use this value for our computations. If the circuit is expected to drive a greater load (smaller load resistor and/or feedback network), then the output will be correspondingly smaller. The ratio of R_F to R_1 is computed with Equation (3.14).

$$\begin{aligned} \frac{R_F}{R_1} &= \frac{2V_{SAT}}{V_H} - 1 \\ &= \frac{2 \times 14\ V}{3.5\ V} - 1 \\ &= 7 \end{aligned}$$

We select R_1 and calculate the value of R_F. For purposes of this example, we select R_1 to be 33 kilohms. Having done this, we can now compute R_F by applying Equation (3.15) where the ratio (R_F/R_1) is known.

$$\begin{aligned} R_F &= \left(\frac{R_F}{R_1}\right)R_1 \\ &= 7 \times 33\ k\Omega \\ &= 231\ k\Omega \end{aligned}$$

We will select a standard value of 240 kilohms.

Calculate V_{REF}. A simple way to calculate the required value of V_{REF} is to apply Equation (3.18).

$$V_{REF} = V_{LT} + \frac{V_H}{2} \tag{3.18}$$

where V_{LT} and V_H are the lower threshold and hysteresis voltages, respectively. In our present case, we can determine V_{REF} as shown:

$$V_{REF} = -7.75\ V + \frac{3.5\ V}{2} = -6.0\ V$$

For purposes of illustration, let us derive this reference voltage from a zener diode network across the –15-volt supply. As long as the equivalent (Thevenin) resistance of the zener circuit is small compared to R_F and R_1 (the usual case), it will not affect our previous selection of components.

Appendix 5 shows the data sheet for a family of zener diodes. One of the listed devices is the 1N5233B, which is a 6.0-volt, ½-watt zener diode. The maximum zener current can be estimated by applying the power formula:

$$I_Z(\max) = \frac{P_Z}{V_Z} \tag{3.19}$$

where P_Z and V_Z are the power and voltage ratings of the zener. In the case of the 1N5233B, the maximum current is

$$I_Z(\max) = \frac{0.5\ W}{6\ V} = 83.3\ mA$$

This establishes the upper limit of zener current, and even this must be derated for temperatures above 25°C. The zener test current (I_{ZT}) is listed as 20 milliamps, which is generally a good quiescent current choice.

The series current limiting resistor for the zener regulator can be computed as follows:

$$R_S = \frac{V_{CC} - V_Z}{I_Z} \tag{3.20}$$

In the present case, we have

$$R_S = \frac{15\ V - 6\ V}{20\ mA} = 450\ \Omega$$

Finally, we will choose the standard value of 470 ohms, which completes our design. The final schematic is shown in Figure 3.12. The waveforms in Figure 3.13 reveal the performance of the circuit. The original design goals are contrasted with the measured performance in Table 3.2.

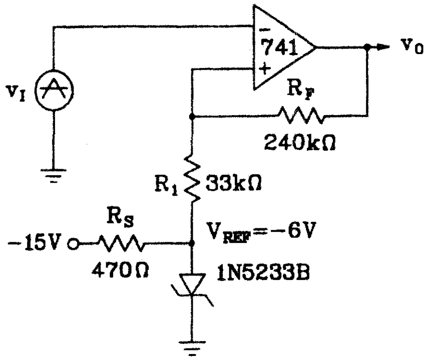
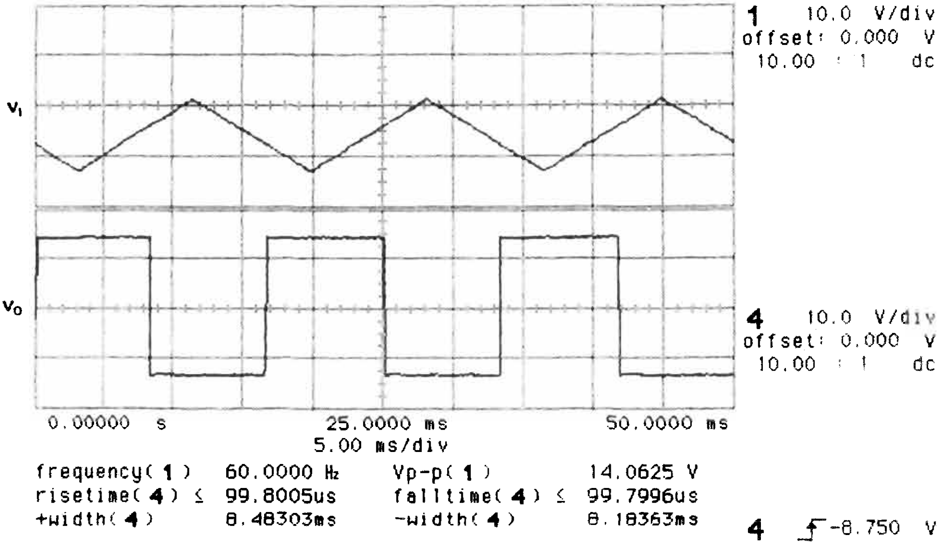


FIGURE 3.12 A voltage comparator design using a zener diode as the reference voltage.



```
frequency( 1 )    60.0000 Hz      Vp-p( 1 )        14.0625 V
risetime( 4 ) ≤   99.8005us       falltime( 4 ) ≤  99.7996us
+width( 4 )       8.48303ms       -width( 4 )      8.18363ms
```

FIGURE 3.13 Waveforms showing the performance of the circuit shown in Figure 3.12. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 3.2

	Design Goal	*Measured Value*
Upper threshold	−4.25 volts	−4.25 volts
Lower threshold	−7.75 volts	−7.813 volts
Hysteresis	3.5 volts	3.56 volts
Maximum switching ratio	0.02	0.012

3.5 WINDOW VOLTAGE COMPARATOR

3.5.1 Operation

A basic op amp window detector circuit, shown in Figure 3.14, is essentially a dual comparator circuit and produces a two-state output that indicates whether or not the input voltage (v_I) is between the limits (i.e., within the window) established by the $\pm V_{REF}$ voltages. It is frequently used to sound an alarm or signal a control circuit when a measured variable (v_I) goes outside of a preset range. The reference voltages in Figure 3.14 are established by two zener diode circuits.

To examine the operation of the circuit, let us start by assuming that the input voltage is within the window. That is, the input voltage is less than $+V_{REF}$ and greater than $-V_{REF}$. Under these conditions, the outputs of both op amps will be driven to the $+V_{SAT}$ level. This reverse-biases the two isolation diodes (D_3 and D_4) and allows the output (v_O) to rise to +15 volts, indicating an "in window" condition. (Note that if the positive saturation levels of the op amps are sufficiently low, the isolation diodes will not be reverse-biased but the output will still be at its most positive level.)

Now suppose that the input either exceeds $+V_{REF}$ or falls below $-V_{REF}$. In either of these cases, the output of one of the two op amps will go to the $-V_{SAT}$ level and forward-bias its associated isolation diode. This will cause the output of the circuit (v_O) to be pulled to −15 volts (ideally). In practice, the output voltage will be equal to the negative saturation level *plus* the forward voltage drop of the conducting isolation diode. This negative level indicates an "out of window" condition.

3.5.2 Numerical Analysis

Let us now analyze the behavior of the circuit shown in Figure 3.14 in greater detail. We shall determine the following characteristics:

1. $+V_{REF}$
2. $-V_{REF}$
3. Output voltage (v_O)

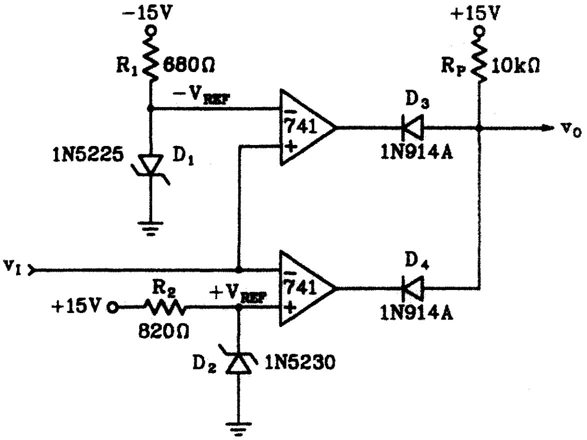


FIGURE 3.14 A window detector is used to determine whether the input voltage (v_I) is within the limits of $\pm V_{REF}$.

$+V_{REF}$. The value of $+V_{REF}$ is established by the 1N5230 zener diode. Appendix 5 indicates that this is a 4.7-volt zener, so $+V_{REF}$ is approximately +4.7 volts. If desired, we can determine the amount of zener current with Equation (3.20) (transposed):

$$\begin{aligned} I_Z &= \frac{+V_{CC} - V_Z}{R_2} \\ &= \frac{15\ V - 4.7\ V}{820\ \Omega} \\ &= 12.6\ mA \end{aligned}$$

$-V_{REF}$. The 1N5225 zener diode is used to establish the $-V_{REF}$ source. Appendix 5 lists the 1N5225 as a 3.0-volt zener. Its current can be calculated with Equation (3.20) (transposed) as

$$\begin{aligned} I_Z &= \frac{+V_{CC} - V_Z}{R_1} \\ &= \frac{15\ V - 3\ V}{680\ \Omega} \\ &= 17.6\ mA \end{aligned}$$

Output Voltage (v_O). The upper limit of v_O occurs when both of the isolation diodes are reverse-biased or effectively open. This means that the pull-up resistor (R_P) has essentially no current flow and therefore no voltage drop across it. Since R_P drops no voltage under these conditions, the output will be at a +15-volt level. As mentioned previously, if $+V_{SAT}$ is sufficiently low, the isolation diode will not be reverse-biased and the output voltage (v_O) will be less than +15 volts ($+V_{SAT} + V_F$, where V_F is the forward voltage drop of the diode).

If either of the op amp outputs is forced to its $-V_{SAT}$ level, then the associated isolation diode will be forward-biased. Appendix 1 indicates that the $-V_{SAT}$ will be about −11 volts. The current through R_P can now be estimated as follows:

$$I_{R_P} = \frac{V_{CC} - (-V_{SAT}) - V_F}{R_P} \tag{3.21}$$

where V_F is the forward voltage drop of the isolation diode (typically 0.7 volts). In our present case, we can compute I_{R_P} as

$$I_{R_P} = \frac{15\ V - (-11\ V) - 0.7\ V}{10\ k\Omega} = 2.53\ mA$$

The actual output voltage (v_O) under these conditions is determined as follows:

$$v_O = V_{CC} - I_{R_P} R_P \tag{3.22}$$

And, for the present circuit,

$$v_O = 15\ V - (2.53\ mA \times 10\ k\Omega) = -10.3\ V$$

This same result can be obtained by applying Kirchhoff's Voltage Law—that is,

$$\begin{aligned} v_O &= -V_{SAT} + V_F \\ &= -11\ V + 0.7\ V \\ &= -10.3\ V \end{aligned}$$

3.5.3 Practical Design Techniques

Let us now design a window detector to meet the following specifications:

1. Upper window limit	+10 volts
2. Lower window limit	+7.5 volts
3. Power supply	±15 volts
4. Input frequency	0 to 100 Hz

Select the Op Amp. Since the circuit is being driven by a very low-frequency source, the high-frequency characteristics of the op amp are unimportant to us. The DC stability of the op amp is more important in circuits like this and will be determined by the requirements of the application being considered. If the switching speed of the device is important for an application that has a higher input frequency, then you would do well to select an op amp that is specifically designed for fast comparator applications.

For purposes of our present example, let us choose the 741.

Select the Zener Diodes. Appendix 5 lists a family of zener diodes. The 1N5236 and 1N5240 devices will satisfy the requirements for our lower and upper reference voltages of 7.5 volts and 10 volts, respectively.

Calculate the Zener-Current Limiting Resistors. Unless we have some reason to do otherwise (e.g., ultra-low current designs), we can use the zener test current as the design value. Appendix 5 lists 20 milliamps as the test current for both diodes. Basic circuit theory, as given in Equation (3.20), allows us to compute the values of current limiting resistors.

$$\begin{aligned} R_1 &= \frac{V_{CC} - V_{REF}}{I_Z} \\ &= \frac{15\ V - 7.5\ V}{20\ mA} \\ &= 375\ \Omega \end{aligned}$$

We will choose a standard value of 390 ohms. In a similar manner,

$$R_2 = \frac{V_{CC} - V_{REF}}{I_Z}$$
$$= \frac{15\ V - 10\ V}{20\ mA}$$
$$= 250\ \Omega$$

We choose the next higher standard value of 270 ohms. Note that in this particular case, both zeners will be connected across the positive supply voltage because we require both references to be positive.

Select R_P. The correct value of R_P is determined by two primary considerations:

1. Current capability of the driving op amps
2. Type of circuit or device being driven

Since we have no information regarding the driven circuit, let us select R_P such that the op amp output current is limited to 5 milliamps. This calculation, from Equation (3.21), is based on Ohm's Law as follows:

$$R_P = \frac{V_{CC} - (-V_{SAT}) - V_F}{I_{R_P}}$$
$$= \frac{15\ V - (-11\ V) - 0.7\ V}{5\ mA}$$
$$= 5.06\ k\Omega$$

Let us select the next higher standard value of 5.1 kilohms.

Select the Isolation Diodes. The requirements for the isolation diodes are not stringent. The two primary parameters that need to be considered are

1. Reverse voltage breakdown
2. Maximum forward current

The maximum current is the same as the value of the op amp output current. In our case, we have designed this to be 5 milliamps. The maximum reverse voltage (ignoring diode drops) is approximately equal to the difference between $+V_{SAT}$ of one op amp and $-V_{SAT}$ of the other. That is,

$$V_{PRV} = +V_{SAT} - (-V_{SAT}) \tag{3.23}$$

More specifically,

$$V_{PRV} = 11\ V - (-11\ V) = 22\ V$$

Appendix 6 shows the characteristics for a 1N914A diode. Almost any diode will satisfy our modest requirements. The 1N914A is a standard, low-cost diode that we can use for this application.

This completes the design of the window detector circuit. The final schematic is shown in Figure 3.15. Figure 3.16 shows the actual waveforms produced by the circuit. Table 3.3 compares the original design goals with the measured circuit performance.

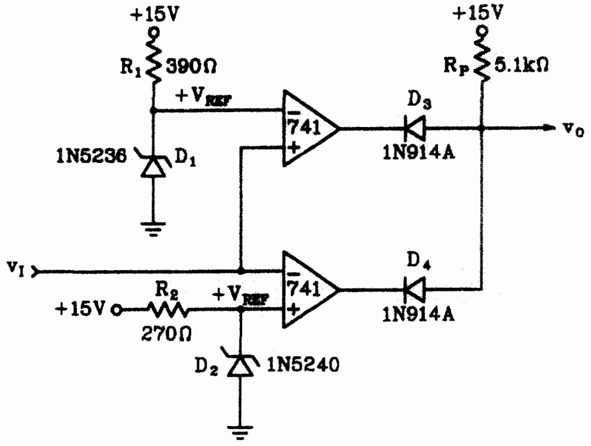

+15V
R_1
390Ω
$+V_{REF}$
1N5236
D_1
741
+15V
R_P
5.1kΩ
D_3
1N914A
V_O
V_I
+15V
R_2
270Ω
$+V_{REF}$
741
D_4
1N914A
D_2
1N5240

FIGURE 3.15 A window detector designed for a lower limit of +7.5 volts and an upper limit of +10 volts

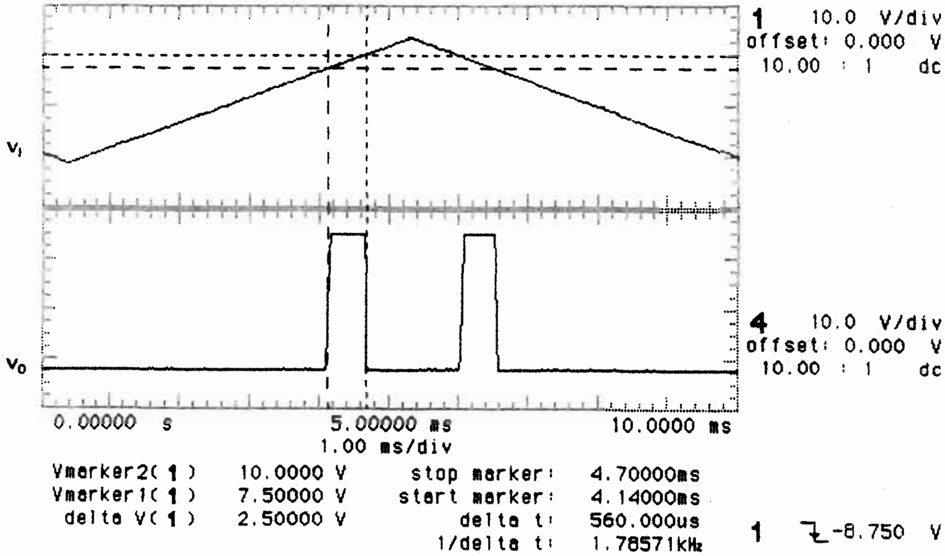


FIGURE 3.16 Oscilloscope displays showing the performance of the circuit in Figure 3.15. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 3.3

	Design Goal	*Measured Value*
Upper window limit	+10 volts	+10 volts
Lower window limit	+7.5 volts	+7.5 volts

3.6 VOLTAGE COMPARATOR WITH OUTPUT LIMITING

3.6.1 Operation

The voltage comparator shown in Figure 3.17 is configured to be noninverting. Additionally, the output uses two zener diodes (D_2 and D_3) to limit the swing of v_O. The zener pair, along with resistor R_1, acts like a bidirectional, biased limiter circuit. D_1 and current limiting resistor R_S establish the reference voltage. Feedback resistor R_F, in conjunction with R_I, establishes hysteresis for the circuit.

For purposes of discussion, let us assume that the input is well below the upper threshold voltage. Since this is a noninverting circuit, we know that the output of the op amp will be driven to the $-V_{SAT}$ level. The zener pair in the output circuit, along with R_1, regulates the $-V_{SAT}$ voltage to a value established by D_3. This reduced and regulated voltage appears as v_O.

Resistors R_F and R_I form a voltage divider that appears between the regulated v_O and the changing input voltage. The circuit will remain in this stable condition as long as the (+) input of the op amp remains lower than the reference voltage on the (–) input.

As the input voltage increases, the voltage on the (+) input also increases. Once the (+) input goes above the voltage on the (–) input, even momentarily, the output of the op amp will go toward the $+V_{SAT}$ level. This rising potential, through R_F, further increases the potential on the (+) input pin. With the output of the op amp at the $+V_{SAT}$ level, diode D_2 establishes the value of voltage at v_O. Again, the circuit will remain in this state until the voltage on the (+) input falls below the

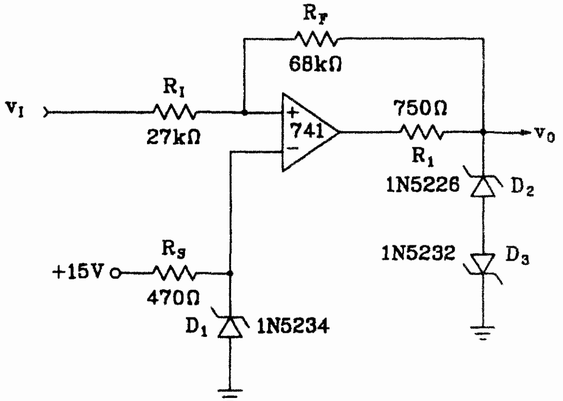


FIGURE 3.17 A voltage comparator with output limiting.

voltage on the (–) terminal. Note that because the rising output has increased the potential on the (+) input, the actual input voltage (v_I) will have to go to a much lower level to cause the circuit to switch states. This effect is, of course, the very nature of hysteresis.

If the input voltage now decreases to a level that causes the voltage on the (+) pin to fall below the voltage on the (–) pin, then the circuit will switch back to its original state.

3.6.2 Numerical Analysis

Now let us extend our analysis of Figure 3.17 to calculate the following:

1. Upper threshold voltage
2. Lower threshold voltage
3. Hysteresis
4. All zener currents
5. Output voltage limits (v_O^+ and v_O^-)

Upper Threshold Voltage. The upper threshold voltage can be found by applying Kirchhoff's Law and basic circuit theory to the resistor network R_I and R_F. Our knowledge of op amp operation tells us that no substantial current enters or leaves the (+) pin. Therefore, $i_1 = i_2$ in Figure 3.18. At the instant v_I reaches the upper threshold, the junction of R_F and R_I will just equal V_{REF}. This is so labeled on Figure 3.18.

Using Ohm's Law, we can write expressions for the values of i_1 and i_2:

$$i_1 = \frac{v_I - V_{REF}}{R_I}$$

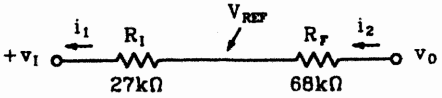
$$i_2 = \frac{V_{REF} - v_O^-}{R_F}$$

If we equate these two currents, we get

$$i_1 = i_2$$

$$\frac{v_I - V_{REF}}{R_I} = \frac{V_{REF} - v_O^-}{R_F}$$

FIGURE 3.18 Basic circuit theory can be used to compute the upper threshold voltage of the circuit in Figure 3.17.



Some algebraic manipulation gives us the expression for v_I at the moment it reaches the upper threshold:

$$v_I = V_{UT} = \frac{R_I(V_{REF} - v_O^-)}{R_F} + V_{REF} \qquad (3.24)$$

In the present example, v_O^- equals the voltage of D_3 (–5.6 volts as listed in Appendix 5) during this period of time. The reference voltage is 6.2 volts (see Appendix 5). Substituting values enables us to calculate the value of the upper threshold voltage:

$$V_{UT} = 27\ k\Omega\left(\frac{6.2\ V - (-5.6\ V)}{68\ k\Omega}\right) + 6.2\ V = 10.9\ V$$

This value can be made slightly more accurate by including the effects of the forward voltage drop of D_2 (about 0.7 volts). That is, v_O^- will equal the voltage of D_3 plus the forward voltage drop of D_2, or –6.3 volts. If this effect is included, the threshold is computed to be 11.2 volts.

Lower Threshold Voltage. A similar application of basic circuit theory when the output is at the $+V_{SAT}$ level and the input is approaching the lower threshold voltage yields the following expression for the lower threshold voltage:

$$V_{LT} = V_{REF} - \frac{R_I(v_O^+ - V_{REF})}{R_F} \qquad (3.25)$$

Recognizing that v_O^+ will be equal to the voltage of D_2 (3.3 volts) during this time, we can calculate the value of lower threshold voltage:

$$V_{LT} = 6.2\ V - \frac{27\ k\Omega(3.3\ V - 6.2\ V)}{68\ k\Omega} = 7.35\ V$$

If the forward voltage drop of D_3 is included in the calculation, the threshold voltage will be computed as 7.07 volts.

Hysteresis. Hysteresis is simply the difference between the two threshold voltages. In our present case, hysteresis is computed as shown in Equation (3.6):

$$\begin{aligned} V_H &= V_{UT} - V_{LT} \\ &= 10.9\ V - 7.35\ V \\ &= 3.55\ V \end{aligned}$$

If the diode drops are included, the hysteresis will be computed as 4.13 volts.

Zener Currents. The current through D_1 can be computed from Equation (3.20) as follows:

$$\begin{aligned} I_{D_1} &= \frac{+V_{CC} - V_{D_1}}{R_S} \\ &= \frac{15\ V - 6.2\ V}{470\ \Omega} \\ &= 18.7\ mA \end{aligned}$$

The reverse current through D_3 is computed with the following expression:

$$I_{D_3} = \frac{-V_{SAT} - V_{D_3} + 0.7}{R_1} \tag{3.26}$$

Continuing with the calculations, we get

$$I_{D_3} = \frac{-11\ V - (-5.6\ V) + 0.7\ V}{750\ \Omega} = -6.27\ mA$$

Note that the minus sign simply indicates direction and is of no significance to us at this time. D_2 current is computed in a similar manner as shown:

$$I_{D_2} = \frac{+V_{SAT} - V_{D_2} - 0.7}{R_1} \tag{3.27}$$

Substituting values for the present circuit gives us

$$I_{D_2} = \frac{11\ V - 3.3\ V - 0.7\ V}{750\ \Omega} = 9.33\ mA$$

The power dissipation of the zeners can be found by applying the basic power equation $P = IV$, where I and V are the current and voltages associated with a particular zener. In our particular case,

$$\begin{aligned} P_{D_1} &= 18.7\ mA \times 6.2\ V = 116\ mW \\ P_{D_2} &= 6.27\ mA \times 5.6\ V = 35.1\ mW \\ P_{D_3} &= 9.33\ mA \times 3.3\ V = 30.8\ mW \end{aligned}$$

Output Voltage Limits. The output voltage swing was essentially determined in a prior step. The upper excursion is established by the zener voltage of D_2 plus the forward voltage drop of D_3. In our case,

$$v_O^+ = V_{D_2} + 0.7\ V = 3.3\ V + 0.7\ V = 4.0\ V$$

The lower limit of v_O is computed as

$$v_O^- = V_{D_3} - 0.7\ V = -5.6\ V - 0.7\ V = -6.3\ V$$

3.6.3 Practical Design Techniques

We will now design a voltage comparator with output limiting that satisfies the following specifications:

1. Upper output voltage (v_O^+)	+5.0 volts
2. Lower output voltage (v_O^-)	−4.0 volts
3. Upper threshold voltage	+2.0 volts
4. Lower threshold voltage	+0.8 volts
5. Power supply	±15 volts
6. Op amp	741

These specifications (i.e., input and output requirements) would normally be dictated by the application.

Compute Hysteresis Voltage. Our first step will be to calculate the required hysteresis voltage. This is, very simply, the difference between the two threshold voltages from Equation (3.6).

$$\begin{aligned} V_H &= V_{UT} - V_{LT} \\ &= 2\ V - 0.8\ V \\ &= 1.2\ V \end{aligned}$$

Compute R_F and R_I. The ratio of R_F to R_I is determined by the ratio of the output voltage swing to the hysteresis voltage. That is,

$$\boxed{\frac{R_F}{R_I} = \frac{v_O^+ - v_O^-}{V_H} \qquad (3.28)}$$

In our design example, the required R_F/R_I ratio is computed as shown:

$$\frac{R_F}{R_I} = \frac{5\ V - (-4\ V)}{1.2\ V} = 7.5$$

We will now select R_I and compute R_F. We will choose 10 kilohms for resistor R_I. The feedback resistor R_F can now be computed, from Equation (3.15), as shown:

$$\begin{aligned} R_F &= \left(\frac{R_F}{R_I}\right) R_I \\ &= 7.5 \times R_I \\ &= 7.5 \times 10\ k\Omega \\ &= 75\ k\Omega \end{aligned}$$

The factor 7.5 in the above equation is simply the R_F/R_I ratio previously computed.

Select the Output Zener Diodes. The voltage rating of the two zener diodes is determined by the stated output voltage swing. That is,

$$V_{D_2} = v_O^+ - 0.7 \tag{3.29}$$

Substituting values gives us

$$V_{D_2} = 5\ V - 0.7\ V = 4.3\ V$$

Similarly, the voltage rating for D_3 is computed as

$$V_{D_3} = v_O^- + 0.7 \tag{3.30}$$

Values for the present circuit are

$$V_{D_3} = -4\ V + 0.7\ V = -3.3\ V$$

The power ratings for the zeners are not critical, but must be noted for subsequent calculations. By referring to Appendix 5, we can select a 1N5229 and a 1N5226 for diodes D_2 and D_3, respectively. We also observe that both of these diodes are rated at 500 milliwatts.

Compute R_1. Resistor R_1 is a current limiting resistor for the zener diodes. First, we will compute the maximum allowable currents through each of the zeners, using Equation (3.19).

$$\begin{aligned} I_{D_2} &= \frac{P_{D_2}}{V_{D_2}} \\ &= \frac{0.5\ W}{4.3\ V} \\ &= 116\ mA \end{aligned}$$

Similarly,

$$
\begin{aligned}
I_{D_3} &= \frac{P_{D_3}}{V_{D_3}} \\
&= \frac{0.5\ W}{3.3\ V} \\
&= 152\ mA
\end{aligned}
$$

Since both of these exceed the short-circuit output current of the 741, we will have to limit the current well below the maximum amount. Let us plan to limit it to 5 milliamps.

Next we compute the minimum values for R_1 in order to limit the diode currents to the desired value by applying Ohm's Law. The minimum value as dictated by D_2 is found, from Equation (3.20), to be

$$
\begin{aligned}
R_1(1) &= \frac{+V_{SAT} - V_{D_2}}{I_{D_2}} \\
&= \frac{13\ V - 4.3\ V}{5\ mA} \\
&= 1.74\ k\Omega
\end{aligned}
$$

Similarly, the value required to limit the current through D_3 is computed as

$$
\begin{aligned}
R_1(2) &= \frac{-V_{SAT} - V_{D_3}}{I_{D_3}} \\
&= \frac{-13\ V - (-3.3\ V)}{5\ mA} \\
&= 1.94\ k\Omega
\end{aligned}
$$

The larger of these two values (1.94 kilohms) sets the lower limit on R_1. We will select the next higher standard value of 2 kilohms for R_1.

Select the Reference Zener Diode. The required reference voltage can be determined by using the following equation:

$$
\boxed{V_{REF} = \frac{V_{UT}R_F + R_I v_{\overline{O}}}{R_I + R_F} \qquad (3.31)}
$$

In our present design, the required reference is calculated as follows:

$$
V_{REF} = \frac{2\ V \times 75\ k\Omega + 10\ k\Omega \times (-4\ V)}{10\ k\Omega + 75\ k\Omega} = 1.29\ V
$$

A brief scan of Appendix 5 reveals that it may be very difficult to locate a 1.3-volt zener. Let us rely on our knowledge of basic semiconductors to discover an alternative. Recall that a forward-biased silicon diode has about 0.6 to 0.7 volts and remains fairly constant. We can obtain the equivalent of a 1.3-volt zener by using two series silicon diodes. Appendix 6 lists the data for 1N914A diodes. A 1N914A diode will have about 0.64 volts across it with a forward current of 0.25 milliamps. Similarly, this same diode will have about 0.74 volts across it with a forward current of 1.5 milliamps. Let us select 1N914A diodes for our application and establish a forward current of about 0.5 milliamps.

Determine the Value of R_S. The purpose of resistor R_S is to limit the current through reference diode D_1. In our case, it will limit the current through two series 1N914A diodes. The value of R_S is computed, from Equation (3.20), as follows:

$$R_S = \frac{V^+ - V_{REF}}{I_{REF}}$$

where I_{REF} is the specified current through the reference diode. For our design, R_S is calculated as shown:

$$R_S = \frac{15\ V - 1.3\ V}{0.5\ mA} = 27.4\ k\Omega$$

We will choose the standard value of 27 kilohms for R_S.

This completes the design of our voltage comparator with output limiting. The final schematic is shown in Figure 3.19, and the actual performance of the circuit is shown in Figure 3.20 by means of oscilloscope displays. The design goals are contrasted with the measured circuit values in Table 3.4.

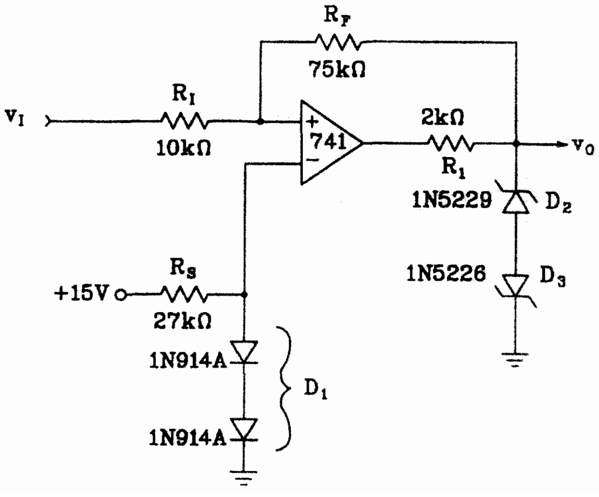
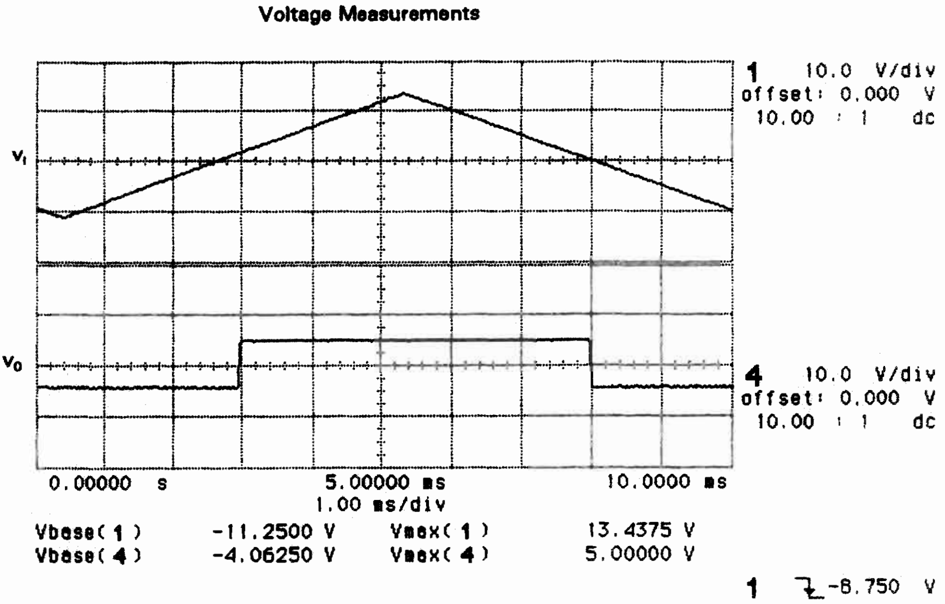


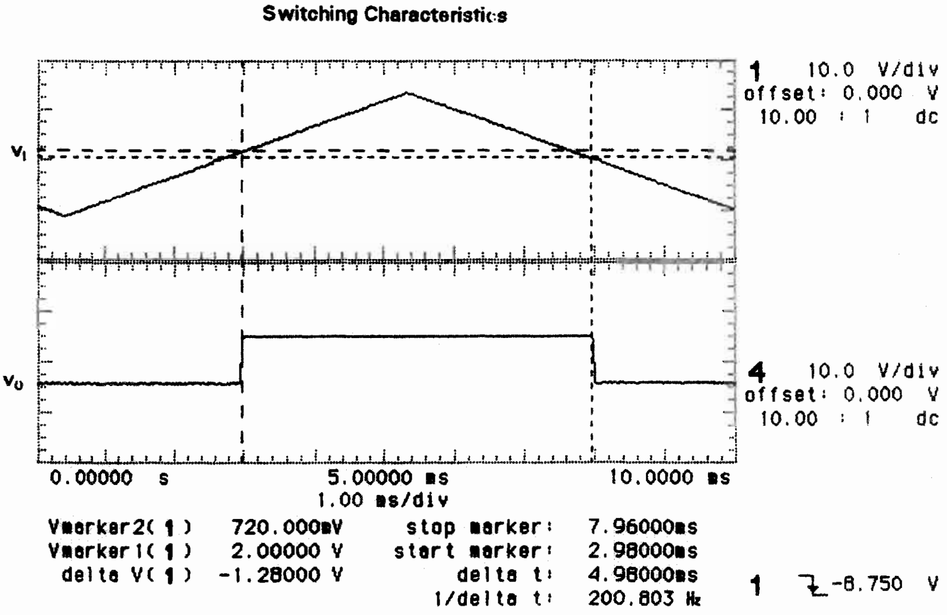
FIGURE 3.19 Final design for a comparator with output limiting.



Voltage Measurements

```
Vbase( 1 )   -11.2500 V    Vmax( 1 )    13.4375 V
Vbase( 4 )   -4.06250 V    Vmax( 4 )    5.00000 V
```

(a)



Switching Characteristics

```
Vmarker2( 1 )  720.000mV     stop marker:  7.96000ms
Vmarker1( 1 )  2.00000 V    start marker:  2.98000ms
 delta V( 1 ) -1.28000 V         delta t:  4.98000ms
                               1/delta t:  200.803 Hz
```

(b)

FIGURE 3.20 Oscilloscope displays showing the behavior of the comparator in Figure 3.19. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 3.4

	Design Goal	*Measured Value*
Output voltage (+)	+5.0 volts	+5.0 volts
Output voltage (–)	–4.0 volts	–4.06 volts
Upper threshold voltage	+2.0 volts	+2.0 volts
Lower threshold voltage	+0.8 volts	+0.77 volts

3.7 TROUBLESHOOTING TIPS FOR VOLTAGE COMPARATORS

Comparator circuits are generally some of the easier op amp circuits to troubleshoot, provided you pay close attention to the symptoms and keep the basic theory of operation in mind at all times. If the circuit worked properly at one time (i.e., it does not have design flaws), then the symptoms of the malfunction will normally fall into one of the following categories:

1. Output is driven to one extreme ($\pm V_{SAT}$) regardless of the input signal.
2. Switching levels (input, output, or both) are wrong.

Output Saturated. It is always a good first check to verify the power supply voltages. A missing supply can cause the output to go to the opposite extreme.

If the power supplies are both correct, then compare the voltage readings on the (+) and (–) inputs of the op amp. If the polarity on the two inputs periodically switches (i.e., one input becomes more positive than the other and then later changes so that it is less positive than the other), then the op amp is a likely suspect. That is, the inputs **directly on the op amp** are telling the device to switch and the op amp has the correct power source, yet the output remains in saturation. The op amp is the most probable trouble.

If, on the other hand, the (+) and (–) input terminal measurements reveal that one of the inputs is always more positive than the other, then the op amp is not being told to change states. In this case, you should check the input signal for proper voltage levels. Pay particular attention to any DC offset signals that may be present. A DC offset at the input can shift the entire operation so far off center that the input signal cannot cause the op amp to switch.

If the input signal is correct, verify the proper voltage on the reference input. If this is incorrect, the problem lies in the reference circuit (i.e., voltage divider, zener diode, etc.).

If both the input signal and the reference voltages are correct but one of the input pins continues to be more positive than the other at all times, measure the output of the op amp (particularly in circuits with output limiting). Although the output is at an extreme voltage, determine if the extreme voltage is one of the expected levels (e.g., a proper zener voltage) or some higher voltage. If the level is incorrect (i.e., too high), then suspect one of the zener diodes in the output.

Incorrect Switching Levels. Although there are many things that can cause minor shifts in switching levels (e.g., component value drifts), some are more probable than others. If the circuit has adjustable components, such as a variable reference voltage, suspect this first. If the variable components are properly adjusted but the problem remains, suspect any solid-state components other than the op amp (e.g., zener diodes).

The zeners can be checked for proper operation by measuring the voltage across them. A forward-biased zener will drop about 0.7 volts; a reverse-biased zener should have a voltage drop that is approximately equal to its rated voltage. Keep in mind that zeners are not precision devices. For example, a 5.6-volt zener that drops 6 volts is probably not defective.

As a last resort, verify the resistance values. Resistor tolerances in a low-power circuit of this type do not present problems very often.

3.8 NONIDEAL CONSIDERATIONS

For many comparator applications, slew rate is the primary nonideal parameter that must be considered. This limitation was discussed in earlier sections, along with methods for determining the effects of a finite slew rate. Additionally, the zener diodes become less ideal as the input frequency is increased.

Throughout the earlier sections of this chapter, it was assumed that the op amp changed states whenever the differential input voltage passed through 0. The input bias current for the op amp, however, can cause the actual switch point to be slightly above or below 0. This problem is minimized by keeping the resistance between the (−) input to ground equal to the resistance between the (+) input and ground.

Input offset voltage is another nonideal op amp parameter that can affect the switching points of the comparator. The effect of a non-0 input offset voltage can be canceled by utilizing the offset null terminals (discussed in Chapter 10). Appendix 4 illustrates the proper way to utilize the null terminals on an MC1741SC op amp. Note, however, that different op amps use different techniques for nulling the effects of input offset voltage. Therefore, you must refer to the manufacturer's data sheet for each particular op amp.

The errors caused by the input bias currents and the input offset voltage can be totally eliminated by utilizing the nulling terminals. Unfortunately, however, the required level of compensation varies with temperature. Thus, although you may completely cancel the nonideal effects at one temperature, the effects will likely return at a different temperature. For many, if not most, comparator applications, this latter drift does not present severe problems. If the application demands greater stability, an op amp that offers optimum performance in these areas should be initially selected.

REVIEW QUESTIONS

1. Refer to Figure 3.7. Which component(s) is (are) used to determine the threshold voltages?
2. Refer to Figure 3.9. If resistor R_1 develops a short circuit, describe the effect on circuit operation. Will there still be a rectangular wave on the output pin?
3. Refer to Figure 3.9. If resistor R_F is reduced in value, describe the relative effect on the circuit hysteresis.
4. Refer to Figure 3.7. If resistor R_1 is changed to 68 kilohms, what is the value for the upper threshold voltage? Does this resistor change affect the circuit hysteresis ($V_{SAT} = 10V$)?
5. Refer to Figure 3.14. If resistor R_1 is reduced in value (and no components are damaged), what is the effect on the negative threshold (assume ideal zeners)?
6. Refer to Figure 3.14. If diode D_3 becomes open, describe the effect on circuit operation.
7. Refer to Figure 3.15. Describe the effect on circuit operation if diode D_1 develops a short circuit.
8. Refer to Figure 3.17. What is the purpose of R_S? Will the circuit still appear to operate correctly if R_S is reduced to one-half its original value as long as no components are damaged? Explain.
9. Sketch a simple graph of voltage versus time that illustrates the relationship between the voltages at the following points in Figure 3.17: v_I, v_O, and the output pin of the op amp. Be sure to indicate relative voltage amplitudes and phase relationships.
10. Refer to Figure 3.19. What is the effect on circuit operation if R_S is returned to a +20-volt supply instead of the +15-volt source shown in the figure?

CHAPTER FOUR

Oscillators

4.1 OSCILLATOR FUNDAMENTALS

An oscillator is essentially an amplifier that produces its own input. That is, if we connect an oscillator circuit to a DC power supply, it will generate a signal without having a similar signal available as an input. One of the most fundamental ways to classify oscillator circuits is by the shape of the waveform generated. In this chapter, we will study oscillator circuits that produce waveforms such as sinewave, rectangular wave, ramp wave, and triangular wave.

In general, in order for a circuit to operate as an oscillator, three basic factors must be provided in the circuit. They are

1. Amplification
2. Positive feedback
3. Frequency determining network

Suppose that many random signal frequencies (e.g., noise voltages) are present at the input of the amplifier shown in Figure 4.1. All of these frequencies are amplified by the amplifier and then enter the frequency selective circuit. This portion of the circuit normally introduces a loss or reduction in signal amplitude. Essentially, all frequencies can enter the frequency determining network, but only a single frequency (ideally) is allowed to pass through. In practice, a narrow band of frequencies can pass with minimal attenuation. The narrower the passband of frequencies, the more stable the output frequency of the oscillator.

Once the desired signal emerges from the frequency selective portion of the circuit, it is returned to the input of the amplifier. The amplifier compensates for losses in the frequency selective portion of the circuit. The overall closed-loop gain of the circuit must be at least 1 (unity) in order for the circuit to sustain oscillation. If the overall loop gain is less than 1, the oscillations quickly decay (ringing at best); If it exceeds unity, then the amplitude of the output signal will continue to increase until saturation is reached. If the circuit is intended to produce

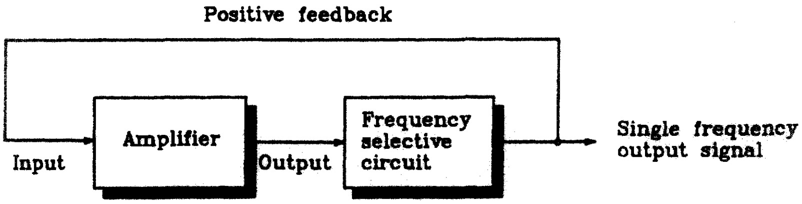

Positive feedback
Input
Amplifier
Output
Frequency selective circuit
Single frequency output signal

FIGURE 4.1 An oscillator circuit requires amplification, frequency selection, and positive feedback to operate.

sinewaves, the loop gain must be set to unity in order to maintain a constant-amplitude, undistorted output signal.

4.2 WIEN-BRIDGE OSCILLATOR

4.2.1 Operation

Figure 4.2 shows the schematic diagram of a Wein-bridge oscillator circuit built around a 741 op amp. A Wien-bridge oscillator produces sinewaves and uses an RC network as the frequency-determining portion of the circuit. The amplification is, of course, provided by the op amp, which is essentially connected as a noninverting amplifier circuit similar to those discussed in Chapter 2. The gain of the op

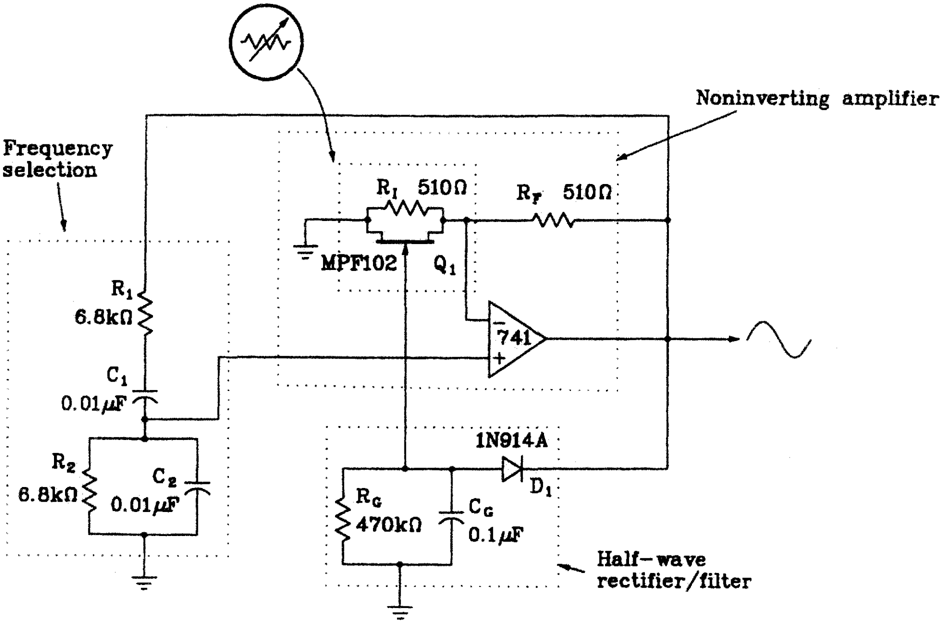

Noninverting amplifier
Frequency selection
R₁ 6.8kΩ
C₁ 0.01μF
R₂ 6.8kΩ
C₂ 0.01μF
R_I 510Ω
R_F 510Ω
MPF102
Q₁
741
1N914A
D₁
R_G 470kΩ
C_G 0.1μF
Half-wave rectifier/filter

FIGURE 4.2 A FET-stabilized Wien-bridge oscillator circuit.

amp portion of the circuit is determined by the ratio of the feedback resistor (R_F) and the effective resistance of the field-effect transistor (FET) in parallel with R_I. The FET's resistance is determined by the amount of bias voltage on the gate. As the voltage on the gate becomes more negative, the channel resistance in the FET is increased.

The gate voltage for the FET is obtained from the output of a half-wave rectifier and filter combination. The input to the rectifier is provided by the output of the oscillator. In short, if the output amplitude tried to increase, the output of the rectifier circuit would become more negative. This increased negative voltage would bias the FET more toward cutoff (i.e., higher channel resistance). The increased FET resistance would cause the gain of the op amp circuit to decrease and thus prevent the output amplitude from increasing. A similar, but opposite, effect would occur if the output amplitude tried to decrease.

The output signal is also returned to the (+) input terminal (positive feedback) via the R_1C_1 and R_2C_2 network. This is the frequency selective portion of the oscillator. At the desired frequency of oscillation, the RC network will have a voltage gain of one-third and a phase shift of zero (i.e., no phase shift). At all other frequencies, the loss will be even greater and the input/output signals will differ in phase.

Now, if the amplifier portion of the circuit can provide a gain of 3 and the frequency selective portion of the circuit has a gain (actually a loss) of ⅓, then the overall closed-loop gain will be 1, or unity, **at the frequency of oscillation.** We now have the conditions necessary for oscillation. Additionally, since the gain of the amplifier is self-adjusting because of Q_1, we also have the conditions necessary for a stable output amplitude.

4.2.2 Numerical Analysis

Let us now analyze the Wien-bridge oscillator circuit shown in Figure 4.2 in greater detail. The most important characteristic to be evaluated is the frequency of operation. This is solely determined by the R_1C_1 and R_2C_2 networks. Although oscillators can be made with unlike values of resistance and capacitance, using equal values for the resistors and equal values for the capacitors in the R_1C_1 and R_2C_2 networks is the general practice. This greatly simplifies the design and analysis of the Wien-bridge oscillator. When equal sets of values are used for the bridge, the frequency of oscillation is given by Equation (4.1).

$$\boxed{f_O = \frac{1}{2\pi RC} \qquad (4.1)}$$

In the case of the circuit in Figure 4.2, the frequency of operation is computed as

$$f_O = \frac{1}{6.28 \times 6.8\ k\Omega \times 0.01\ \mu F} = 2.34\ kHz$$

The voltages at the various points in the circuit are not readily computed because they are highly dependent on the specific FET being used in the circuit. We know from our basic oscillator theory that the amplifier must have a voltage gain of 3 at the frequency of oscillation. Because the amplifier is configured as noninverting, we can compute the voltage gain as we did in Chapter 2.

$$A_V = \frac{R_F}{R_{IN}} + 1, \textit{ or}$$

$$R_{IN} = \frac{R_F}{A_V - 1}$$

$$= \frac{510\ \Omega}{3 - 1}$$

$$= 255\ \Omega$$

In the present case, however, R_{IN} is the effective resistance of R_I in parallel with the FET. The effective resistance of the FET can be computed with our basic parallel resistance formula.

$$R_{IN} = \frac{R_I R_{FET}}{R_I + R_{FET}}, \textit{ or}$$

$$R_{FET} = \frac{R_{IN} R_I}{R_I - R_{IN}}$$

$$= \frac{255\ \Omega \times 510\ \Omega}{510\ \Omega - 255\ \Omega}$$

$$= 510\ \Omega$$

Now we know that the channel resistance of the FET will be 510 ohms during oscillation. How does it get to that value? Well, the output of the op amp will be as large as necessary to produce the exact DC level at the gate of the FET that is needed to cause the 510-ohm channel resistance. Unfortunately, the parameters of the FET vary considerably (see Appendix 7) and can only be estimated for a particular device. The manufacturer's data sheet (Appendix 7) gives the value of $V_{GS(OFF)}$ as a maximum of 8 volts. In order to bias the FET in the "resistive" range (i.e., below the knee of the I_D versus V_{DS} curve), the gate voltage will generally be 25 percent of $V_{GS(OFF)}$ or less. In the case of Figure 4.2, we can anticipate a gate voltage of 2 volts or less, which, of course, restricts our peak output voltage to about 2.7 volts because the output actually produces the FET's gate voltage via the rectifier circuit (D_1). If we try to generate significantly higher voltages, then we can anticipate a distorted output because we will be operating past the knee of the FET curve.

4.2.3 Practical Design Techniques

Now let us design a Wien-bridge oscillator circuit that will perform according to the following design goals:

1. Frequency of oscillation	10.5 kHz
2. Available FET	MPF102

Compute the Frequency Determining Values. We will base our design on the accepted practice that $R_1 = R_2 = R$ and $C_1 = C_2 = C$. We will choose a value for C and compute the associated value for R. The initial selection of C is somewhat arbitrary, but will generally produce good results with values at least 100 times greater than the input capacitance of the op amp. For our present example, let us choose an initial capacitance value of 1000 picofarads. We can now compute the required value of R with Equation (4.1).

$$\begin{aligned} f_O &= \frac{1}{2\pi RC}, \textit{ or} \\ R &= \frac{1}{2\pi C f_O} \\ &= \frac{1}{6.28 \times 1000\ pF \times 10.5\ kHz} \\ &= 15.2\ k\Omega \end{aligned}$$

We will choose a standard value of 15 kilohms. If the computed value of R is below 1 kilohm or greater than 470 kilohms, you might want to select a different value for C and recompute R.

Compute R_F and R_I. R_F and R_I are selected to produce **both** of the following conditions:

1. When the FET is biased off, the gain of the op amp will be less than 3.
2. When the FET is in its "resistive" range, the gain of the op amp can exceed 3.

We will compute R_I as follows:

$$\boxed{R_I = \frac{V_{GS(off)}}{I_{DSS}(\text{max})} \qquad (4.2)}$$

In our present case, we compute R_I as

$$R_I = \frac{8\ V}{20\ mA} = 400\ \Omega$$

Let us select a standard value of 390 ohms for R_I. We will set R_F to be equal to R_I. That is,

$$\boxed{R_F = R_I \qquad (4.3)}$$

More specifically,

$$R_F = 390\ \Omega$$

This ensures that conditions for oscillation will be met.

Compute Rectifier and Filter Components. The R_GC_G network is a filter for the half-wave rectifier circuit. As with any basic rectifier circuit, the time constant of the filter should be long relative to the period of the input signal. In the case of the circuit shown in Figure 4.2, the input signal is the basic oscillator frequency (f_O). Thus, the R_GC_G time constant is computed as

$$R_GC_G = \frac{100}{f_O} \tag{4.4}$$

In this particular case, the required RC time constant is computed as

$$R_GC_G = \frac{100}{10.5\ kHz} = 9.52\ ms$$

Let us select a value for R_G and compute the associated value for C_G. The value for R_G is not critical, but it is generally in the range of 10 kilohms to 1 megohm. Let us select 270 kilohms as that value. Capacitor C_G can now be computed using Equation (4.4).

$$\begin{aligned} R_GC_G &= \frac{100}{f_O},\ or \\ C_G &= \frac{100}{R_Gf_O} \\ &= \frac{100}{270\ k\Omega \times 10.5\ kHz} \\ &= 0.035\ uF \end{aligned}$$

We will choose a standard value of 0.039 μF.

The rectifier diode can be any general-purpose diode capable of withstanding the currents and voltages present in this application. Although the actual voltages and currents will be less, the following provides an easy and conservative computation for diode selection:

$$V_{PIV} = +V_{SAT} - (-V_{SAT}) \tag{4.5}$$

where V_{PIV} is the minimum reverse voltage breakdown rating for the diode. Also,

$$I_F = \frac{-V_{SAT}}{R_G} \tag{4.6}$$

where I_F is the maximum average forward current rating for the diode. Let us select a 1N914A for this example. The data for this diode is listed in Appendix 6.

Select the Op Amp. The two most significant considerations regarding op amp selection are unity gain frequency (bandwidth) and slew rate. The minimum required unity gain frequency can be estimated with the following equation:

$$f_{UG} = 30 f_O \tag{4.7}$$

In our particular example, the minimum required unity gain frequency is

$$f_{UG} = 30 \times 10.5\ kHz = 315\ kHz$$

The minimum required slew rate for our op amp can be estimated from the following equation:

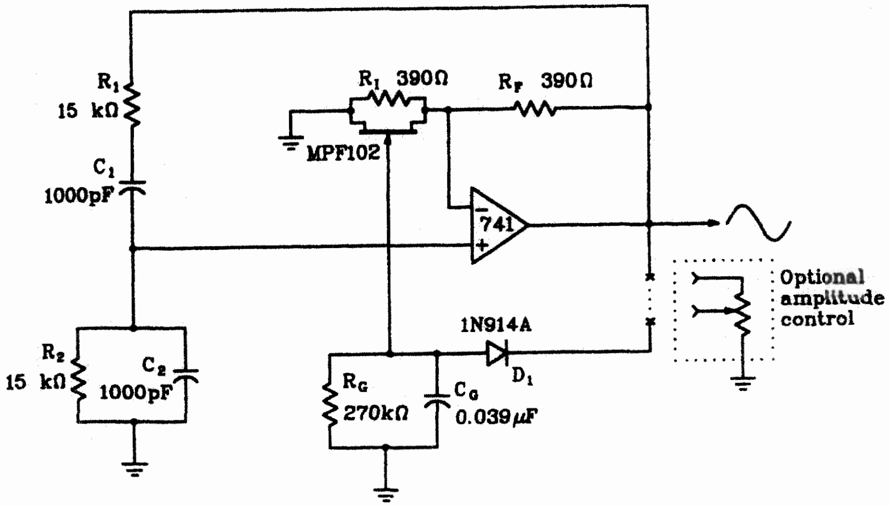
$$slew\ rate(\text{min}) = \pi f_O \left[\frac{V_{GS(OFF)}}{2} + 0.7 \right] \tag{4.8}$$

For our present application the minimum slew rate is estimated as

$$slew\ rate(\text{min}) = 3.14 \times 10.5\ kHz \left[\frac{8\ V}{2} + 0.7\ V \right] = 0.155\ V/\mu s$$

The required values for both unity gain frequency and slew rate are well within the values offered by the 741 op amp, so we will choose the 741 for this application.

The final schematic of our Wien-bridge oscillator is shown in Figure 4.3. Its performance is indicated by the oscilloscope plots presented in Figure 4.4. Also



R₁ 15 kΩ
C₁ 1000pF
R₁ 390Ω
R_F 390Ω
MPF102
741
−
+
Optional amplitude control
1N914A
D₁
R₂ 15 kΩ
C₂ 1000pF
R_G 270kΩ
C_G 0.039µF

FIGURE 4.3 A design example of a 10.5-kilohertz Wien-bridge oscillator.

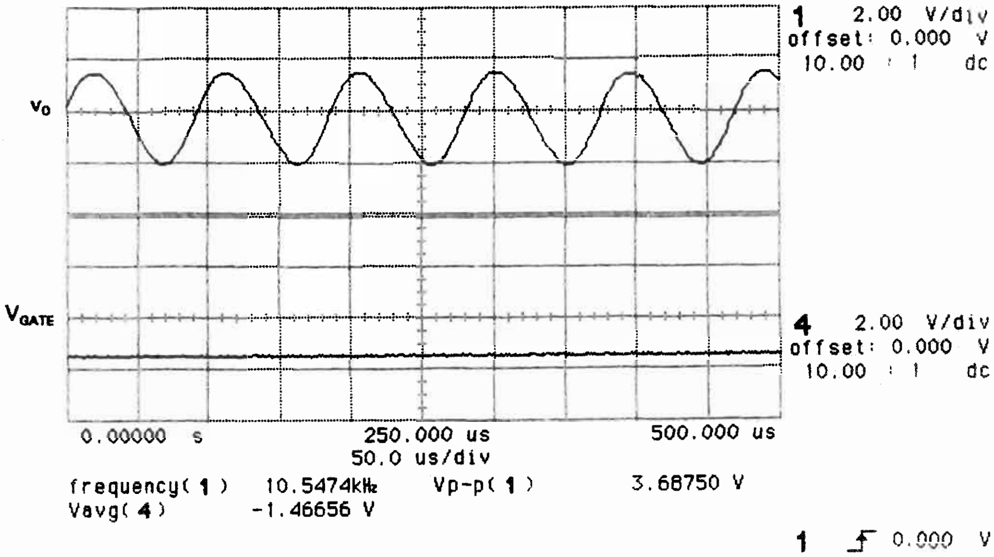


FIGURE 4.4 Oscilloscope display showing the output of the Wien-bridge oscillator circuit shown in Figure 4.3. (Test equipment courtesy of Hewlett-Packard Company.)

indicated in Figure 4.3 is a potentiometer being used as an amplitude control. As the amount of signal fed to the rectifier circuit decreases, the gain of the op amp increases, causing a higher output signal amplitude. However, as stated earlier, if the output amplitude is made too large, the FET will not be operating in the correct portion of its curve and the signal will have significant distortion.

4.3 VOLTAGE-CONTROLLED OSCILLATOR

4.3.1 Operation

A voltage-controlled oscillator (VCO) is an oscillator circuit whose frequency can be controlled or varied by a DC input voltage. This type of circuit is also called a voltage-to-frequency converter (VFC). The output waveform from the VCO may be sine, square, or other waveshape depending on the circuit design. Figure 4.5 shows the schematic of a representative VCO circuit, which produces both triangle- and square-wave outputs. In both cases, the frequency is determined by the magnitude of the DC input voltage ($+V_{IN}$).

Let us examine the circuit's operation one stage at a time. The leftmost stage is basically an inverting, summing amplifier with the feedback resistor replaced by a capacitor. The operation of this circuit, called an integrator, is discussed in greater detail in Chapter 7. For now, recall that the value of feedback current in an inverting amplifier is determined by the input voltage and the value of the input resistor(s). First, let us assume that diode D_4 is reverse-biased and acting as an open. Under these conditions, $+V_{IN}$ and R_1 will determine the value of feedback current for A_1. Since V_{IN} is DC and R_1 does not change, the value of input current

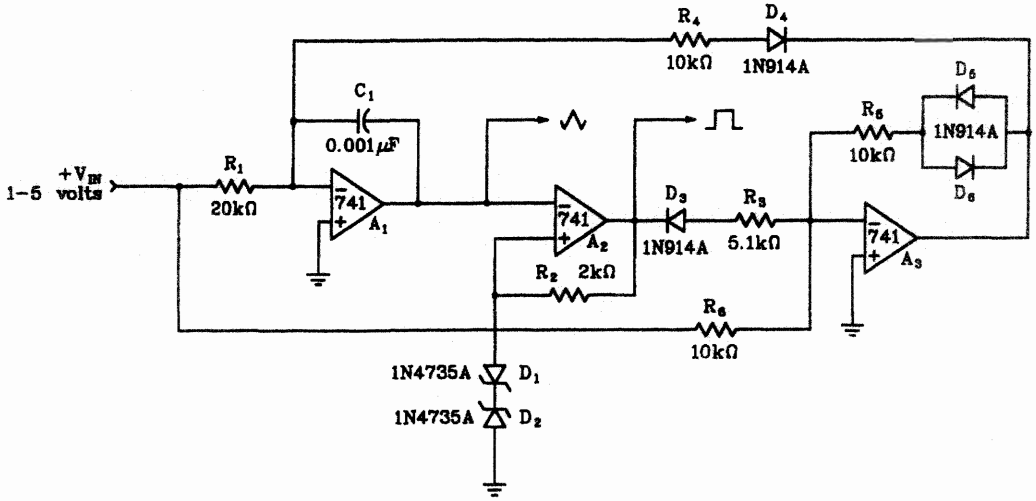


FIGURE 4.5 A voltage-controlled oscillator providing both triangle- and square-wave outputs.

and, therefore, the feedback current will be constant. The feedback current must flow through C_1.

You may recall from basic electronics theory that if a capacitor is charged with a constant current source, the resulting voltage will increase linearly. Because the charging current for C_1 is constant, we can expect a linear ramp of voltage across C_1. And because the left end of C_1 is connected to a virtual ground point, the other end (output of the op amp) will reflect the linear ramp voltage. The input voltage V_{IN} is positive, so we know that the output ramp will be increasing in the negative direction.

A_2 is configured as a voltage comparator circuit with the upper and lower thresholds being established by diodes D_1 and D_2. As long as the ramp voltage is above the lower threshold point (established by D_1), the output of amplifier A_2 will remain at its negative limit ($-V_{SAT}$).

Amplifier A_3 is connected as an inverting summing amplifier. One input comes from A_2 and receives a gain of -2. The other input is provided by $+V_{IN}$ and receives a gain of -1. As long as the output of A_2 is at its $-V_{SAT}$ level, diode D_3 will be forward-biased and this voltage will be coupled to the input of A_3. Clearly, this high-negative voltage will drive amplifier A_3 into saturation. That is, the output of A_3 will be at the $+V_{SAT}$ level regardless of the value of input voltage ($+V_{IN}$). It is this $+V_{SAT}$ level on the output of A_3 that causes D_4 to remain in a reverse-biased state. This circuit condition remains constant as long as the ramp voltage on the output of A_1 is above the lower threshold voltage of A_2.

Once the decreasing ramp voltage from A_1 falls below the lower threshold voltage of comparator A_2, the output of A_2 changes to its $+V_{SAT}$ level. This reverse-biases diode D_3 and causes A_3 to act as a simple inverting amplifier with regard to the input voltage $+V_{IN}$. A voltage level that is equal (but opposite polarity) to $+V_{IN}$ is felt at the right end of R_4. Since R_4 is half as large as R_1 and has the same voltage applied, we can expect the current flow through R_4 to be twice as large as that through R_1 and in the opposite direction.

The current provided by R_4 not only cancels the input current provided via R_1 but supplies an equal (but opposite) current to C_1. That is, C_1 will now continue to charge at the **same** linear rate but in the opposite direction. The ramp voltage at the output of A_1 will rise linearly until it exceeds the upper threshold of A_2. Once the upper threshold has been exceeded, the output of A_2 switches to the $-V_{SAT}$ level. This forces the output of A_3 to $+V_{SAT}$ and reverse-biases D_4. We are now back to the original circuit state, and the cycle repeats.

The frequency of operation is determined by the time it takes C_1 to charge to the threshold levels of A_2. Once the circuit components have been fixed, the only thing that determines frequency is the value of input voltage ($+V_{IN}$). This, of course, gives rise to the name *voltage-controlled oscillator.*

A triangle-wave (or double ramp) signal may be taken from the output of A_1. The output of A_2 provides a square-wave output.

4.3.2 Numerical Analysis

Let us now analyze the performance of the circuit in Figure 4.5 numerically. First, consider the voltage comparator A_2. It has no negative feedback, so we know that the output will be driven to one of its two extremes ($\pm V_{SAT}$) at all times. For purposes of this analysis, let us use the typical values of ±13 volts for $\pm V_{SAT}$. The threshold voltages for the comparator are determined by the zener diodes (D_1 and D_2). Appendix 8 shows that the 1N4735 diodes are designed to regulate at 6.2 volts. Therefore, when the output is at $+V_{SAT}$, the upper threshold (V_{UT}) will be determined by the regulated voltage of D_2 plus the forward voltage drop of D_1. We can express this in equation form as

$$\boxed{V_{UT} = V_{Z_{D_2}} + V_{F_{D_1}} \qquad (4.9)}$$

where V_Z is the rated zener voltage and V_F is the forward voltage drop. In the case of the circuit in Figure 4.5, the upper threshold is computed as

$$V_{UT} = 6.2\ V + 0.6\ V = 6.8\ V$$

The lower threshold (V_{LT}) is computed in a similar manner:

$$\boxed{V_{LT} = -V_{Z_{D_1}} - V_{F_{D_2}} \qquad (4.10)}$$

In the present case, we have

$$V_{LT} = -6.2\ V - 0.6\ V = -6.8\ V$$

These threshold values are particularly important because they will determine the charging limits of capacitor C_1, which is the heart of the circuit.

Now let us evaluate the numerical performance of A_3 and its associated circuitry. We will apply the Superposition Theorem and consider the two inputs to

A_3 independently. First, let us consider the $+V_{IN}$ signal input. The voltage gain of this signal is computed in the same manner as in Chapter 2 for a simple inverting amplifier. That is,

$$\begin{aligned} A_V &= -\frac{R_F}{R_I} \\ &= -\frac{10\ k\Omega}{10\ k\Omega} \\ &= -1 \end{aligned}$$

In this case, the generic R_I is replaced with physical resistor R_6. Notice that we have ignored the effects of D_5 and D_6. Recall that the output of a closed-loop op amp will go to whatever level is required to bring the differential input voltage back to near 0. By inserting a forward-biased diode in the feedback loop, the output is forced to rise an additional 0.6 volts (the forward voltage drop of the diode). By paralleling two diodes in opposite polarities (D_5 and D_6), we force the output to be 0.6 volts larger than it would otherwise have been. The actual output voltage, then, will be the normal expected output plus a fixed 0.6-volt potential that causes the output to be more positive during positive output times and more negative during negative output times. The reason for D_5 and D_6 will be evident in a moment.

Since the voltage gain for the $+V_{IN}$ signal is –1, the range of output voltages for A_3 as a result of $+V_{IN}$ is

$$\begin{aligned} v_{O_1} &= -1 \times 1\ V - 0.6\ V = -1.6\ V, \textit{ and} \\ v_{O_2} &= -1 \times 5\ V - 0.6\ V = -5.6\ V \end{aligned}$$

Now let us consider the effects of the second A_3 signal input, which comes from the output of A_2. The voltage gain for this input is computed in a similar manner.

$$A_V = -\frac{R_F}{R_I} = -\frac{10\ k\Omega}{5.1\ k\Omega} = -1.96 \approx -2$$

The input voltage (output from A_2) is the $\pm V_{SAT}$ levels for A_2. Since diode D_3 will block the positive level, we need only calculate the effects of the $-V_{SAT}$ input. The resulting output voltage from A_3 as a result of this input is computed as shown:

$$\begin{aligned} v_O &= -2 \times (-V_{SAT} + 0.6) + 0.6 \\ &= -2 \times (-13\ V + 0.6\ V) + 0.6\ V \\ &= +25.4\ V \end{aligned}$$

This computed value exceeds the limits of A_3 because it only has a ±15-volt power supply. This means that the output of A_3 will be driven to its $+V_{SAT}$ level (+13 volts).

Now let us consider the combined effects of the two inputs to A_3. Recall that the combined effect is found by adding the outputs caused by the two individual inputs. During times when the output of A_2 is positive, it has no effect on the output of A_3 (D_3 is reverse-biased), and the output of A_3 is solely determined by the $+V_{IN}$ signal, as computed previously. During the times when A_2 is at its $-V_{SAT}$ level, the output of A_3 clearly will be driven to its $+V_{SAT}$ level. Even in the best case, when $+V_{IN}$ is at its most positive (+5-volt) level, the output of A_3 will be

$$\begin{aligned} V_O &= V_{O_1} + V_{O_2} \\ &= +25.4\ V + (-5.5\ V) \\ &= +19.8\ V \end{aligned}$$

where V_{O_1} and V_{O_2} are the effective output voltages produced by A_2 and $+V_{IN}$, respectively. As you can readily see, this combined value still exceeds the $+V_{SAT}$ level of A_3, so we will expect the output of A_3 to remain at +13 volts anytime the output of A_2 is at the $-V_{SAT}$ level. On the other hand, when the output of A_2 is at the $+V_{SAT}$ level, the output of A_3 will be between −1.6 and −5.6 depending on the value of input voltage ($+V_{IN}$).

Finally, let us examine the operation of A_1 more closely. During times that the output of A_3 is at the $+V_{SAT}$ level, diode D_4 will be reverse-biased and will isolate or remove that input path for A_1. During these times, A_1 is controlled by the effects of $+V_{IN}$ only. Let us examine the charging rate of C_1 at the two extremes of $+V_{IN}$.

If $+V_{IN}$ is at its lower limit (+1 volt), then the current through R_1 is computed as

$$\begin{aligned} I_{R_1} &= \frac{+V_{IN}}{R_1} \\ &= \frac{1\ V}{20\ k\Omega} \\ &= 50\ \mu A \end{aligned}$$

Similarly, the maximum input current is computed as

$$\begin{aligned} I_{R_1} &= \frac{+V_{IN}}{R_1} \\ &= \frac{5\ V}{20\ k\Omega} \\ &= 250\ \mu A \end{aligned}$$

Since D_4 is effectively open (i.e., reverse-biased), and since no significant current can flow into or out of the (−) input terminal of the op amp, we can infer that all of the input current goes to charge C_1. More specifically, electrons flow from the output of A_1 through C_1 (i.e., charging C_1), and through R_1 to $+V_{IN}$. Further, because this current is constant (unless $+V_{IN}$ changes), capacitor C_1 will charge linearly according to the following expression:

$$V_{C_1} = \frac{It}{C_1} \tag{4.11}$$

where I is the input current computed and t is the time C_1 is allowed to charge. This equation can be transposed to produce another very useful form:

$$t = \frac{C_1 \times \Delta V_{C_1}}{I} \tag{4.12}$$

This allows us to compute the amount of time it takes C_1 to charge to a given voltage change (ΔV_{C_1}) when a given value of charging current is applied.

We already know from earlier discussions that the limits of C_1's charge are set by the upper and lower thresholds of A_2. That is, C_1 will charge linearly between the V_{LT} and V_{UT} values established by A_2. In the present circuit, the change in C_1 voltage in going from the V_{LT} to the V_{UT} is

$$\Delta V_{C_1} = V_{UT} - V_{LT} \tag{4.13}$$

More specifically,

$$\Delta V_{C_1} = +6.8\ V - (-6.8\ V) = 13.6\ V$$

If we now compute the time it takes C_1 to make this voltage change, we will know the time for one alternation (negative slope) of the oscillator's output. Let us compute this time for input voltages of +1 and +5 volts, which were previously shown to produce 50 microamperes and 250 microamperes, respectively. Equation (4.12) gives us

$$t = \frac{C_1 \times \Delta V_{C_1}}{I}$$

$$t_{+1} = \frac{0.001\ \mu F \times 13.6\ V}{50\ \mu A} = 272\ \mu s,\ and$$

$$t_{+5} = \frac{0.001\ \mu F \times 13.6\ V}{250\ \mu A} = 54.4\ \mu s$$

The remaining alternation (positive ramp) occurs when D_4 is forward-biased. This effectively connects the output of A_3 to A_1 via R_4. Recall that during this portion of the cycle, the output of A_3 is 0.6 volts larger than $+V_{IN}$ and is of the opposite polarity. Since diode D_4 drops 0.6 volts when it is forward-biased, this means that the voltage applied to the right end of R_4 is exactly the same as the value of $+V_{IN}$, but it is negative instead of positive. That is, this input to A_1 ranges from −1 to −5 volts. The resulting input current through R_4 is computed as

$$I_{R_4} = \frac{V_{R_4}}{R_4} = \frac{1\ V}{10\ k\Omega} = 100\ \mu A$$

for the –1-volt input case. The input current for the –5-volt case is

$$I_{R_4} = \frac{5\ V}{10\ k\Omega} = 500\ \mu A$$

Let us consider the electron flow in the case of a 1-volt input. Recall that R_1 will have a 50-microampere current flowing in a right-to-left direction. R_4, as computed, will have a current of 100 microamperes flowing from right to left. When the latter current gets to the summing point of A_1, it splits. One part, 50 microamperes, goes through R_1 and satisfies the requirements of $+V_{IN}$ and R_1. Kirchhoff's Current Law tells us that the remaining 50 microamperes must flow into C_1 in a left-to-right direction. It is very important to note that the magnitude of this charging current is **identical** to that which flowed on the previous alternation, but it is flowing in the opposite direction. Therefore, C_1 will charge at the **same** rate but in the opposite polarity. Because the charging currents are equal and the required voltage change (ΔV_{C1}) is the same, the amount of time for this alternation will be the same as the first. Given this observation, we can now compute the frequency of oscillation for a given input voltage ($+V_{IN}$):

$$\boxed{f_O = \frac{+V_{IN}}{2R_1C_1(V_{UT} - V_{LT})} \qquad (4.14)}$$

This equation will be valid as long as the slew rates of the op amps do not interfere with circuit operation. As the oscillator frequency increases, the slew rate limitations of the op amp tend to reduce the actual frequency from the value computed.

4.3.3 Practical Design Techniques

We will now design a voltage-controlled oscillator that meets the following design criteria:

1. Input voltage range	0 to 6 volts DC
2. Ramp output voltage	±4 volts (±3 volts minimum)
3. Frequency range	0 to 5.0 kHz

The configuration and gain values for A_3 should stay the same as that shown in Figure 4.5. Therefore, the following components will be considered as "previously computed": D_3, R_3, R_5, D_5, D_6, R_6, and D_4. If, because of availability, you elect to change any of these resistors, be sure to keep their ratios such that the voltage gain of A_3 is –1 and –2 for the $+V_{IN}$ and A_2 signals, respectively. The diodes may be substituted with any general-purpose diode, but they should all be of the same type in order to have similar voltage drops.

Select the Zener Diodes. The voltage rating of D_2 plus the forward voltage drop of D_1 determines the upper limit of the ramp output voltage. Similarly, D_1 plus the forward voltage drop of D_2 determines the lower limit of the ramp output voltage. We can express this as an equation for selecting the voltage ratings of D_1 and D_2:

$$V_{D_1} = -V_{RAMP} + 0.6 \tag{4.15}$$

and

$$V_{D_2} = +V_{RAMP} - 0.6 \tag{4.16}$$

For our present design, the required zener ratings are computed as shown:

$$V_{D_1} = -4\ V + 0.6\ V = -3.3\ V,\ and$$
$$V_{D_2} = +4\ V - 0.6\ V = +3.3\ V$$

Appendices 5 and 8 provide a manufacturer's listing of several zener diodes. Either 1N5226 or 1N4728 zeners should work for our application. Let us select the 1N5226 device for this example.

Compute R_2. Resistor R_2 is a current limiting resistor that keeps the current through D_1 and D_2 within safe limits. Although the circuit will work well with a wide range of values for R_2, a good choice is to design for a current through the zener diodes given by the following expression:

$$I_Z = 10 I_{ZK} \tag{4.17}$$

Resistor R_2 can then be determined from the following equation:

$$R_2 = \frac{V_{SAT} - V_Z - 0.6}{I_Z} \tag{4.18}$$

where V_{SAT} is the highest expected saturation voltage for A_2, V_Z is the lower of the two zener voltages (if not equal), and I_Z is the zener current calculated with Equation (4.17). The data sheet in Appendix 5 lists a knee current (I_{ZK}) of 0.25 milliamperes for the 1N5226 diodes. The design value of the zener current is then computed, as in Equation (4.17):

$$I_Z = 10 \times 0.25\ mA = 2.5\ mA$$

The value of R_2 can now be computed, as in Equation (4.18):

$$R_2 = \frac{+13\ V - 3.3\ V - 0.6\ V}{2.5\ mA} = 3.64\ k\Omega$$

We will select a standard value of 3.6 kilohms for R_2. However, because this design method inherently uses a zener current that is less than the test current (I_{ZT}), we can expect the regulated voltage to be less than the stated value. Appendix 5 includes a graph that allows us to estimate the error. In the present case, the zeners will have about 2.65 volts instead of the rated 3.3 volts, which will in turn cause the ramp output to have an amplitude of 6.5 volts instead of the design goal of 8. If this is an important circuit parameter for a given application, we should select a zener with a higher voltage rating but continue to operate it below its rated current. We continue with our present selection, since the reduced voltage is still within the tolerance stated as part of the original design goals.

Compute R_1 and C_1. Once the zeners have been selected, the values of R_1 and C_1 determine the frequency for a given voltage. The required R_1C_1 product can be found with Equation (4.19):

$$\boxed{R_1C_1 = \frac{V_{IN}(\text{max})}{2f_{HI}V_{RAMP}} \qquad (4.19)}$$

where V_{RAMP} is the amplitude of the ramp output voltage, V_{IN}(max) is the highest input voltage, and f_{HI} is the highest frequency of oscillation. Calculations for our present design example are

$$R_1C_1 = \frac{6\ V}{2 \times 5\ kHz \times 8\ V} = 75\ \mu s$$

At this point, we can either select C_1 and calculate R_1 or vice versa. In either case, we want R_1 to be in the range of 1.0 to 470 kilohms, if practical. Similarly, C_1 should be greater than 470 pF and nonpolarized. Because it is essential that R_4 be exactly one-half the value of R_1, and because there are a limited number of resistor pairs that have exactly a 2:1 ratio, it is generally easier to select R_1 and compute C_1.

For purposes of this design, let us select R_1 as 2 kilohms. We can then compute C_1 by transposing the results of Equation (4.19):

$$
\begin{aligned}
R_1C_1 &= 75\ \mu s,\ or \\
C_1 &= \frac{75\ \mu s}{R_1} \\
&= \frac{75\ \mu s}{2\ k\Omega} \\
&= 0.0375\ \mu F
\end{aligned}
$$

We will select a standard value of 0.033-microfarad for C_1. If greater accuracy is required, we can add a second capacitor in parallel with C_1.

Compute R_4. R_4 must be exactly one-half the value of R_1. That is,

$$\boxed{R_4 = \frac{R_1}{2} \qquad (4.20)}$$

In our case, we compute R_4 as

$$R_4 = \frac{2\ k\Omega}{2} = 1.0\ k\Omega$$

Select the Op Amp. The primary op amp characteristic (other than power supply voltage, etc.) in this application is slew rate. If the output of A_1 tries to change faster than the slew rate will allow, the actual operating frequency will be lower than originally predicted. Similarly, if the switching times for A_2 and A_3 are a substantial percentage of one alternation, again, the actual frequency of oscillation will be below the calculated value. To minimize this effect, we can ensure that the slew rate is fast enough to allow the rise and fall times of A_2 and A_3 to be a small part of the time for one alternation. That is,

$$\boxed{slew\ rate = 40 f_{MAX}[+V_{SAT} - (-V_{SAT})] \qquad (4.21)}$$

This equation ensures that switching time is no greater than 20 percent of the time for one alternation. If the factor 40 is changed to 200, this relationship is reduced to 1 percent, but it requires a very high slew rate op amp to achieve moderate frequencies. If this is an important consideration for your application, think about using an integrated comparator. These devices are readily available with switching times in the range of tens of nanoseconds. For our present design, however, let us determine the required slew rate for a 20-percent rise time factor:

$$
\begin{aligned}
slew\ rate &= 40 \times 5\ kHz[+13\ V - (-13\ V)] \\
&= 5.2\ V/\mu S
\end{aligned}
$$

TABLE 4.1

	Design Goal	*Measured Results*
Input voltage range	0–6 volts	0–6 volts
Frequency range	0–5 kilohertz	0–5.01 kilohertz
Ramp voltage	±4 volts ±3 volts (min)	–4, +3.75 volts

This requirement exceeds the 0.5-volts-per-microsecond slew rate rating of the standard 741, but falls within the capabilities of the MC741SC. We will utilize this latter device in our design.

Figure 4.6 shows the schematic diagram of our design example, and the oscilloscope displays in Figure 4.7 show the performance of the circuit. Additionally, Table 4.1 contrasts the design goals with the actual measured performance of the circuit.

4.4 VARIABLE-DUTY CYCLE

4.4.1 Operation

Figure 4.8 is the schematic of a very useful rectangular wave oscillator. What makes the circuit particularly useful is that the duration of each alternation is independently adjustable, which means that the duty cycle of the output can be easily adjusted from a very small to a very high value.

To begin, let us assume that the output is at its $+V_{SAT}$ level. This voltage will be regulated down to a lower value by D_3 and returned to the (+) input as a reference voltage. The positive output voltage is also regulated to a lower level by D_5. This latter voltage provides a stable charging voltage for C_1.

C_1 charges from ground through D_2, R_3, and R_4 to the regulated positive voltage provided by D_5. C_1 will charge exponentially toward the D_5 voltage. As long as the voltage on C_1 is less than the reference voltage on the (+) input of the op amp, the circuit will be stable and C_1 will continue to charge.

Once the voltage of C_1 reaches the reference voltage on the (+) input, the output of the op amp quickly switches to its $-V_{SAT}$ level. Diode D_4 regulates this negative voltage and provides a new reference voltage for the (+) input. Similarly, D_6 regulates the $-V_{SAT}$ voltage and provides a new charging source for C_1. The new source is negative, so C_1 will discharge and then recharge in the opposite polarity. The charging path is from the negative source provided by D_6 through R_2, R_1, D_1, and C_1 to ground. Again, this is an exponential charging action and will continue as long as the voltage on C_1 remains more positive than the negative reference voltage on the (+) input. Once the voltage on C_1 falls below the reference voltage on the (+) input, the circuit quickly switches back to its original state and the cycle repeats.

The time it takes C_1 to charge during the positive output alternation is determined by the values of C_1, R_3, R_4, and D_5. Since R_3 is adjustable, it can be used to

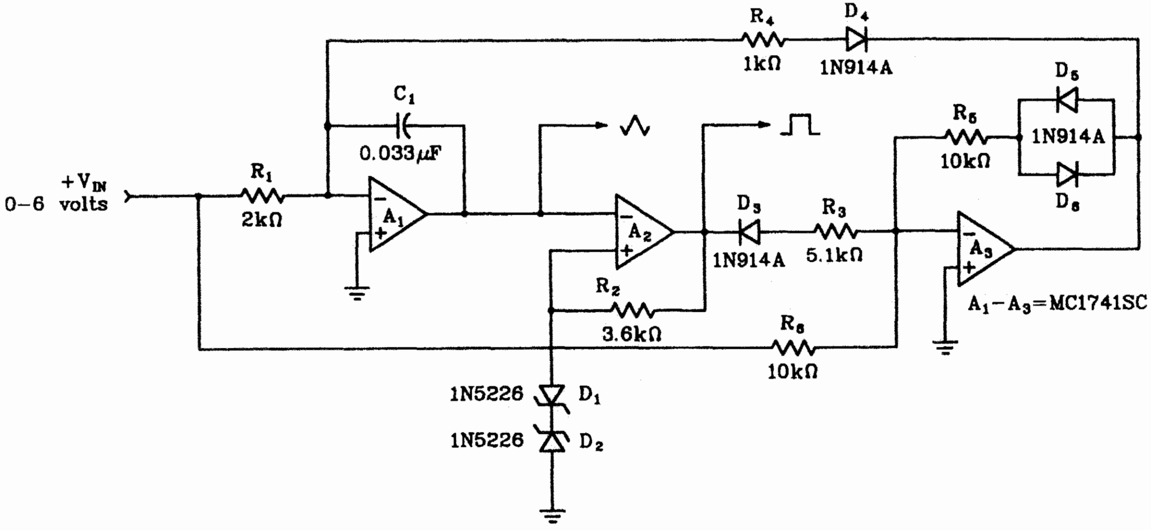

R4
1kΩ
D4
1N914A
D5
C1
0.033μF
R5
10kΩ
1N914A
D6
+VIN
0–6 volts
R1
2kΩ
A1
A2
D3
1N914A
R3
5.1kΩ
A3
A1−A3=MC1741SC
R2
3.6kΩ
R6
10kΩ
1N5226
D1
1N5226
D2

FIGURE 4.6 A design example of a 0–5-kilohertz voltage-controlled oscillator.

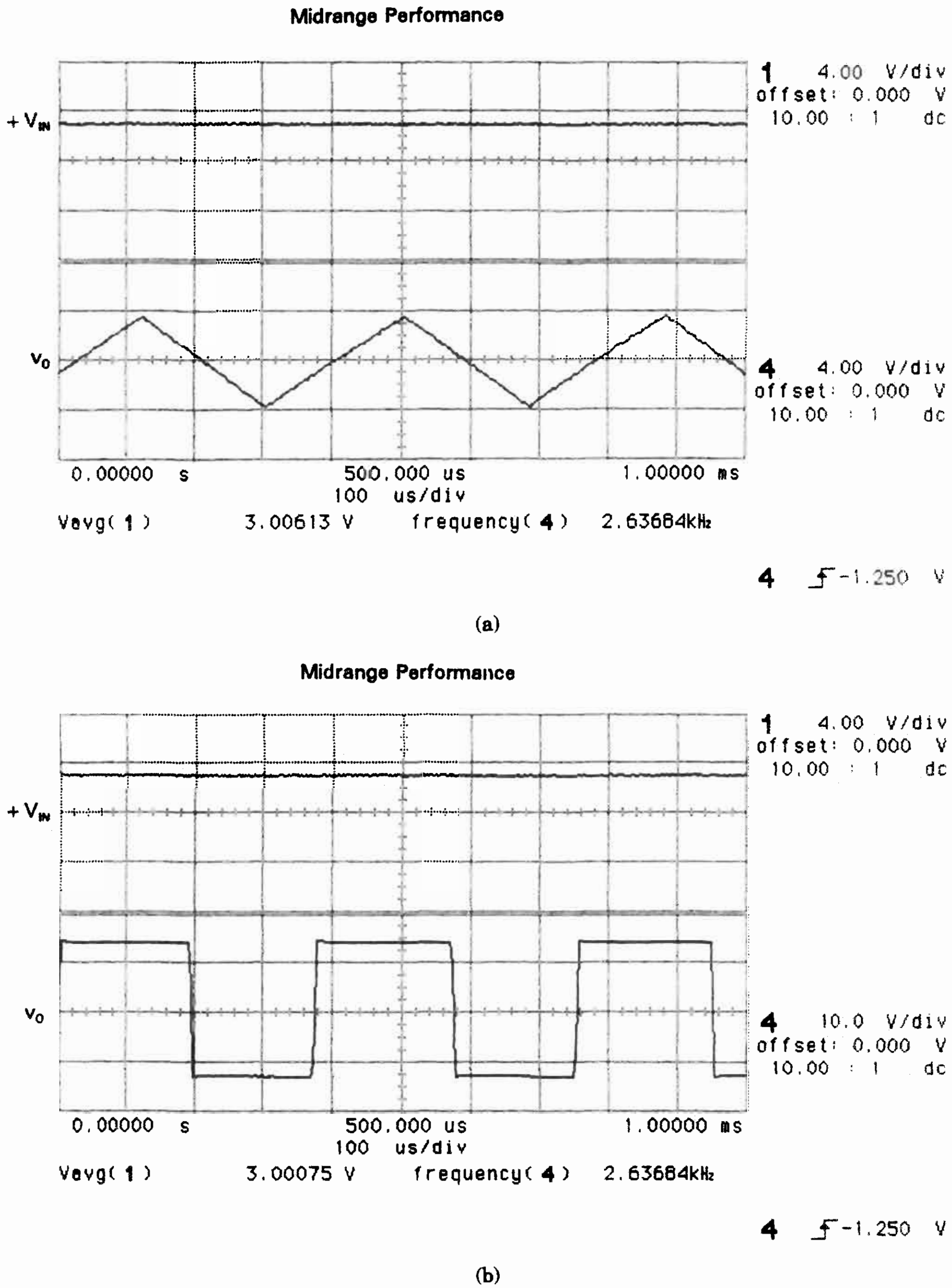
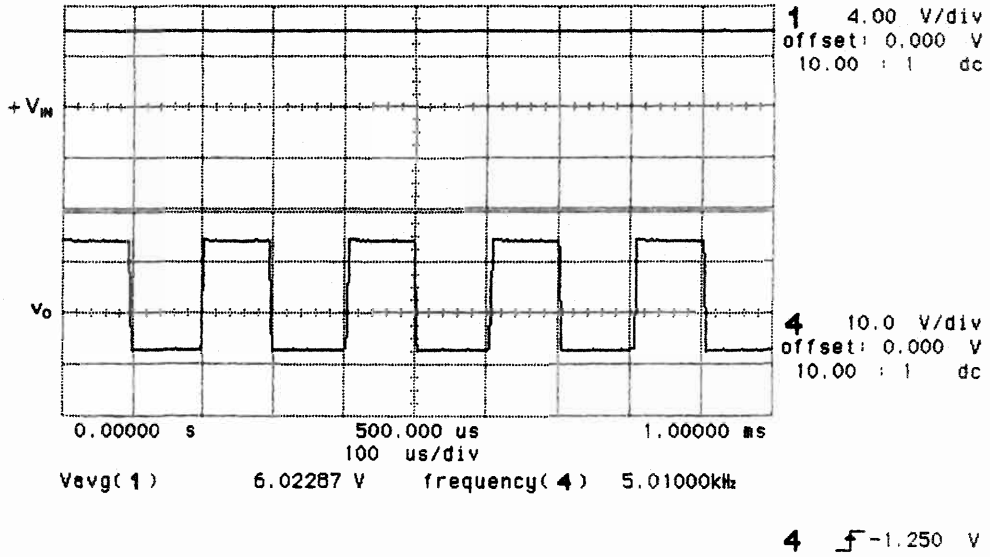


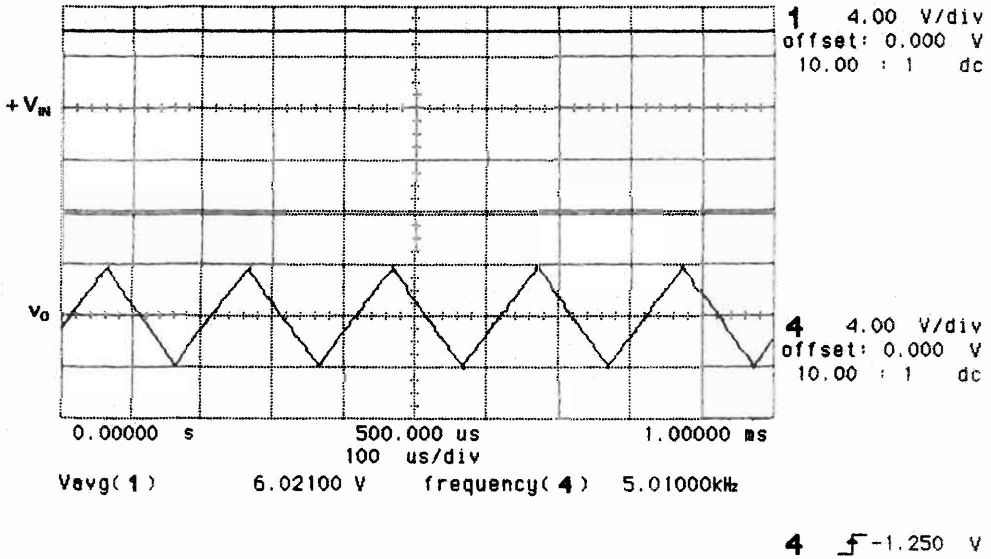
FIGURE 4.7 Oscilloscope displays showing the performance of the voltage-controlled oscillator circuit shown in Figure 4.6. (Test equipment courtesy of Hewlett-Packard Company.)

High-Frequency Performance



(c)

High-Frequency Performance



(d)

FIGURE 4.7 *Continued*

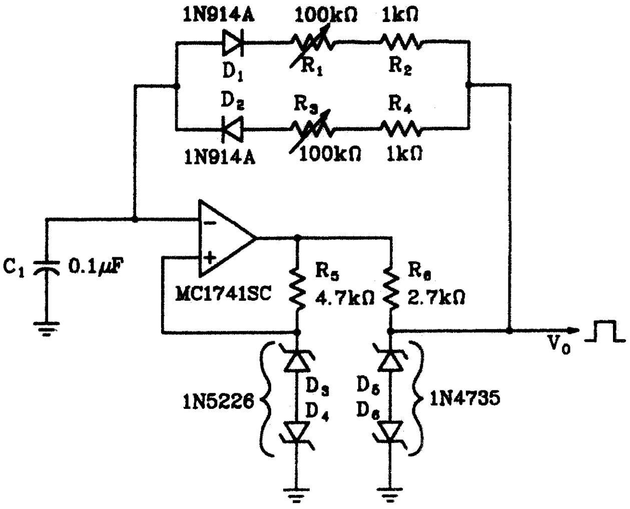


FIGURE 4.8 A rectangular wave oscillator with independently controllable alternation times providing both frequency and duty-cycle control.

control the period of the positive alternation without affecting the negative alternation. The values of C_1, R_1, R_2, and D_6 determine the charge time for C_1 during the negative output alternation as well. Resistor R_1 can be used to control this time period without affecting the positive alternation.

Resistors R_5 and R_6 are current limiting resistors for the two sets of back-to-back zener regulators.

4.4.2 Numerical Analysis

Let us now extend our analysis of the variable-duty cycle oscillator shown in Figure 4.8 to include a numerical understanding of its operation. We will first consider the two sets of back-to-back zener regulators. The $\pm V_{SAT}$ output of the op amp will be regulated by D_3 and D_4 to provide a reference voltage for the (+) input. The value of this reference is computed with Equations (4.22) and (4.23).

$$+V_{REF} = V_{D_3} + 0.6 \tag{4.22}$$

$$-V_{REF} = -V_{D_4} - 0.6 \tag{4.23}$$

For many analytical purposes, the rated voltages of the zeners may be used. If you require greater accuracy, you can compute the current through the zeners and refer to the manufacturer's data sheet to determine the actual voltage. For the present example, let us compute the reference voltages in both ways. First, the approximate reference voltage can be found by applying Equations (4.22) and (4.23) using the rated voltages for the zeners. In our case, we have

$$+V_{REF} = 3.3\ V + 0.6\ V = 3.9\ V, \textit{and}$$
$$-V_{REF} = -3.3\ V - 0.6\ V = -3.9\ V$$

If we compute the actual zener current, we can make a closer approximation. Since the circuit is utilizing similar zeners, we can calculate either one. Suppose we work out the current during the positive output alternation:

$$I_{D_3} = \frac{+V_{SAT} - V_{D_3} - 0.6}{R_5} \tag{4.24}$$

Substituting values gives us

$$I_{D_3} = \frac{13\ V - 3.3\ V - 0.6\ V}{4.7\ k\Omega} = 1.94\ mA$$

Of course, even this is not an exact value because we know that the 3.3-zener drop is actually less, but our overall result will be very close to the actual value. If we now refer to the manufacturer's data sheet in Appendix 5, we can estimate the actual zener voltage for a 1N5226 with about 2 milliamperes of current. The graph in Figure 2 of Appendix 5 indicates that our zener will have a voltage of about 2.6 volts. If we use this value and recompute the reference voltages with Equations (4.22) and (4.23), we will get more accurate values.

$$+V_{REF} = 2.6\ V + 0.6\ V = 3.2\ V, \textit{and}$$
$$-V_{REF} = -2.6\ V - 0.6\ V = -3.2\ V$$

Let us now perform a similar calculation for the D_5 and D_6. We will use the nominal values for the zener voltages and apply Equations (4.25) and (4.26).

$$+V_O = V_{D_5} + 0.6 \tag{4.25}$$

$$-V_O = -V_{D_6} - 0.6 \tag{4.26}$$

Substituting values gives us the following estimates:

$$+V_O = 6.2\ V + 0.6\ V = 6.8\ V, \textit{and}$$
$$-V_O = -6.2\ V - 0.6\ V = -6.8\ V$$

Note that the actual measured zener voltages will vary somewhat from their nominal value. Nevertheless, we will use our computed values for the remainder of the analysis.

We are now in a position to compute the operating frequency, duty cycle, pulse width, and so on. Equation 4.27 is used to determine the duration of the positive output alternation.

$$t^{+} = (R_3 + R_4)C_1 \ln \frac{V_{D_6} - V_{D_3}}{V_{D_6} - V_{D_4}} \tag{4.27}$$

Similarly, Equation (4.28) is used to determine the time for the negative output alternation.

$$t^{-} = (R_1 + R_2)C_1 \ln \frac{V_{D_5} - V_{D_4}}{V_{D_5} - V_{D_3}} \tag{4.28}$$

For illustrative purposes, let us compute the minimum and maximum time for both alternations by repeatedly applying Equations (4.27) and (4.28).

$$t^{+}(\text{min}) = (0 + 1\ k\Omega) \times 0.1\ \mu F \times \ln \frac{6.2\ V - (-3.3\ V)}{6.2\ V - 3.3\ V} = 119\ \mu s,\ and$$

$$t^{+}(\text{max}) = (100\ k\Omega + 1\ k\Omega) \times 0.1\ \mu F \times \ln \frac{6.2\ V - (-3.3\ V)}{6.2\ V - 3.3\ V} = 12\ ms$$

We can already see that the circuit gives us a 101:1 range of control on the positive alternation. A similar calculation for the negative alternation gives us

$$t^{-}(\text{min}) = (0 + 1\ k\Omega) \times 0.1\ \mu F \times \ln \frac{6.2\ V - (-3.3\ V)}{6.2\ V - 3.3\ V} = 119\ \mu s,\ and$$

$$t^{-}(\text{max}) = (100\ k\Omega + 1\ k\Omega) \times 0.1\ \mu F \times \ln \frac{6.2\ V - (-3.3\ V)}{6.2\ V - 3.3\ V} = 12\ ms$$

Since Equations (4.27) and (4.28) ignore the forward voltage drops of D_1, D_2, and the effective resistance of the zener regulator circuit, the actual times for t^{+} and t^{-} will be somewhat longer than our calculations predict.

Because the components are matched, the results are the same for each alternation. In practice, however, the two alternations do not have to have equal ranges.

Now let us extend our analysis to determine the minimum and maximum frequency of operation. These two extremes are given by Equations (4.29) and (4.30).

$$f_{MIN} = \frac{1}{t^{+}(\text{max}) + t^{-}(\text{max})} \tag{4.29}$$

$$f_{MAX} = \frac{1}{t^+(\min) + t^-(\min)} \tag{4.30}$$

Substituting values for our case gives the following results for a frequency range:

$$f_{MIN} = \frac{1}{12\ ms + 12\ ms} = 41.7\ Hz, \text{ and}$$

$$f_{MAX} = \frac{1}{119\ \mu s + 119\ \mu s} = 4.2\ kHz$$

This, of course, equates to a frequency range of 101:1.

Finally, let us determine the range of duty cycles. Recall from your basic electronics theory that duty cycle is defined as the ratio of pulse width to total period.

$$\%\ duty = \frac{PW}{period} \times 100 \tag{4.31}$$

For this calculation, we will consider pulse width to be the positive alternation of the output signal. The range of duty cycles is then computed.

$$\%\ duty(\min) = \frac{119\ \mu s}{119\ \mu s + 12\ ms} \times 100 = 0.98\%, \text{ and}$$

$$\%\ duty(\max) = \frac{12\ ms}{12\ ms + 119\ \mu s} \times 100 = 99\%$$

As you might suspect, this is also a 101:1 range of control.

4.4.3 Practical Design Techniques

For purposes of our design example, let us design a circuit similar to the one in Figure 4.8 that displays the following behavior:

1. Positive output time	1 to 10 milliseconds
2. Negative output time	2 to 20 milliseconds
3. Output amplitude	±7 volts (±6 minimum)

Select the Output Zeners. The amplitude of the output voltage specification dictates the zener diodes that will be used. If the required output amplitude is less than 6 to 7 volts, it is best to design for a higher voltage and subsequently reduce it with an output voltage divider. For proper circuit operation, it is essential that the output swing be larger than the reference swing felt on the (+) input. Equation (4.25) can be used to determine the required voltage rating for D_5.

$$\begin{aligned} +V_O &= V_{D_5} + 0.6, \ or \\ V_{D_5} &= +V_O - 0.6 \\ &= +7\ V - 0.6\ V \\ &= 6.4\ V \end{aligned}$$

Similarly, Equation (4.26) tells us the nominal voltage rating for D_6.

$$\begin{aligned} -V_O &= -V_{D_6} - 0.6, \ or \\ -V_{D_6} &= -V_O + 0.6 \\ &= -7\ V + 0.6\ V \\ &= -6.4\ V \end{aligned}$$

Referring to Appendices 5 and 8, we see that there will be difficulty getting a 6.4-volt zener. However, if we design for a zener current that is less than the test current, the actual zener voltage will be less than the rated value. With this in mind, let us select the next higher standard value. More specifically, let us plan to use 1N5235 zeners for diodes D_5 and D_6.

Compute the Value for R_6. R_6 can be found with our basic zener equation, Equation (4.24). In our present case, we will be finding the value of R_6 with $+V_{SAT}$, V_{D5}, and I_{D5} known. Because the output of the op amp must supply currents to two zener circuits and the C_1 timing circuit, we will limit the zener currents to no more than 20 percent of the short-circuit output current. That is,

$$\boxed{I_Z = 0.2 I_{OS} \qquad (4.32)}$$

In our present case,

$$I_Z = 0.2 \times 20\ mA = 4\ mA$$

If we use the typical $+V_{SAT}$ value of +13 volts, we can calculate a value for R_6 by applying Equation (4.24).

$$\begin{aligned} R_6 &= \frac{+V_{SAT} - V_{D_5} - 0.6}{I_Z} \\ &= \frac{13\ V - 6.4\ V - 0.6\ V}{4\ mA} \\ &= 1.5\ k\Omega \end{aligned}$$

Select the Reference Zener. Although the selection of diodes D_3 and D_4 is not critical, the following equation provides a good rule of thumb:

$$V_{Z_{REF}} = \frac{V_{Z_{OUT}}}{2} \tag{4.33}$$

Let us utilize this practice and determine the required voltage for the reference diodes.

$$V_{Z_{REF}} = \frac{6.4\ V}{2} = 3.2\ V$$

We choose to use 1N5226 zeners for our application. As Appendix 5 shows, these diodes have a rated voltage of 3.3 volts; however, with less than 20 milliamperes of zener current, the actual voltage will be somewhat lower.

Compute the Value for R_5. Resistor R_5 is computed in the same way as resistor R_6. We use the same guideline, Equation (4.32), that sets the zener current to 20 percent of I_{OS}, which was previously computed to be 4 milliamperes. The value for R_5 can be found by applying the principle represented in Equation (4.24).

$$R_5 = \frac{+13\ V - 3.3\ V - 0.6\ V}{4\ mA} = 2.28\ k\Omega$$

We will choose the standard value of 2.2 kilohms.

Compute C_1 and the Timing Resistors. The first step in determining values for C_1 and $R_1 - R_4$ is to determine the required RC time constant for the shorter period in the design requirement. For this, we utilize a transposed version of Equations (4.27) or (4.28). If the positive alternation is the shorter, use a transposed version of Equation (4.27). Equation (4.28) should be utilized if the negative alternation is shorter. For our case, the 1-millisecond positive output time is clearly the shorter, so we will apply Equation (4.27) to determine the required RC product.

$$\begin{aligned} R_4C_1 &= \frac{t_+}{\ln\left(\dfrac{V_{D_6} - V_{D_3}}{V_{D_6} - V_{D_4}}\right)} \\ &= \frac{1.0\ ms}{\ln\left(\dfrac{6.4\ V - (-3.3\ V)}{6.4\ V - 3.3\ V}\right)} \\ &= 877\ \mu s \end{aligned}$$

To ensure that we come up with practical values, it is generally best to select R_4 at this point and compute C_1. Additionally, we are working with the shortest time period, so we should select a fairly small value for R_4 as long as we don't go below 1000 ohms. For this example, let us use a 1.8-kilohm resistor for R_4. We can utilize the results of our previous calculation and determine the value of C_1.

$$\begin{aligned} R_4C_1 &= 877\ \mu s,\ or \\ C_1 &= \frac{877\ \mu s}{R_4} \\ &= \frac{877\ \mu s}{1.8\ k\Omega} \\ &= 0.487\ \mu F \end{aligned}$$

We will select a standard value of 0.47 microfarad for C_1.

We can utilize Equation (4.27) to compute the required value for R_3. Its value will establish the maximum time for the positive alternation.

$$\begin{aligned} t^+ &= (R_3 + R_4)C_1 \ln \frac{V_{D_6} - V_{D_3}}{V_{D_6} - V_{D_4}},\ or \\ R_3 &= \frac{t_+}{C_1 \ln\left(\frac{V_{D_6} - V_{D_3}}{V_{D_6} - V_{D_4}}\right)} - R_4 \\ &= \frac{10\ ms}{0.47\ \mu F \times \ln\left(\frac{6.4\ V - (-3.3\ V)}{6.4\ V - 3.3\ V}\right)} - 1.8\ k\Omega \\ &= 16.85\ k\Omega \end{aligned}$$

The nearest standard potentiometer value is 20 kilohms. We will use a 20-kilohm variable resistor for R_3.

Resistors R_1 and R_2 are computed in the same way as R_3 and R_4, except that Equation (4.28) is utilized along with the times associated with the negative alternation. These calculations are

$$t^- = (R_1 + R_2)C_1 \ln \frac{V_{D_5} - V_{D_4}}{V_{D_5} - V_{D_3}}$$

and

$$\begin{aligned} R_2 &= \frac{t^-(\text{min})}{C_1 \ln\left(\frac{V_{D_5} - V_{D_4}}{V_{D_5} - V_{D_3}}\right)} \\ &= \frac{2\ ms}{0.47\ \mu F \times \ln\left(\frac{6.4\ V - (-3.3\ V)}{6.4\ V - 3.3\ V}\right)} \\ &= 3.73\ k\Omega \end{aligned}$$

We will select a standard value of 3.6 kilohms for R_2.

Finally, we compute the value of R_1 by applying Equation (4.28).

$$t^- = (R_1 + R_2)C_1 \ln \frac{V_{D_5} - V_{D_4}}{V_{D_5} - V_{D_3}}, \textit{ or}$$

$$\begin{aligned} R_1 &= \frac{t^-(\max)}{C_1 \ln\left(\dfrac{V_{D_5} - V_{D_4}}{V_{D_5} - V_{D_3}}\right)} - R_2 \\ &= \frac{20\ ms}{0.47\ \mu F \times \ln\left(\dfrac{6.4\ V - (-3.3\ V)}{6.4\ V - 3.3\ V}\right)} - 3.6\ k\Omega \\ &= 33.7\ k\Omega \end{aligned}$$

The nearest standard value for R_1 is 25 kilohms. It might be a better choice, however, to go to the next higher value so we can be sure that the maximum pulse width in our original design goal can be achieved. With this in mind, let us select a 50-kilohm variable resistor for R_1.

Select D_1 and D_2. Diodes D_1 and D_2 are simple isolation diodes and have no critical characteristics as long as the V_{PIV} rating of the diode exceeds about 30 volts and the I_F rating is greater than the I_{OS} rating of the op amp. We will use 1N914A diodes for our example design.

Select the Op Amp. The primary op amp parameter that must be considered in this application is the slew rate. If the slew rate causes the rise and fall times of the output waveform to be a significant part of either alternation, then the alternation will be longer than originally predicted.

For purposes of our present example, let us accept a rise and fall time of 10 percent of the shortest alternation period. In our case, this means that the rise and fall times can be no longer than 10 percent of 1 millisecond, or 100 microseconds. Having established the longest acceptable switching time, we can apply Equation (4.34) to determine the required slew rate:

$$\boxed{\textit{slew rate}(\min) = 10\frac{+V_{SAT} - (-V_{SAT})}{t_{MIN}} \qquad (4.34)}$$

where t_{MIN} is the shortest alternation for the circuit. In our design, the shortest alternation occurs on the positive half cycle and is 1.0 milliseconds. We will use typical values for $\pm V_{SAT}$ and compute our minimum slew rate.

$$\textit{slew rate}(\min) = 10\frac{13\ V - (-13\ V)}{1.0\ ms} = 0.26\ V/\mu S$$

This is below the 0.5-volts-per-microsecond slew rate of the 741 op amp, so let us select this device for our design.

The completed design is shown in Figure 4.9, and the actual performance of the circuit is indicated by the oscilloscope waveforms presented in Figure 4.10. Finally, Table 4.2 contrasts the original design goals with the measured performance of the circuit.

These first-try values will satisfy the requirements of many applications. If greater accuracy is needed in a particular parameter, simple tweaking in the laboratory will bring the circuit into compliance.

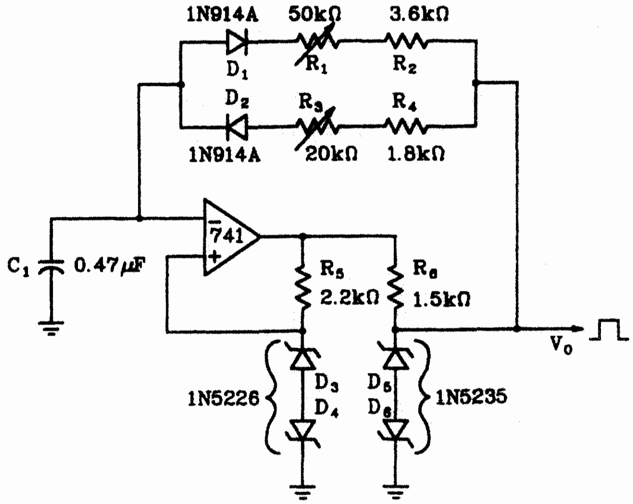
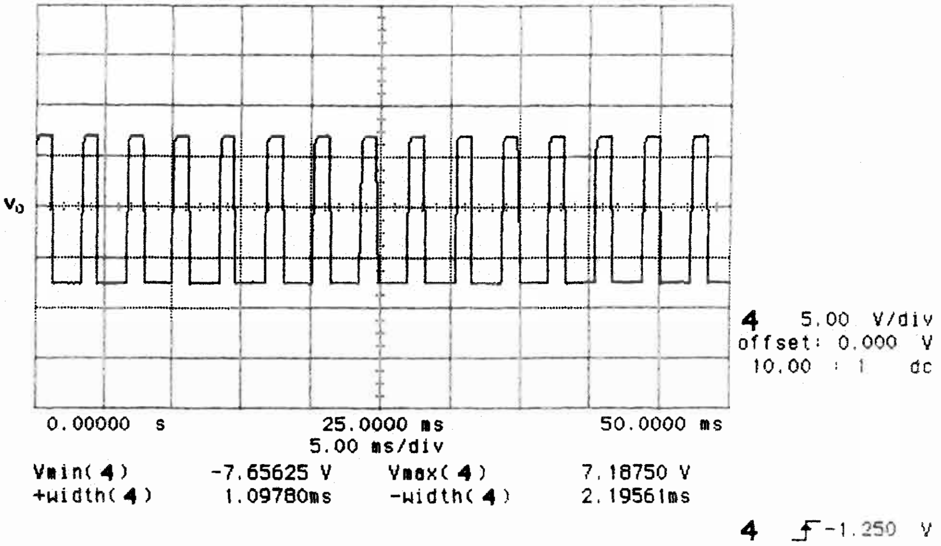


FIGURE 4.9 A design example of a variable-duty-cycle oscillator circuit.

TABLE 4.2

		Design Goal	*Measured Value*
Positive output time	Minimum	1.0 milliseconds	1.1 milliseconds
	Maximum	10 milliseconds	12.8 milliseconds
Negative output time	Minimum	2.0 milliseconds	2.2 milliseconds
	Maximum	20 milliseconds	26.5 milliseconds
Output amplitude		±7 volts (±6 volts min)	−7.6, +7.2 volts

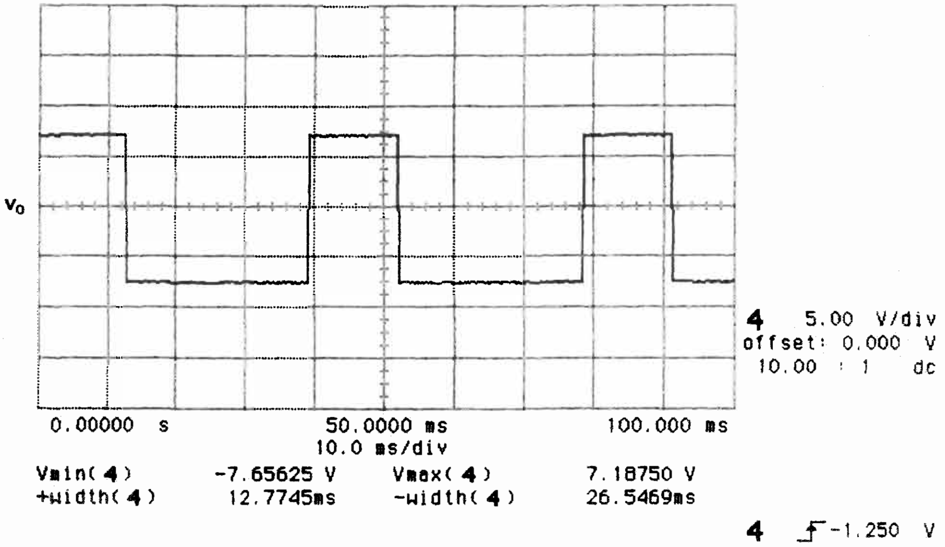
Minimum Pulse Widths



```
                                                      4   5.00  V/div
                                                      offset: 0.000  V
                                                       10.00  : 1    dc
 0.00000  s          25.0000 ms           50.0000 ms
                     5.00 ms/div
Vmin( 4 )     -7.65625 V    Vmax( 4 )     7.18750 V
+width( 4 )    1.09780ms    -width( 4 )   2.19561ms
                                                      4  -1.250  V
```

(a)

Maximum Pulse Widths



```
                                                      4   5.00  V/div
                                                      offset: 0.000  V
                                                       10.00  : 1    dc
 0.00000  s          50.0000 ms          100.000 ms
                     10.0 ms/div
Vmin( 4 )     -7.65625 V    Vmax( 4 )     7.18750 V
+width( 4 )   12.7745ms     -width( 4 )   26.5469ms
                                                      4  -1.250  V
```

(b)

FIGURE 4.10 Oscilloscope displays of the output of the oscillator circuit shown in Figure 4.9. (Test equipment courtesy of Hewlett-Packard Company.)

4.5 TRIANGLE-WAVE OSCILLATOR

4.5.1 Operation

Figure 4.11 shows the schematic of an oscillator circuit that generates a dual ramp (triangle) output. The heart of the circuit is amplifier A_1 which uses a capacitor as the feedback element. This operates as an integrator and is similar in operation to amplifier A_1 in Figure 4.5 discussed in an earlier section.

Let us assume that the output of A_2 is at its $-V_{SAT}$ level. Under these conditions, electrons will flow from the negative potential at the output of A_2, through R_1 and then C_1 as a charging current. The value of this current is determined by the voltage at the output of A_2 and the value of R_1. Since neither of these is changing at the moment, we assume the charging current is constant.

Whenever a capacitor is charged from a constant current source, the voltage across it accumulates linearly. Therefore, the voltage across C_1 will be increasing linearly, with the right side becoming more positive. Since the left side of C_1 is connected to a virtual ground point, the right side has a positive-going ramp with reference to ground. This is, of course, our output signal.

When the positive-going ramp exceeds the upper threshold voltage of A_2, which you should recognize as a noninverting voltage comparator, the output of A_2 will quickly switch to its $+V_{SAT}$ level.

The electron flow through C_1 now reverses and flows from C_1 through R_1 toward the positive potential at the A_2 output. Again, the value of the current is constant and determined by R_1 and the voltage at the output of A_2. The voltage across C_1 will decay linearly until it passes through 0. It will then begin to charge at the same rate in the opposite polarity, producing the negative slope on our output.

The output of A_1 continues to become more negative until it falls below the lower threshold voltage of A_2. At this time, the output of A_2 switches to its $-V_{SAT}$ level and the cycle repeats.

4.5.2 Numerical Analysis

Let us now numerically analyze the performance of the circuit shown in Figure 4.11. First we compute the upper ($+V_{TH}$) and lower ($-V_{TH}$) threshold voltages for the noninverting comparator A_2. The value of either threshold can be determined with Equation (4.35).

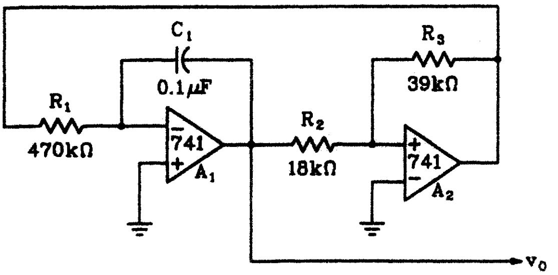


FIGURE 4.11 A triangle-wave oscillator circuit.

$$\pm V_{TH} = \frac{\pm V_{SAT} R_2}{R_3} \tag{4.35}$$

In the case of the circuit in Figure 4.11, the threshold voltages are computed as

$$\pm V_{TH} = \frac{\pm 13\ V \times 18\ k\Omega}{39\ k\Omega} = \pm 6\ V$$

We are now ready to compute the frequency of operation. Since both positive and negative saturation voltages, as well as both thresholds of A_2, are equal in this circuit, the time for either alternation can be computed with Equation (4.36).

$$t^{\pm} = R_1 C_1 \ln \frac{V_{SAT} + V_{TH}}{V_{SAT} - V_{TH}} \tag{4.36}$$

In our present case, these times are computed as follows:

$$t^{\pm} = 470\ k\Omega \times 0.1\ \mu F \times \ln \frac{13\ V + 6\ V}{13\ V - 6\ V} = 46.93\ ms$$

The total period for one cycle is, of course, twice the time computed with Equation (4.36). The frequency is simply the inverse of the total period, which is

$$f = \frac{1}{t^{+} + t^{-}} \tag{4.37}$$

In our particular circuit, the frequency of oscillation is found as follows:

$$f = \frac{1}{46.93\ ms + 46.93\ ms} = 10.65\ Hz$$

4.5.3 Practical Design Techniques

Now let us design a dual ramp oscillator similar to the one shown in Figure 4.11. For this design, we will strive for the following design goals:

1. Frequency of oscillation	1.5 kilohertz
2. Ramp amplitude	±3 volts

Calculate the Values for R_2 and R_3. Resistors R_2 and R_3 establish the threshold voltages for comparator A_2. These voltages in turn determine the output amplitude of the ramp voltage. The ratio of R_2 to R_3 can be found by applying Equation (4.35).

$$\pm V_{TH} = \frac{V_{SAT}R_2}{R_3}, \ or$$

$$\frac{R_2}{R_3} = \frac{V_{TH}}{V_{SAT}}$$

$$= \frac{3\ V}{13\ V}$$

$$= 0.231$$

We can now select R_2 and compute R_3. Both resistors should be in the range of 1 to 680 kilohms unless there is a compelling reason to exceed these suggested extremes. Let us select R_2 to be 56 kilohms. R_3 can now be computed by using the results of our previous calculation.

$$\frac{R_2}{R_3} = 0.231, \ or$$

$$R_3 = \frac{R_2}{0.231}$$

$$= \frac{56\ k\Omega}{0.231}$$

$$= 242.4\ k\Omega$$

We will use the nearest standard value of 240 kilohms.

Compute R_1 and C_1. Once the thresholds have been established on the comparator circuit, R_1 and C_1 determine the frequency of oscillation. The required R_1C_1 time constant can be found by applying Equations (4.36) and (4.37). First, let us use Equation (4.37) to determine the total period for one cycle.

$$f = \frac{1}{t^+ + t^-}, \ or$$

$$t^+ + t^- = \frac{1}{f}$$

$$= \frac{1}{1.5\ kHz}$$

$$= 666.7\ \mu s$$

Since we know the two alternations are equal, we can determine the time for either alternation by dividing the total time by 2. That is,

$$t^+ = t^- = \frac{666.7\ \mu s}{2} = 333.35\ \mu s$$

We can now apply Equation (4.36) to determine the R_1C_1 time constant.

$$t^{\pm} = R_1C_1 \ln\left(\frac{V_{SAT} + V_{TH}}{V_{SAT} - V_{TH}}\right), \text{ or}$$

$$\begin{aligned} R_1C_1 &= \frac{t^{\pm}}{\ln\left(\dfrac{V_{SAT} + V_{TH}}{V_{SAT} - V_{TH}}\right)} \\ &= \frac{333.35\ \mu s}{\ln\left(\dfrac{13\ V + 3\ V}{13\ V - 3\ V}\right)} \\ &= 709.25\ \mu s \end{aligned}$$

We now select either R_1 or C_1 and compute the other. In either case, we want R_1 to be in the range of 1.0 to 470 kilohms, if practical. Similarly, C_1 should be greater than 470 picofarads and nonpolarized. For our present example, let us select C_1 as 0.0047 microfarad. We now compute R_1 by dividing C_1 into the R_1C_1 time constant.

$$\begin{aligned} R_1 &= \frac{R_1C_1}{C_1} \\ &= \frac{709.25\ \mu s}{0.0047\ \mu F} \\ &= 150.9\ k\Omega \end{aligned}$$

Let us use a standard value of 150 kilohms for R_1.

Select the Op Amps. Other than obvious things like supply voltage ratings, the most critical op amp parameter is slew rate. In order for our calculations regarding frequency of operation to be valid, the rise and fall time in the output of A_2 must be a small part of the time for either alternation. The greater the switching times, the greater the error in calculations. If we accept rise and fall times of 10 percent of one alternation of the triangle wave, we can apply Equation (4.34).

$$\begin{aligned} \text{slew rate(min)} &= 10\frac{+V_{SAT} - (-V_{SAT})}{t^{\pm}} \\ &= 10\frac{13\ V - (-13\ V)}{333.35\ \mu s} \\ &= 0.78\ V/\mu s \end{aligned}$$

This exceeds the 0.5-volts-per-microsecond rating of the standard 741, but falls well within the capability of the MC1741SC. We will select this device for our op amps.

Figure 4.12 shows the schematic diagram of the completed design. The oscilloscope plots in Figure 4.13 indicate the actual performance of the circuit. Finally, Table 4.3 contrasts the original design goals with the measured performance of the

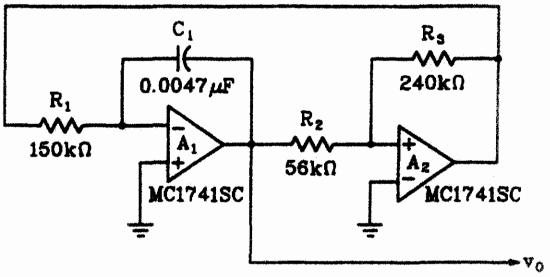


FIGURE 4.12 A triangle-wave oscillator designed for a 1.5-kilohertz operating frequency.

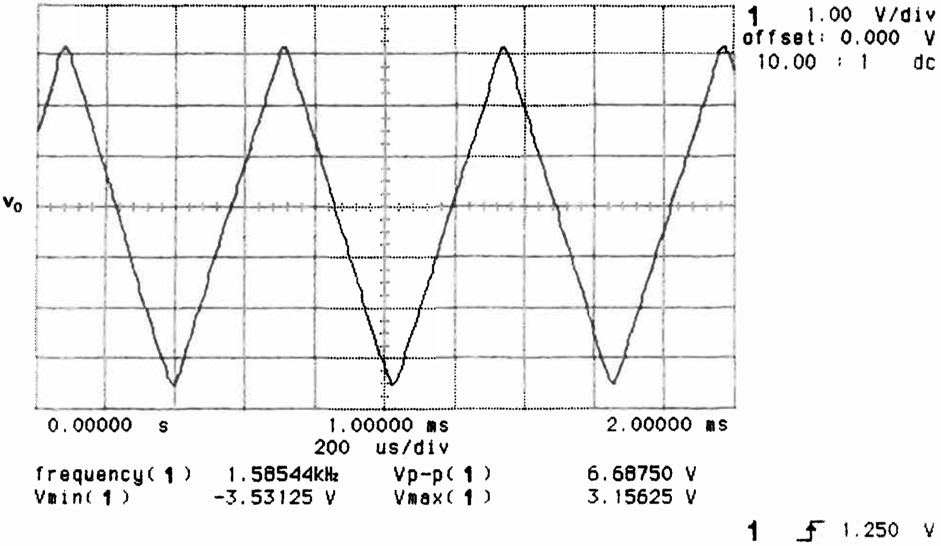


FIGURE 4.13 Oscilloscope displays showing the actual performance of the triangle-wave oscillator shown in Figure 4.12. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 4.3

	Design Goal	*Measured Value*
Frequency	1.5 kilohertz	1.59 kilohertz
Ramp amplitude	±3 volts	+3.2 volts, −3.3 volts

circuit. An interesting modification to the circuit involves paralleling R_1 with a smaller resistor in series with a diode. This will cause one alternation to be significantly shorter and will generate a forward or reverse sawtooth waveform (determined by the polarity of the added diode). The slew rate of the op amp ultimately limits the minimum ramp time.

4.6 TROUBLESHOOTING TIPS FOR OSCILLATOR CIRCUITS

The problems with op amp oscillator circuits generally fall into one of three categories:

1. Completely inoperative (i.e., no output signal)
2. Distorted output waveform
3. Incorrect frequency of oscillation

In many cases, items 2 and 3 occur simultaneously. As always, your best troubleshooting tool is your basic electronics theory and your complete understanding of correct circuit operation.

Oscillator Completely Inoperative. The first thing to check if there is no output signal is the power supply voltages. A quick check **directly** on the $\pm V_{CC}$ pins of the op amp will reveal or eliminate this potential problem. When checking for missing voltages, be certain to measure directly on the pin of the op amp. If you measure at some other point, you may fail to detect a poor solder joint, a broken printed circuit trace, and so on.

If the supplies are proper but the oscillator has no output (and assuming it is correctly designed to oscillate), then measure the DC level of the output pin of the op amp. Some oscillators (e.g., Wien-bridge) use AC coupling for some of the feedback. If the output is near 0 volts DC (i.e., not driven to either saturation level), suspect an open in the AC feedback path. If the output is driven to V_{SAT}, the circuit has a DC problem.

If the circuit is found to have a DC problem and the output is at one of the saturation levels, note the polarity of the output voltage and then measure the two input pins. Ask yourself if the polarity of the input pins would **cause** the output to be at the present saturation limit. If the answer is no, then the op amp is probably defective.

If the input polarity would indeed cause the present output polarity, then mentally examine the circuit paths to determine what signal is supposed to cause the input polarity to change. That is, in order for the output to change (e.g., oscillate), the input pins must have a change. Further, since this is an oscillator, the changing input signal originates at the output. So, if the changing input signal is missing, trace the path between input and output and determine where the signal is lost.

A useful technique in some cases is to force the oscillator (or input) to a given state and monitor the effects elsewhere in the circuit. If the op amp you are using is short-circuit protected, you can directly short the output to ground momentarily while observing the input pins. Ask yourself if the results agree with the behavior of a properly connected circuit.

Distorted Output Waveform. If the oscillator being analyzed is a new design, one common cause for output distortion is an improperly selected op amp. More specifically, if the slew rate of the op amp is not sufficiently high relative to the demands of the oscillator, the output will be distorted.

If the oscillator circuit uses active components as part of the basic oscillator loop (e.g., transistors), a shift in the DC levels in the circuit can cause the active device to move out of its normal range of operation and introduce distortion.

If the waveform distortion is caused by clipping at one of the V_{SAT} levels (unless this is normal behavior for the circuit), look for defects that would affect the DC operating point of the circuit. The first thing to do in this case is to verify proper power supply voltages. Some oscillator configurations can continue to oscillate with dramatic changes in power supply voltages. The symmetry and purity of the output signal, however, may suffer.

Incorrect Frequency of Operation. In certain oscillator designs, nearly every component in the circuit affects the frequency of operation. Troubleshooting a circuit of this type can be streamlined by noting, but not concentrating on, the frequency error. Rather, verify all other aspects of the oscillator's operation (e.g., DC level, waveshape, duty cycle), and if one of these other characteristics is found to be abnormal, focus your attention on this latter problem. The off-frequency problem is probably only a symptom and will be corrected when the other, more easily detected problem is corrected. If all other characteristics appear to be normal, then suspect the components whose sole purpose is for frequency determination and that a change in value will not alter the DC levels in the circuit. There will be very few components that can qualify for this category.

4.7 NONIDEAL CONSIDERATIONS

We have already discussed one of the most significant nonideal op amp characteristics—the slew rate. If the op amp's slew rate is not high enough, the output will be distorted (at best) and the frequency of operation will generally be lower than expected.

Another constraint that can cause problems is the limited current capability of the op amp output. For best performance, stability, and so forth, it is generally wise to avoid heavy loading of an oscillator output—especially if the loads vary. This limitation can easily be overcome by buffering the oscillator output with another op amp configured as a voltage follower.

Unless the application is particularly demanding (e.g., low-frequency drift with temperature changes), the other nonideal parameters do not generally create major problems in oscillator circuits.

REVIEW QUESTIONS

1. In order for a sinewave oscillator to maintain a constant-amplitude (undistorted) output waveform, the overall closed-loop gain must be ____.
2. What is the general name for an oscillator circuit whose frequency is determined by the magnitude of input voltage?
3. Refer to Figure 4.2. This circuit uses (positive, negative) feedback that is (AC, DC) coupled.
4. Refer to Figure 4.2. Will the circuit oscillate if the 1N914A diode becomes open? Explain your answer.
5. Refer to Figure 4.3. What is the primary purpose of resistor R_2?
6. Refer to Figure 4.5. If capacitor C_1 is made larger, what happens to the frequency at the output of A_1? Does the amplitude of the signal at the output of A_2 change?
7. Refer to Figure 4.5. Explain the effect on circuit operation if resistor R_4 is changed to 20 kilohms.
8. Refer to Figure 4.8. If capacitor C_1 is changed to 0.33 microfarad, R_1 is set to 100 kilohms, and R_3 is set to 0, compute the following:
   a. Positive pulse width
   b. Duty cycle
   c. Frequency
9. Refer to Figure 4.12. Amplifier A_2 operates as a ____ circuit.
10. Refer to Figure 4.3. Compute the frequency of operation if R_1, R_2, C_1, and C_2 are changed to the following values:

    $R_1 = R_2 = 4.7\text{ k}\Omega$

    $C_1 = C_2 = 1500\text{ pF}$

CHAPTER FIVE

Active Filters

5.1 FILTER FUNDAMENTALS

A filter, be it an oil filter, a lint filter, a furnace filter, or an active filter, accepts a wide spectrum of inputs, but only passes certain of these inputs through to the output. In some cases, it may pass through the "good stuff" while it catches the "bad stuff." An oil filter in your car is one example. Other applications require a filter to catch the "good stuff" and let the "bad stuff" pass through. A gold prospector's sieve is an example of this type of filter action. In both of the preceding examples, the filter discriminates between "good" and "bad" on the basis of physical size (i.e., size of the dirt particle). In the filters discussed in this chapter, the "good" and "bad" signals will be classified on the basis of their frequency. The input will be a broad range of signal frequencies. The filter will allow a certain range of them to pass and will reject others.

Electronic filters designed to discriminate as a function of frequency can be broadly grouped into five classes:

1. Low pass	Allows frequencies below a specified frequency to pass through the filter circuit.
2. High pass	Allows frequencies above a specified frequency to pass through the filter circuit.
3. Bandpass	Allows a range or band of frequencies to pass through the filter circuit while rejecting frequencies higher or lower than the desired band.
4. Band reject	Rejects all frequencies within a certain band, but passes frequencies higher or lower than the specified band. Also called a band-stop filter.
5. Notch	Essentially a band-stop filter with a very narrow range of frequencies that are rejected.

Figure 5.1 shows the general frequency response curves for each of the basic filter types. The exact nature of a given curve will vary with the type of circuit implementation. Most notably, the slope of the curve between the "pass" and "reject" regions of the filter varies greatly with different filter designs.

There are seemingly endless ways to achieve the various filter functions listed. Each method of implementation has its individual advantages and disadvantages for a particular application. In this chapter, we will select a representative filter design for each basic filter type. In each case, we will discuss its operation, numerically evaluate its performance, and, finally, design one to satisfy a given design goal. Band reject and notch filters will be treated as one general class.

An important consideration regarding active filters is how sharply the frequency response drops off for frequencies outside of the passband of the filter. In general, the steeper the slope of the curve, the more ideal the filter behavior. If the slope becomes too steep, however, the filter becomes unstable and is prone to oscillations. It is common to express the steepness of the slope in terms of dB per decade where a decade represents a factor of 10 increase or decrease in frequency. For example, suppose a low-pass filter had a 20-dB-per-decade slope beyond the cutoff frequency. This means that if the input frequency is increased by a factor of 10, then the output will decrease by 20 dB. If the input frequency is again increased by a factor of 10, then the output will decrease another 20 dB, or 40 dB from the first measurement. Typical filter circuits have slopes ranging from 6 to 60 dB per decade or more.

In the case of bandpass, bandstop, and notch filters, we often describe the steepness of the slopes in another way. The ratio of the center frequency (f_C) to the bandwidth (*bw*) gives us an indication of the sharpness of the cutoff region.

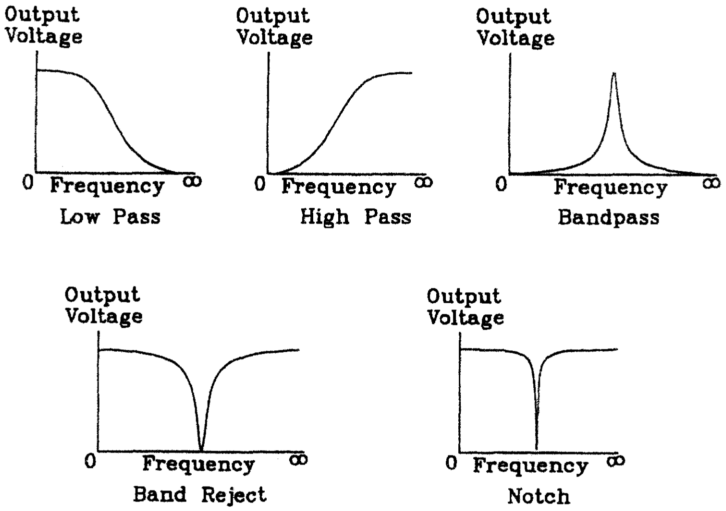


FIGURE 5.1 Theoretical response curves for the five basic classes of filter circuits.

The ratio f_C/bw is called the Q of the circuit. The higher the Q, the sharper the cutoff slopes of the filter.

The term Q is also used with reference to low-pass and high-pass filters, but it must be interpreted differently. The output of some filters peaks just before the edge of the passband. The Q of the filter indicates the degree of peaking. A Q of 1 has only a slight peaking effect. A Q of less than 1 reduces this peaking, while a Q greater than 1 causes a more pronounced peaking. There is usually a trade-off between peaking (generally undesired) and steepness (generally desired) of the slope. The high- and low-pass filter designs in this chapter use a Q of 0.707, which produces a very flat response.

5.2 LOW-PASS FILTER

Figure 5.2 shows one of the most common implementations of the low-pass filter circuit. This particular configuration is called a Butterworth filter and is characterized by a very flat response in the passband portion of its response curve.

Ideally, a low-pass filter will pass frequencies from DC up through a specified frequency, called the *cutoff frequency*, with no attenuation or loss. Beyond the cutoff frequency, the filter ideally offers infinite attenuation to the signal. In practice, however, the transition from passband to stopband is a gradual one. The cutoff frequency is defined as the frequency that passes with a 70.7-percent response. This, of course, is the familiar half-power point referenced in basic electronics theory.

5.2.1 Operation

Let us try to understand the operation of the low-pass filter circuit shown in Figure 5.2 from an intuitive or logical standpoint before evaluating it numerically. First, mentally open-circuit the capacitors. This modified circuit is shown in Figure 5.3, which is essentially how the circuit will look at low frequencies when the capacitive reactance of the capacitors is high. We can see that this amplifier is connected as a simple voltage follower circuit. Resistor R_3 is included in the feedback loop to compensate for the effects of bias currents flowing through R_1 and R_2. For low frequencies, then, we expect to have a voltage gain of about unity.

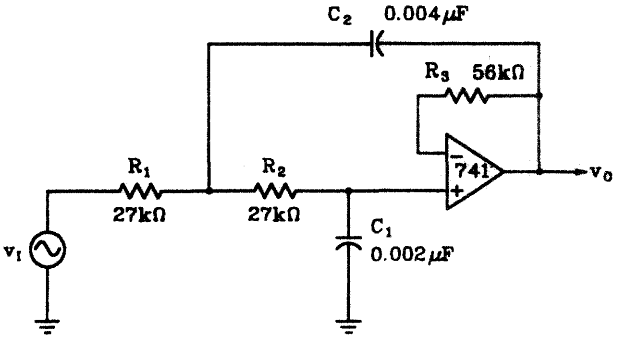


FIGURE 5.2 A low-pass Butterworth filter circuit.

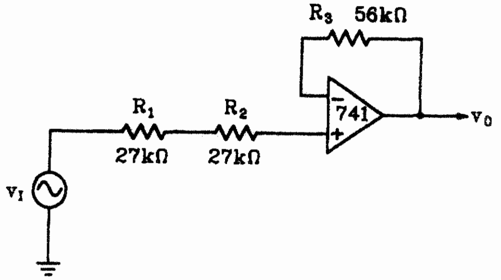


FIGURE 5.3 A low-frequency equivalent circuit for the low-pass filter shown in Figure 5.2.

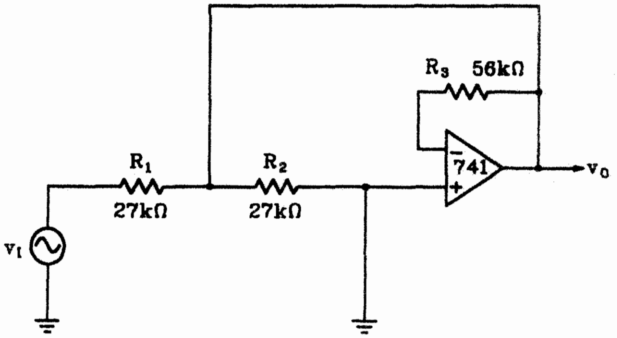


FIGURE 5.4 A high-frequency equivalent circuit for the low-pass filter shown in Figure 5.2.

Now let us mentally short-circuit the capacitors in Figure 5.2 to get an idea of how the circuit looks to high frequencies where the capacitive reactance is quite low. This equivalent circuit is shown in Figure 5.4.

First, notice that the (+) input of the amplifier is essentially grounded. This should eliminate any chance of signals passing beyond this point. The junction of R_1 and R_2 is effectively connected to the output of the op amp. This, you will recall, is a very low impedance point, so for high frequencies, the junction of R_1 and R_2 also has a low impedance to ground.

As our preliminary analysis indicates, the low frequencies should receive a voltage gain of about 1, and the high frequencies should be severely attenuated. We are now ready to confirm this numerically.

5.2.2 Numerical Analysis

The three primary considerations in active filters are

1. Cutoff frequency
2. Q
3. Input impedance

Cutoff Frequency. In the case of the circuit in Figure 5.2, the cutoff frequency is the frequency that causes the output amplitude to be 70.7 percent of the input. We can compute this frequency with Equation (5.1),

$$f_C = \frac{1}{2\pi R\sqrt{C_1 C_2}} \tag{5.1}$$

where $R = R_1 = R_2$. For the circuit in Figure 5.2, the cutoff frequency is computed as follows:

$$f_C = \frac{1}{6.28 \times 27\ k\Omega\sqrt{0.002\ \mu F \times 0.004\ \mu F}} = 2.09\ kHz$$

Filter Q. The Q of the circuit in Figure 5.2 is computed with Equation (5.2).

$$Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}} \tag{5.2}$$

In our present case, we have

$$Q = \frac{1}{2}\sqrt{\frac{0.004\ \mu F}{0.002\ \mu F}} = 0.707$$

The value of 0.707 produces a maximally flat curve in the passband. That is, the response curve has minimal peaking at the edge of the passband. This is a common choice for Q.

Input Impedance. The input impedance is an important consideration because it determines the amount of loading presented by the filter to the circuit driving the filter. The exact value of input impedance will vary dramatically with frequency. At very low frequencies, the input impedance approaches that of the standard voltage follower amplifier. As the input frequency increases, the input impedance decreases. The ultimate limit for the dropping input impedance is the value of R_1. Expressing this as an equation gives us

$$Z_{IN}(\text{min}) = R_1 \tag{5.3}$$

In the case of the circuit in Figure 5.2, we can be assured that the input impedance will never be lower than 27 kilohms.

5.2.3 Practical Design Techniques

Let's now design a low-pass filter similar to the circuit in Figure 5.2. The design goal for our filter is

1. Cutoff frequency	1.5 kilohertz
2. Q	0.707
3. Input impedance	>10 kilohms

Compute the Ratio of C_2/C_1. From Equation (5.2), we can see that the ratio of C_2/C_1 determines the Q of the circuit. Therefore, since we know Q (from the design criteria), we can compute the capacitor ratio by transposing Equation (5.2).

$$Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}},\ or$$

$$\frac{C_2}{C_1} = 4Q^2$$

$$= 4(0.707)^2$$

$$= 2$$

This tells us that C_2 will have to be twice as large as C_1. In general, the value of C_2 is determined with Equation (5.4).

$$C_2 = 4Q^2 \times C_1 \tag{5.4}$$

We can now select C_1 to be any convenient value and then double it to get C_2. For this design, let us choose C_1 as a 3300-picofarad capacitor. We can then make C_2 a 6600-picofarad ideally, or perhaps a 6800-picofarad as this is a standard size.

Compute R_1 and R_2. R_1 and R_2 should be within the general range of 1.0 to 220 kilohms. And, of course, R_1 must be larger than the minimum required input impedance (10 kilohms in this case). If the following calculation produces a value for R_1 and R_2 that does not comply with these restrictions, then a different value must be selected for C and the resistor values recalculated. We compute the resistance value by applying Equation (5.1).

$$f_C = \frac{1}{2\pi R\sqrt{C_2C_1}},\ or$$

$$R = \frac{1}{2\pi f_C\sqrt{C_2C_1}}$$

$$= \frac{1}{6.28 \times 1.5\ kHz\sqrt{6800\ pF \times 3300\ pF}}$$

$$= 22.4\ k\Omega$$

We will use a standard value of 22 kilohms for R_1 and R_2.

Determine the Value of R_3. The value for resistor R_3 is calculated in the same way as for a simple voltage follower. That is, we want equal DC resistances between each op amp input and ground. For the circuit in Figure 5.2, we can compute R_3 with Equation (5.5).

$$R_3 = R_1 + R_2 \tag{5.5}$$

Substituting values for our present circuit gives us

$$R_3 = 22\ k\Omega + 22\ k\Omega = 44\ k\Omega$$

We will select the nearest standard value of 47 kilohms for R_3.

Select the Op Amp. There are three op amp parameters that we should evaluate before specifying a particular op amp for our low-pass filter:

1. Bandwidth
2. Slew rate
3. Op amp corner frequency

Since our op amp is operated as a voltage follower, the required bandwidth of the amplifier is essentially the same as the cutoff frequency. That is,

$$f_{UG}(\text{min}) = f_C \tag{5.6}$$

In the case of our present circuit, our op amp must have a bandwidth of greater than 1.5 kilohertz. In many cases, including this one, the bandwidth will not be a limiting factor because the op amp is operated at unity gain.

The minimum required slew rate for the op amp can be estimated with Equation (5.7),

$$slew\ rate(\text{min}) = \pi f_C v_O(\text{max}) \tag{5.7}$$

where f_C is the filter cutoff frequency and v_O is the highest expected peak-to-peak output swing. If the application clearly has externally imposed limits on the maximum output amplitude, then use them. If the maximum output amplitude is not specifically known, as in the present case, then design for worst case and assume that the signal will swing between the $\pm V_{SAT}$ levels. In the present circuit, the required op amp slew rate (using ±13 volts as the saturation limits) is computed as

$$slew\ rate(\text{min}) = 3.14 \times 1.5\ kHz \times 26\ V = 0.122\ V/\mu s$$

Finally, the minimum op amp corner frequency may be estimated with Equation (5.8),

$$\boxed{f_{BREAK}(\text{min}) = \frac{40 f_C}{A_{OL}} \qquad (5.8)}$$

where A_{OL} is the low-frequency, open-loop gain of the op amp and f_C is the filter cutoff frequency. The corner frequency of the op amp is the one where the open-loop gain has dropped to 70.7 percent of its low-frequency or DC value. If we choose a 741 ($A_{OL} = 50{,}000$), it must have a corner frequency greater than

$$f_{BREAK}(\text{min}) = \frac{40 \times 1.5\ kHz}{50{,}000} = 1.2\ Hz$$

Let us consider a 741 op amp for this application. Appendix 1 lists the data for the 741. The minimum bandwidth and slew rate requirements for our application are exceeded by the 741's ratings. By referring to the graph of open-loop frequency response in Appendix 1, we can estimate the corner frequency of the 741 as about 5 hertz. Again, this exceeds our requirements, so let us choose a 741 for our design.

The schematic diagram of our completed low-pass filter design is shown in Figure 5.5. This circuit configuration provides a theoretical roll-off slope of 40 dB per decade. The oscilloscope plots in Figure 5.6 indicate the actual behavior of the circuit. The filter shifts the phase of different frequencies by differing amounts as evidenced in the figure. This is important in certain applications. Finally, Table 5.1 contrasts the original design goal with the measured performance of the circuit.

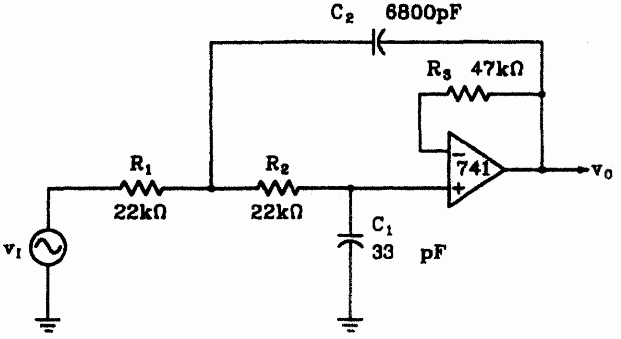
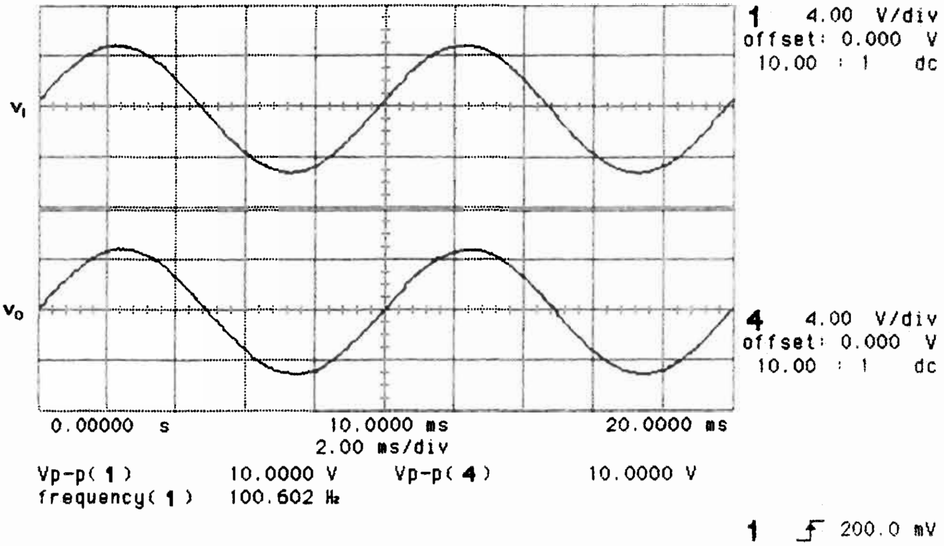


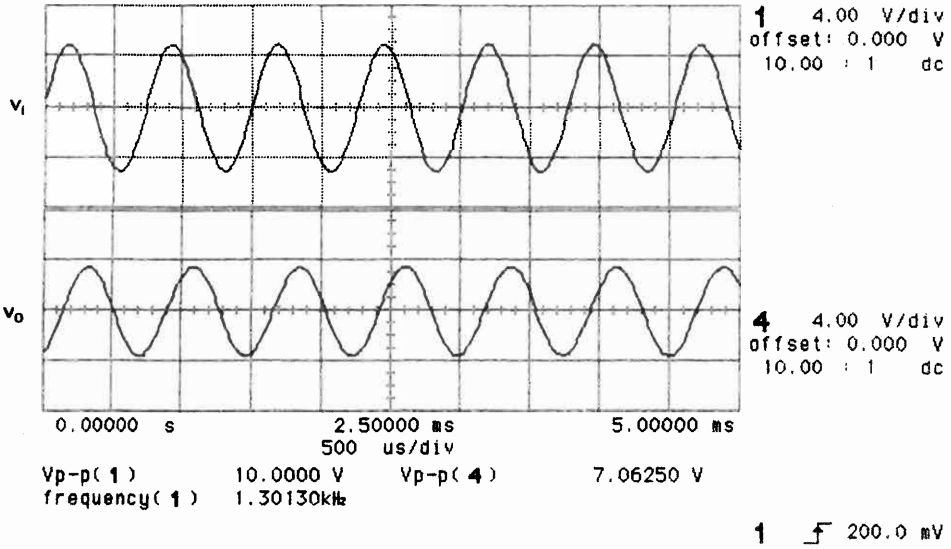
FIGURE 5.5 A low-pass filter designed for a cutoff frequency of 1.5 kilohertz.

Below the Cutoff Frequency



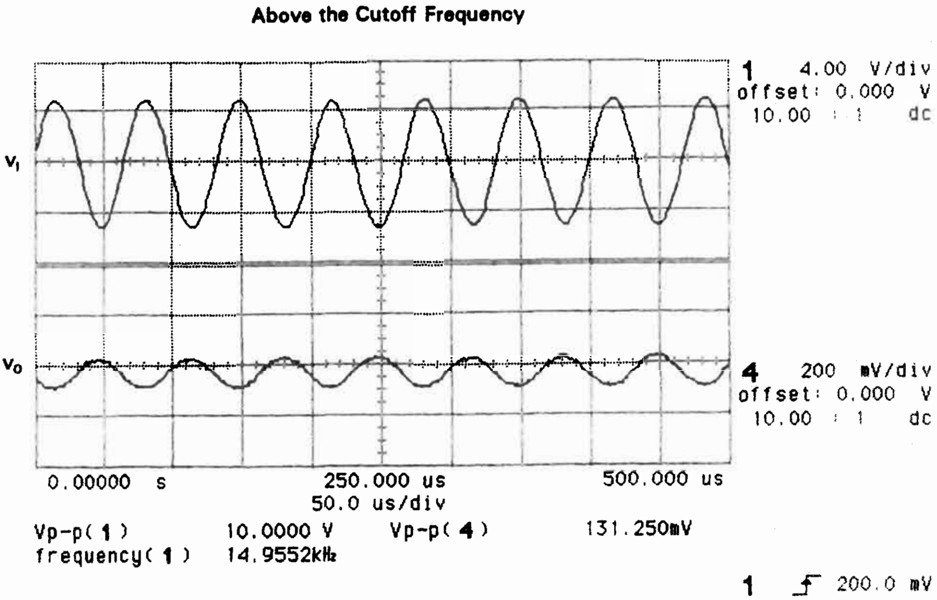
(a)

At the Cutoff Frequency



(b)

FIGURE 5.6 Actual circuit performance of low-pass filter shown in Figure 5.5. (Test equipment courtesy of Hewlett-Packard Company.)


Above the Cutoff Frequency
V_I
V_O
1 4.00 V/div
offset: 0.000 V
10.00 : 1 dc
4 200 mV/div
offset: 0.000 V
10.00 : 1 dc
0.00000 s
250.000 us
50.0 us/div
500.000 us
Vp-p(1) 10.0000 V
frequency(1) 14.9552kHz
Vp-p(4) 131.250mV
1 200.0 mV

(c)

FIGURE 5.6 *Continued*

TABLE 5.1

	Design Goal	*Measured Value*
Cutoff frequency	1.5 kilohertz	1.3 kilohertz
Input impedance (min)	>10 kilohms	>22 kilohms

5.3 HIGH-PASS FILTER

Figure 5.7 shows the schematic diagram of a high-pass filter circuit that provides a theoretical roll-off slope of 40 dB per decade. The circuit configuration is obtained by changing positions with all of the resistors and capacitors (except R_3) in the low-pass equivalent (Figure 5.2). As a high-pass filter, we will expect it to severely attenuate signals below a certain frequency and pass the higher frequencies with minimal attenuation.

5.3.1 Operation

An intuitive feel for the operation of the circuit in Figure 5.7 can be gained by picturing the equivalent circuit at very low and very high frequencies. At very low frequencies, the capacitors will have a high reactance and will begin to appear as open circuits. Figure 5.8 shows the low-frequency equivalent circuit for the high-pass filter shown in Figure 5.7. As you can readily see, the amplifier acts as a unity

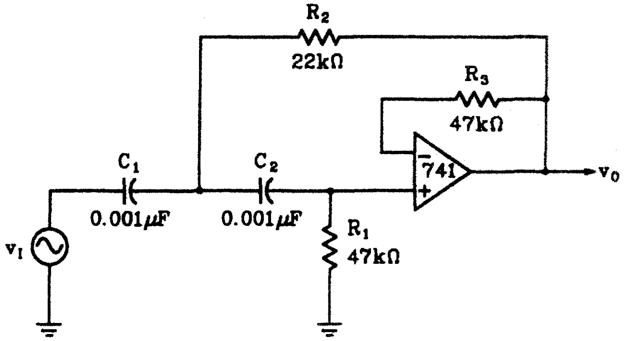

R₂
22kΩ
R₃
47kΩ
C₁
0.001μF
C₂
0.001μF
741
R₁
47kΩ
v_I
v_O

FIGURE 5.7 A 40-dB-per-decade high-pass filter circuit.

gain circuit, but **it has no input signal**. At low frequencies, we expect little or no output signal.

At high frequencies, the capacitors will have a low reactance and will begin to appear as short circuits. The high-frequency equivalent circuit is shown in Figure 5.9. Here we see that the capacitors have been replaced with direct connections. Also, resistor R_2 has been removed, because it is connected between two points that have the same signal amplitude and phase (i.e., input and output of a voltage follower). Because it has the same potential on both ends, it will have no current flow and is essentially open. The resulting equivalent circuit indicates that for high frequencies, our high-pass filter will act as a simple voltage follower.

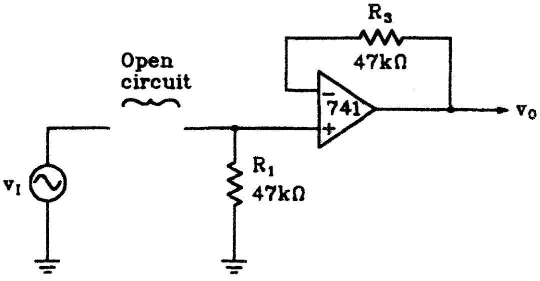

R₃
47kΩ
Open circuit
741
R₁
47kΩ
v_I
v_O

FIGURE 5.8 A low-frequency equivalent circuit for the high-pass filter shown in Figure 5.7.

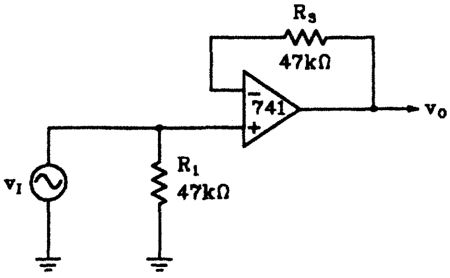

R₃
47kΩ
741
R₁
47kΩ
v_I
v_O

FIGURE 5.9 A high-frequency equivalent circuit for the high-pass filter shown in Figure 5.7.

5.3.2 Numerical Analysis

Let us now extend our look at the high-pass filter shown in Figure 5.7 to a numerical analysis. There are three primary characteristics that we will want to determine:

1. Cutoff frequency
2. Q
3. Input impedance

Cutoff Frequency. The cutoff frequency for a high-pass filter is the frequency that causes the output voltage to be 70.7 percent of the amplitude of signals in the passband (i.e., the higher range of frequencies in this case). We can determine the cutoff frequency for the circuit in Figure 5.7 by applying Equation (5.9).

$$f_C = \frac{1}{2\pi C\sqrt{R_1 R_2}} \tag{5.9}$$

For the values in our present circuit, the cutoff frequency is computed as

$$f_C = \frac{1}{6.28 \times 0.001\ \mu F\sqrt{47\ k\Omega \times 22\ k\Omega}} = 4.95\ kHz$$

Filter Q. The Q of the circuit shown in Figure 5.7 is computed with Equation (5.10).

$$Q = \frac{1}{2}\sqrt{\frac{R_1}{R_2}} \tag{5.10}$$

For the values given in Figure 5.7, the Q is computed as

$$Q = \frac{1}{2}\sqrt{\frac{47\ k\Omega}{22\ k\Omega}} = 0.731$$

If the resistor values had an exact ratio of 2:1, the Q would equal 0.707 and the passband response would be maximally flat.

Input Impedance. The input impedance of the circuit shown in Figure 5.7 varies inversely with the input frequency. The limit, however, is established by R_1 in parallel with the input impedance of the voltage follower. Therefore, for practical purposes, the limit is established by the value of R_1. In our present case, the minimum input impedance will be 47 kilohms.

5.3.3 Practical Design Techniques

Let us now design a high-pass filter similar to the circuit shown in Figure 5.7. We will use the following as our design goals:

1. Cutoff frequency	300 hertz
2. Q	0.707
3. Input impedance	> 2000 ohms
4. Highest input frequency	5000 hertz

Determine the R_1/R_2 ratio. As indicated by Equation (5.10), the ratio of R_1 to R_2 determines the Q of the circuit. Let us apply Equation (5.10) to determine the required ratio for our present design.

$$Q = \frac{1}{2}\sqrt{\frac{R_1}{R_2}},\ or$$

$$\frac{R_1}{R_2} = 4Q^2$$

$$= 4(0.707)^2$$

$$= 2$$

Now we know that resistor R_1 will be twice as large as R_2. In general, R_1 is computed with Equation (5.11).

$$R_1 = 4Q^2 \times R_2 \qquad (5.11)$$

We can pick any convenient set of values for these resistors provided they fall within the suggested range of 1.0 to 470 kilohms, and as long as R_1 is larger than the minimum input impedance specified in the design criteria. For our present example, let us choose R_2 as 10 kilohms. R_1 is simply twice this value, or 20 kilohms.

Compute the Value of C_1 and C_2. Capacitors C_1 and C_2 are equal in value and can be computed by applying Equation (5.9).

$$f_C = \frac{1}{2\pi C\sqrt{R_1 R_2}},\ or$$

$$C = \frac{1}{2\pi f_C\sqrt{R_1 R_2}}$$

$$= \frac{1}{6.28 \times 300\ Hz\sqrt{20\ k\Omega \times 10\ k\Omega}}$$

$$= 0.0375\ \mu F$$

We will select a standard value of 0.033 microfarad for both capacitors.

Compute the Value of R_3. Resistor R_3 is included to reduce the effects of the op amp bias current that flows through R_1. R_3 is set equal to R_1, or simply

$$R_3 = R_1 \tag{5.12}$$

In our case, we will use a 20-kilohm resistor for R_3.

Select the Op Amp. The following op amp parameters are the most essential when designing a high-pass filter circuit:

1. Bandwidth
2. Slew rate

Additionally, if it is necessary to use high-resistance values, then every effort should be made to use an op amp with low-bias currents.

Bandwidth. When we construct a high-pass filter with an op amp, we inherently build a bandpass filter. That is, our filter circuit, by design, will attenuate all frequencies below the cutoff frequency. Ideally, all frequencies above the cutoff frequency should be passed with minimal attenuation. In practice, however, the gain of our op amp falls off at high frequencies. Thus, the very high frequencies are attenuated by the reduced gain of the op amp.

When selecting an op amp for a particular application, we must ensure that the amplifier gain is still adequate at the highest expected frequency of operation. Since the op amp is configured for unity gain, we simply need to be sure that it has a unity gain bandwidth (f_{UG}) that is higher than the highest input frequency. In the present case, the highest input frequency is cited as 5000 hertz. Therefore, our choice of op amps must have a unity gain frequency greater than that. This should be an easy task.

Slew Rate. The slew rate limitation of the op amp restricts the highest frequency that we can properly amplify at a given amplitude. Since the maximum input amplitude was not specified in the design goals, we will assume that the output may produce a full swing between $\pm V_{SAT}$. Equation (5.7) can be used to estimate the required op amp slew rate for our present application:

$$\begin{aligned} \textit{slew rate}(\text{min}) &= \pi f_C v_O(\text{max}) \\ &= 3.14 \times 5\ kHz \times 26\ V \\ &= 0.408\ V/\mu s \end{aligned}$$

Both bandwidth and slew rate requirements are within the capabilities of a standard 741 op amp. Let us plan to use this device in our design.

This completes the design of our high-pass filter circuit. The final schematic is shown in Figure 5.10, and the oscilloscope plots shown in Figure 5.11 indicate the performance of the circuit. Note the varying phase shifts for different frequencies. Additionally, Table 5.2 compares the original design goals with the actual measured circuit performance. The measured cutoff frequency is somewhat higher than the original design goal, for two reasons: First, we chose to use standard values of 0.033 microfarad for the capacitors when the correct value was 0.0375 microfarad; second, the capacitors used to build the circuit were actually 0.032 microfarad (0.022 μF || 0.01 μF) because of availability. If the exact cutoff frequency is needed, then the resistors can be made variable.

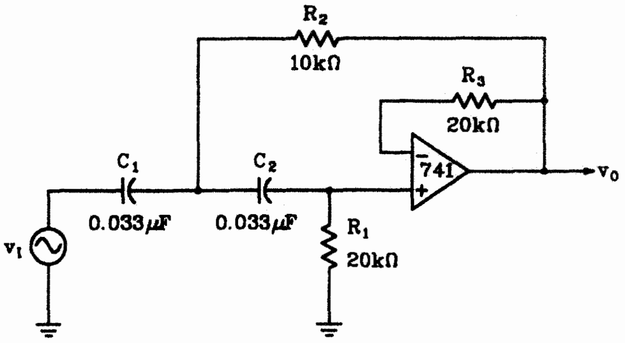
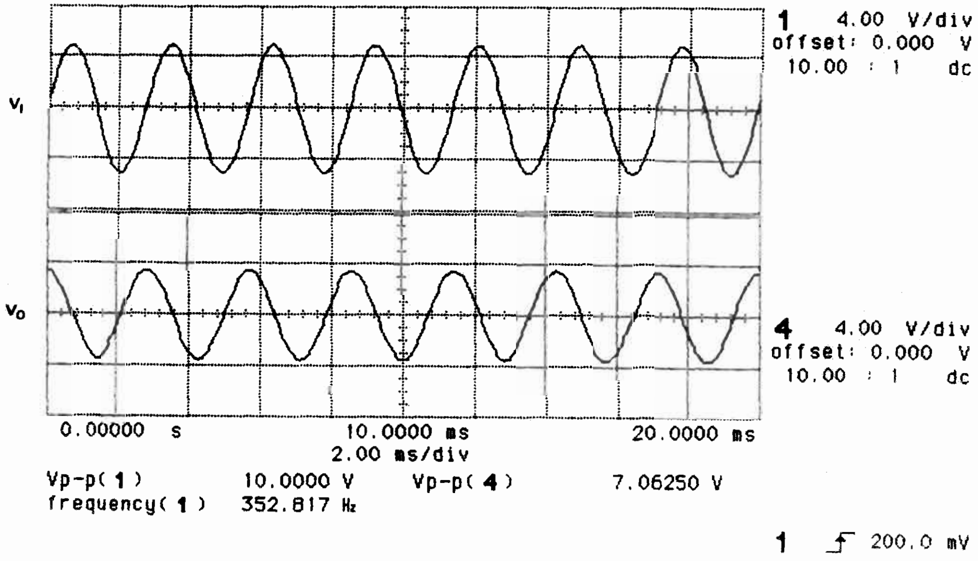


FIGURE 5.10 A high-pass filter designed for a flat response and a cutoff frequency of 300 hertz.

At the Cutoff Frequency



1 4.00 V/div
offset: 0.000 V
10.00 : 1 dc

4 4.00 V/div
offset: 0.000 V
10.00 : 1 dc

2.00 ms/div

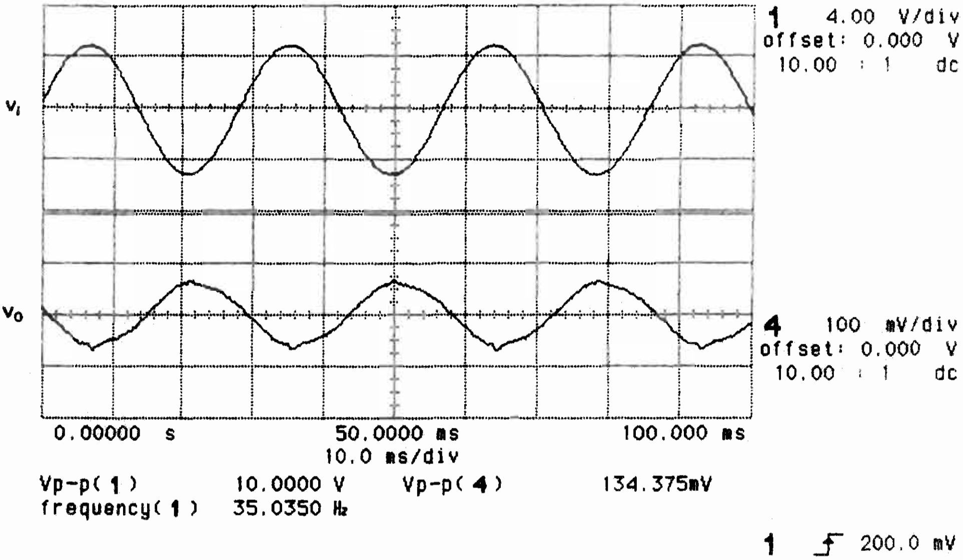
Vp-p(1) 10.0000 V Vp-p(4) 7.06250 V
frequency(1) 352.817 Hz

1 200.0 mV

(a)

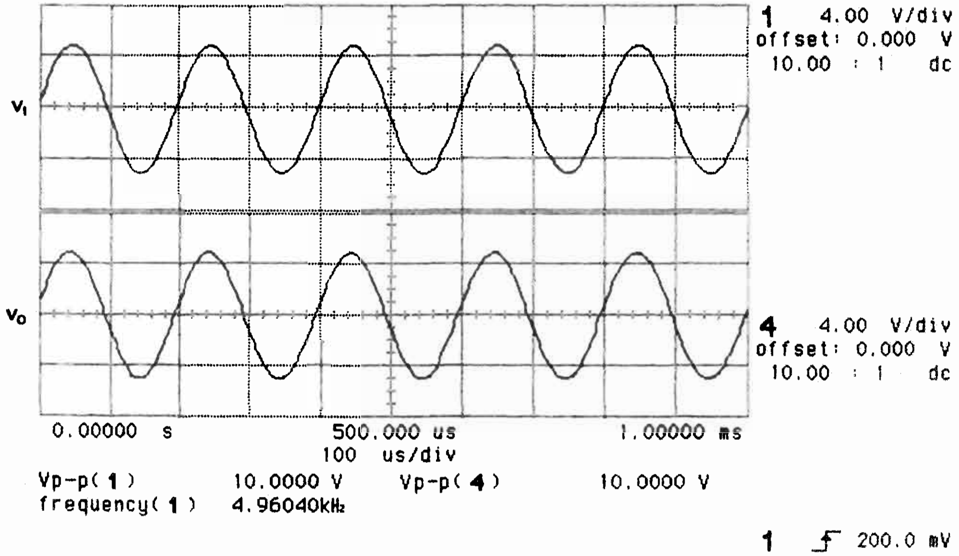
FIGURE 5.11 Actual circuit performance of the high-pass filter shown in Figure 5.10. (Test equipment courtesy of Hewlett-Packard Company.)

Below the Cutoff Frequency



(b)

Above the Cutoff Frequency



(c)

FIGURE 5.11 *Continued*

TABLE 5.2

	Design Goal	*Measured Value*
Cutoff frequency	300 hertz	352.8 hertz
Input impedance	>2000 ohms	>10 kilohms

5.4 BANDPASS FILTER

Figure 5.12 shows the schematic diagram of a bandpass filter. This circuit provides maximum gain (or minimum loss) to a specific frequency called the **resonant,** or **center, frequency** (even though it may not actually be in the center). Additionally, it allows a range of frequencies on either side of the resonant frequency to pass with little or no attenuation, but severely reduces frequencies outside of this band. The edges of the passband are identified by the frequencies where the response is 70.7 percent of the response for the resonant frequency.

The range of frequencies that make up the passband is called the **bandwidth** of the filter. This can be stated as

$$bw = f_H - f_L \tag{5.13}$$

where f_H and f_L are the frequencies that mark the edges of the passband. The Q of the circuit is a way to describe the ratio of the resonant frequency (f_R) to the bandwidth (bw). That is,

$$Q = \frac{f_R}{bw} \tag{5.14}$$

If the Q of the circuit is 10 or less, we call the filter a wide-band filter. Narrow-band filters have values of Q over 10. In general, higher Qs produce sharper, more well-defined responses. If the application requires a Q of 20 or less, then a single op

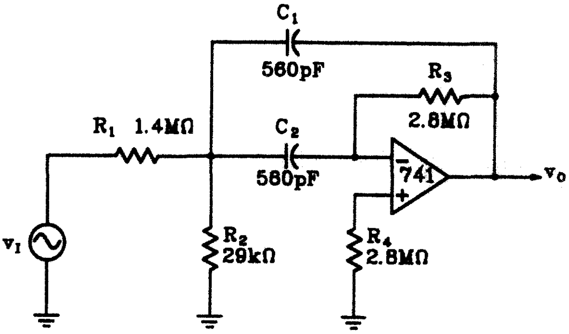


FIGURE 5.12 A bandpass filter used for a numerical analysis example.

amp filter circuit can be used. For higher Qs, a cascaded filter should be used to avoid potential oscillation problems.

5.4.1 Operation

To help us gain an intuitive understanding of the circuit's operation, let us draw equivalent circuits for the filter shown in Figure 5.12 at very high and very low frequencies. To obtain the low-frequency equivalent where the capacitors have a high reactance, we simply open-circuit the capacitors. Figure 5.13 shows the low-frequency equivalent; it is obvious from it that the low frequencies will never reach the amplifier's input and therefore cannot pass through the filter.

At high frequencies, the reactance of the capacitors will be low and the capacitors will begin to act like short circuits. Figure 5.14 shows the high-frequency equivalent circuit, which was obtained by short-circuiting all of the capacitors. From this equivalent circuit, we can see that the high frequencies will be attenuated by the voltage divider action of R_1 and R_2. Additionally, the amplifier has 0 resistance in the feedback loop, which causes our voltage gain to be 0 for the op amp (i.e., no output).

At some intermediate frequency (determined by the component values), the gain of the amplifier will offset the loss in the voltage divider (R_1 and R_2) and the signals will be allowed to pass through. The circuit is frequently designed to have unity gain at the resonant frequency, but may be set up to provide some amplification.

5.4.2 Numerical Analysis

The numerical analysis of the filter shown in Figure 5.12 can range from very "messy" to straightforward, depending on the ratios of the components. That is, each component except R_4 affects both frequency and Q of the filter. The following

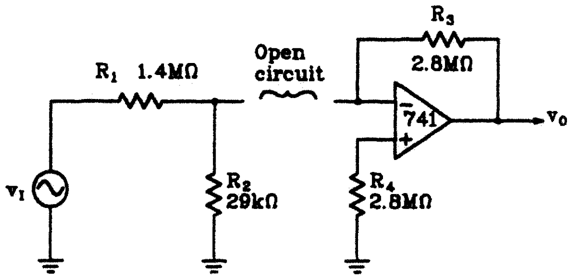


FIGURE 5.13
A low-frequency equivalent circuit for the bandpass filter shown in Figure 5.12.

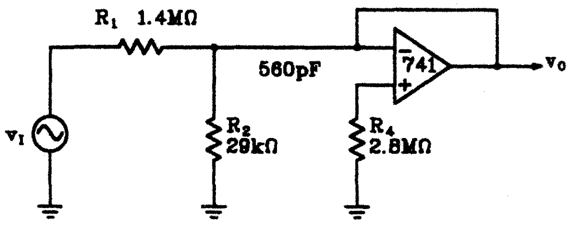


FIGURE 5.14
A high-frequency equivalent circuit for the bandpass filter shown in Figure 5.12.

analytical method assumes that the filter was designed according to standard practices. The checks below will provide you with a reasonable degree of assurance that the filter design is compatible with the analytical procedure to be described:

1. Is R_3 approximately twice the size of R_1?
2. Are C_1 and C_2 equal in value?
3. Is R_1 at least 10 times the size of R_2?

If the answer is yes to *all* of these questions (which is the typical case), then the filter can be analyzed as described below. We will compute the following characteristics:

1. Resonant frequency
2. Q
3. Bandwidth
4. Voltage gain

Filter Q. The Q of the filter shown in Figure 5.12 can be computed with the following equation:

$$Q = \sqrt{\frac{R_1 + R_2}{2R_2}} \tag{5.15}$$

Substituting values gives us

$$Q = \sqrt{\frac{1.4\ M\Omega + 29\ k\Omega}{2 \times 29\ k\Omega}} = 4.96$$

Since the Q is less than 10, we will classify this circuit as a wide-band filter.

Resonant Frequency. The resonant frequency of the filter shown in Figure 5.12 can be computed with the following equation:

$$f_R = \frac{2Q}{2\pi R_3 C} \tag{5.16}$$

where C is the value of either C_1 or C_2. Calculations for the present circuit are

$$f_R = \frac{2 \times 4.96}{6.28 \times 2.8\ M\Omega \times 560\ pF} = 1.01\ kHz$$

It is this frequency that should receive the most amplification (or least attenuation) from the filter circuit.

Bandwidth. The bandwidth of the filter can be calculated by applying a transposed version of Equation (5.14).

$$Q = \frac{f_R}{bw}, \text{ or}$$

$$\begin{aligned} bw &= \frac{f_R}{Q} \\ &= \frac{1.01\ kHz}{4.96} \\ &= 204\ Hz \end{aligned}$$

Thus, the range of frequencies that is amplified at least 70.7 percent as much as the resonant frequency is 204 hertz wide.

Voltage Gain at the Resonant Frequency. The voltage gain at the resonant frequency can be estimated with Equation (5.17).

$$A_V = \frac{Q}{2\pi R_1 f_R C} \tag{5.17}$$

In the case of the circuit in Figure 5.12, the voltage gain is computed as

$$A_V = \frac{4.96}{6.28 \times 1.4\ M\Omega \times 1.01\ kHz \times 560\ pF} = 0.997$$

5.4.3 Practical Design Techniques

We are now ready to design a bandpass filter to satisfy a given design requirement. Let us design a filter similar to the circuit in Figure 5.12 that will perform according to the following design goals:

1. Resonant frequency	8 kilohertz
2. Q	10
3. Voltage gain at f_R	Unity
4. Bandwidth	800 hertz

The following design is based on the assumption that the circuit provides unity gain at the resonant frequency. Although common in practice, how to design a filter to have a voltage gain of greater than unity at the resonant frequency will also be shown.

Select C_1 and C_2. Although the selection of these capacitors is somewhat arbitrary, our choice of values for C_1 and C_2 will ultimately determine the values for the resistors. If our subsequent calculations result in an impractical resistance value, we will have to select a different value for C_1 and C_2 and recompute the resistance values. Because of the wide range of resistance values typically required in a given design, it is not uncommon to have resistance values ranging from 1000 ohms or less to well into the megohm ranges. Nevertheless, it should remain a goal to keep the resistance values above 1 kilohm and below 1 megohm if practical. The lower limit is established by the output drive of the op amp and the effects on input impedance. The upper limit is established by the op amp bias currents and circuit sensitivity. That is, if the resistance values are very large, then the voltage drops due to op amp bias currents become more significant. Additionally, if the resistances in the circuit are excessively high, then the circuit is far more prone to interference from outside noise, nearby circuit noise, or even unwanted coupling from one part of the filter to another. For our initial selection, let us choose to use 0.001-microfarad capacitors for C_1 and C_2.

Compute the Value of R_1. The value of resistor R_1 is computed with Equation (5.18).

$$R_1 = \frac{Q}{2\pi A_V f_R C} \tag{5.18}$$

In the case of the present design, we compute the value for R_1 as

$$R_1 = \frac{10}{6.28 \times 1 \times 8\ kHz \times 0.001\ \mu F} = 199\ k\Omega$$

We will plan to use a standard value of 200 kilohms. It should be noted, however, that the component values in an active filter are generally more critical than in many other types of circuits, so if close adherence to the original design goals is required, use either variable resistors for trimming or fixed resistors in a series and/or parallel combination, or use precision resistors.

Compute the Value for R_2. Resistor R_2 is calculated with Equation (5.19).

$$R_2 = \frac{R_1 A_V}{2(2\pi f_R C R_1 A_V)^2 - A_V} \tag{5.19}$$

For our present design, we compute R_2 as follows:

$$R_2 = \frac{199\ k\Omega \times 1}{2(6.28 \times 8\ kHz \times 0.001\ \mu F \times 199\ k\Omega \times 1)^2 - 1} = 1.0\ k\Omega$$

Compute the Value for R_3. Resistor R_3 is computed by simply doubling the value of R_1. That is,

$$R_3 = 2R_1 \tag{5.20}$$

For our design, we compute R_3 as

$$R_3 = 2 \times 200\ k\Omega = 400\ k\Omega$$

The nearest standard value is 390 kilohms. As previously stated, if the application requires greater compliance with the original design goals, use either a variable resistor or a combination of fixed resistors to achieve the exact value required. In our case, we will use two 200-kilohm resistors in series for R_3.

Determine the Value for R_4. Resistor R_4 has no direct effect on the frequency response of the filter circuit. Rather, it is included to help compensate for the effects of the op amp bias current that flows through R_3. You will recall that we try to keep equal the resistances between ground and the (+) and (–) input pins of the op amp. Therefore, we will set R_4 equal to R_3. In equation form, we have

$$R_4 = R_3 \tag{5.21}$$

In this case, it is probably not necessary to use a variable resistor or fixed resistor combination to obtain an exact resistance. We will simply use the nearest standard value of 390 kilohms for R_4.

Select the Op Amp. We will pay particular attention to the following op amp parameters when selecting an op amp for our active filter:

1. Bandwidth
2. Slew rate

If the resistance values turn out to be quite high, then an op amp with particularly low bias current will be important. If the capacitance values must be below about 270 picofarads, then select an op amp with minimum internal capacitances.

Bandwidth. The required bandwidth of our op amp is determined by the highest frequency that must pass the circuit. This is, of course, the upper cutoff frequency (f_H) and can be approximated (for our purposes) with Equation (5.22).

$$f_H = f_R + \frac{bw}{2} \tag{5.22}$$

In the present case, f_H is estimated as

$$f_H = 8\ kHz + \frac{800\ Hz}{2} = 8.4\ kHz$$

The required bandwidth for the op amp is computed in the same manner as described in Chapter 2. It can be computed as

$$\begin{aligned} f_{UG} &= A_V f_H \\ &= 1 \times 8.4\ kHz \\ &= 8.4\ kHz \end{aligned}$$

This is well within the capabilities of the standard 741 op amp.

Slew Rate. The minimum slew rate for the op amp can be computed with Equation (5.7).

$$\begin{aligned} slew\ rate(\mathrm{min}) &= \pi f_H v_O(\mathrm{max}) \\ &= 3.14 \times 8.4\ kHz \times 26\ V \\ &= 0.686\ V/\mu s \end{aligned}$$

This exceeds the capability of the standard 741, which has a 0.5-volts-per-microsecond slew rate. We will use an MC1741SC for our design because it satisfies both the bandwidth and slew rate requirements of our design.

The schematic of our final design is shown in Figure 5.15. Its performance is indicated by the oscilloscope plots in Figure 5.16. Be sure to note the varying phase shifts at different frequencies. Finally, the design goals are contrasted with the actual measured performance of the circuit in Table 5.3.

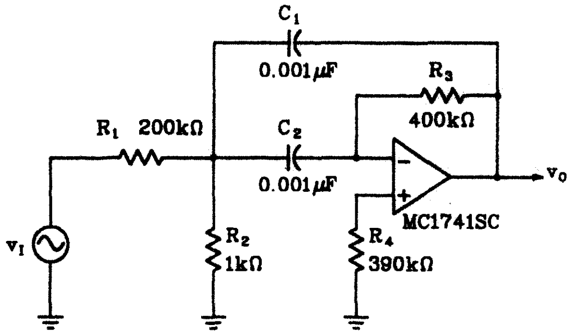
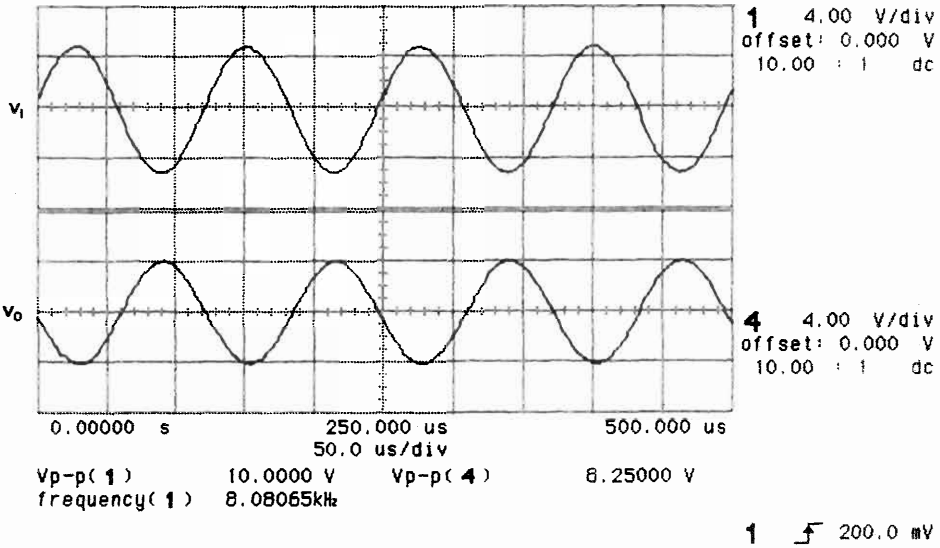


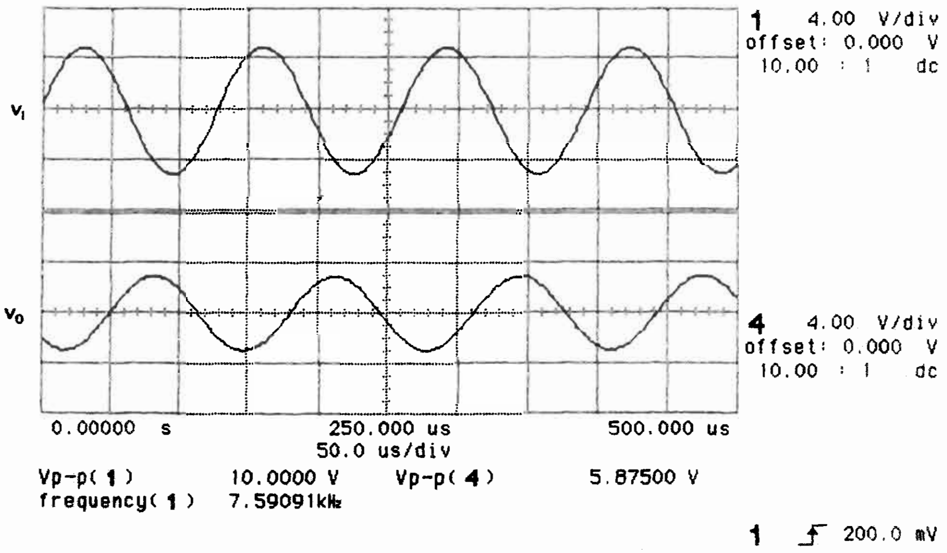
FIGURE 5.15 A bandpass filter designed for a center frequency of 8000 hertz and a Q of 10.

At Center Frequency



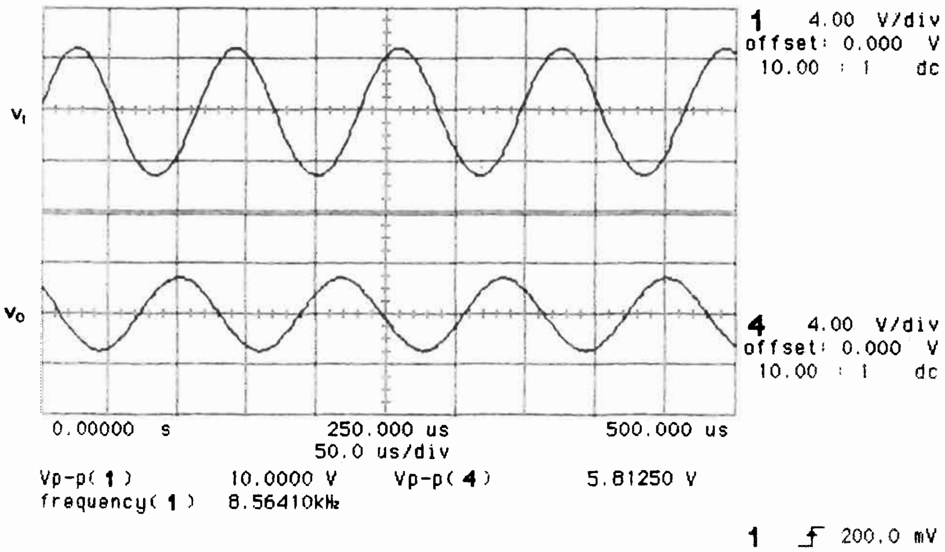
(a)

At the Lower Cutoff Frequency



(b)

FIGURE 5.16 Oscilloscope displays showing the performance of the bandpass filter shown in Figure 5.15. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*


At the Upper Cutoff Frequency

V_i
V_o
1 4.00 V/div
offset: 0.000 V
10.00 : 1 dc
4 4.00 V/div
offset: 0.000 V
10.00 : 1 dc
0.00000 s
250.000 us
50.0 us/div
500.000 us
Vp-p(1) 10.0000 V
Vp-p(4) 5.81250 V
frequency(1) 8.56410kHz
1 ƒ 200.0 mV

(c)

FIGURE 5.16 *Continued*

TABLE 5.3

	Design Goal	*Measured Value*
Resonant frequency	8000 hertz	8080 hertz
Q	10	8.3
Bandwidth	800 hertz	973 hertz
Voltage gain at f_R	1.0	0.825

5.5 BAND REJECT FILTER

A band reject filter is a circuit that allows frequencies to pass that are either lower than the lower cutoff frequency or higher than the upper cutoff frequency. That is, only those frequencies that fall between the two cutoff frequencies are rejected or at least severely attenuated.

5.5.1 Operation

Figure 5.17 shows an active filter that is based on the common twin "T" configuration. The twin T gets its name from the two RC T networks on the input. For purposes of analysis, let us consider the lower ends of R_3 and C_3 to be grounded. This is a reasonable approximation, since the output impedance of an op amp is generally quite low. The T circuit consisting of C_1, C_2, and R_3 is, by itself, a high-

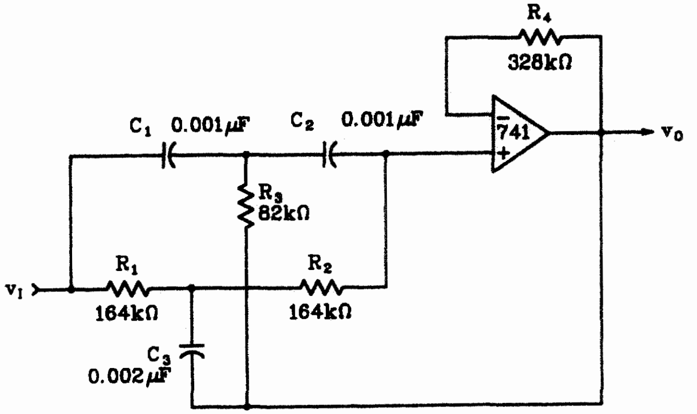


FIGURE 5.17 A band-reject filter circuit used for a numerical analysis example.

pass filter. That is, the low frequencies are prevented from reaching the input of the op amp because of the high reactance of C_1 and C_2. The high frequencies, on the other hand, find an easy path to the op amp because the reactance of C_1 and C_2 is low at higher frequencies.

The second T network is made up of R_1, R_2 and C_3 and forms a low-pass filter. Here the low frequencies find C_3's high reactance to be essentially open, so they pass on to the op amp input. High frequencies, on the other hand, are essentially shorted to ground by the low reactance of C_3. It would seem that both low and high frequencies have a way to get to the (+) input of the op amp and therefore to be passed through to the output. If, however, the cutoff frequencies of the two T networks do not overlap, there is a frequency (f_R) that results in a net voltage of 0 at the (+) terminal of the op amp.

To understand this effect, we must also consider the phase shifts given to a signal as it passes through the two networks. At the center, or resonant, frequency (f_R), the signal is shifted in the negative direction while passing through one T network. It receives the same amount of positive phase shift while passing through the other T network. These two shifted signals pass through equal impedances (R_2 and X_{C2}) to the (+) input. Thus, at any instant in time (at the center frequency), the effective voltage on the (+) input is 0. The more the input frequency deviates from the center frequency, the less the cancellation effect. Thus, as we initially expected, this circuit rejects a band of frequencies and passes those frequencies that are higher or lower than the cutoff frequencies of the filter.

The op amp offers a high impedance to the T networks, thus reducing the loading effects and therefore increasing the Q of the circuit. Additionally, by connecting the "ground" point of C_3 and R_3 to the output of the op amp, we have another increase in Q as a result of the feedback signal. At or very near the center frequency, very little signal makes it to the (+) input of the op amp. Therefore, very little signal appears at the output of the op amp. Under these conditions the output of the op amp merely provides a ground (i.e., low impedance return to ground) for the T networks. For the other frequencies, though, the feedback essentially raises the impedance offered by C_3 and R_3 at a particular frequency. Therefore, they don't attenuate the off-resonance signals as much, which has the effect of narrowing the bandwidth or, we could say, increasing the Q.

Resistor R_4 is to compensate for the voltage drops caused by the op amp bias current flowing through R_1 and R_2. It is generally equal in value to the sum of R_1 and R_2.

5.5.2 Numerical Analysis

The component values for the twin-T circuit normally have the following ratios:

1. $R_1 = R_2$
2. $R_1 = 2R_3$
3. $C_1 = C_2$
4. $C_3 = 2C_1$
5. $0 \leq R_4 \leq (R_1 + R_2)$

Under these conditions, let us compute the following circuit characteristics:

1. Center frequency
2. Input impedance

Center Frequency. The center frequency for the twin-T filter is the frequency that causes the reactance of C_3 to equal the resistance of R_3. At this same frequency, $X_{C1} = X_{C2} = R_1 = R_2$. The equation for the center frequency, then, is simply a transposed version of the basic capacitive reactance equation:

$$X_C = \frac{1}{2\pi fC}, \text{ or}$$

$$f = \frac{1}{2\pi X_C C}$$

Since, at the center frequency, $X_{C1} = R_1$, we can substitute R_1 for X_C in the preceding equation to yield our equation for the center frequency of the twin-T filter:

$$\boxed{f_O = \frac{1}{2\pi R_1 C_1} \qquad (5.23)}$$

In the case of the circuit shown in Figure 5.17, we can compute the center frequency as follows:

$$f_R = \frac{1}{6.28 \times 164\ k\Omega \times 0.001\ \mu F} = 971\ Hz$$

On either side of the center frequency, we can expect the signals to pass with a voltage gain of nearly unity.

Input Impedance. As with many filter circuits, the input impedance of the circuit shown in Figure 5.17 varies with frequency. The lowest impedance occurs at the higher frequencies and is approximately equal to R_1, R_2, and R_3 in parallel. That is,

$$Z_{IN}(\text{min}) \approx R_1 \| R_2 \| R_3 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \tag{5.24}$$

In the case of Figure 5.17, we can estimate the minimum input impedance as

$$Z_{IN}(\text{min}) = \frac{1}{\frac{1}{164\ k\Omega} + \frac{1}{164\ k\Omega} + \frac{1}{82\ k\Omega}} = 41\ k\Omega$$

5.5.3 Practical Design Techniques

Now let us design a twin-T, band reject filter to satisfy a specific design requirement. We will design a filter that will deliver the following performance:

1. Center frequency	5500 hertz
2. Minimum input impedance	10 kilohms
3. Highest input frequency	18 kilohertz

Select a Preliminary Value for R_3. The minimum value for R_3 is determined by the specification for the minimum input impedance. More specifically, the minimum value for R_3 is determined according to Equation (5.25).

$$R_3(\text{min}) = 2Z_{IN}(\text{min}) \tag{5.25}$$

In our present case, the minimum value for R_3 is determined as follows:

$$R_3(\text{min}) = 2 \times 10\ k\Omega = 20\ k\Omega$$

The upper limit for the value of R_3 is established by two factors:

1. Effects of op amp bias currents
2. Minimum practical values for C_1 to C_3

The effects of op amp bias currents can be made tolerable if we keep the value of R_3 below about 270 kilohms. Although the bias currents do not actually flow through R_3, it is the value of R_3 that will determine the values for R_1 and R_2.

The minimum practical value for the capacitors is affected by several things, including the op amp used and the required degree of stability. A workable goal, however, is to design the circuit such that all capacitor values are greater than 100 picofarads.

Let us initially choose a value of 22 kilohms for R_3. If the computed values for the capacitors are found to be too small, or there are no reasonably close standard values, then we will have to select a different value for R_3 and recompute.

Determine the Value for C_1. First we compute the ideal value for C_1; then we will select the nearest standard value. We can compute the required value of capacitance by applying Equation (5.26).

$$C_1 = \frac{1}{4\pi f_R R_3} \tag{5.26}$$

For the present design, we compute the value for C_1 as follows:

$$C_1 = \frac{1}{4 \times 3.14 \times 5.5\ kHz \times 22\ k\Omega} = 658\ pF$$

Let us choose the nearest standard value of 680 picofarads for C_1.

Compute the Exact Value for R_3. Now that a standard value for C_1 has been selected, we can determine the exact value required for R_3. It should be noted that the performance of the twin-T filter design relies heavily on accurate selection and matching of component values. Therefore, "ballpark" values are usually inappropriate. The exact value needed for R_3 can now be computed by applying a transposed version of Equation (5.26).

$$\begin{aligned} C_1 &= \frac{1}{4\pi f_R R_3}, \text{ or} \\ R_3 &= \frac{1}{4\pi f_R C_1} \\ &= \frac{1}{4 \times 3.14 \times 5.5\ kHz \times 680\ pF} \\ &= 21.3\ k\Omega \end{aligned}$$

We can obtain this value by combining fixed resistances (e.g., 27 kΩ in parallel with 100 kΩ) or by using a fixed resistance and a variable resistor in series (e.g., 18-kilohm fixed resistor in series with a 5-kilohm variable resistor). In either case, however, every effort should be made to obtain the correct value.

Compute C_2 and C_3. Capacitor C_2 is always the same value as C_1. That is,

$$C_2 = C_1 \tag{5.27}$$

For our purposes, we compute C_2 as

$$C_2 = C_1 = 680\ pF$$

Capacitor C_3 is twice the size of C_1, or simply

$$C_3 = 2C_1 \tag{5.28}$$

In our particular case

$$C_3 = 2C_1 = 2 \times 680\ pF = 1360\ pF$$

The nearest standard value is 1500 picofarads, which is close enough for many applications, but would undermine the performance of our filter. The simplest way to obtain more precise values in this case is to parallel two 680-picofarad capacitors. This will give us the value we need.

Compute R_1 and R_2. Resistors R_1 and R_2 are equal in size and are twice the value of R_3. We can express this as an equation.

$$R_1 = R_2 = 2R_3 \tag{5.29}$$

In the present design case, we compute these resistors as

$$R_1 = R_2 = 2 \times 21.3\ k\Omega = 42.6\ k\Omega$$

The nearest standard value is 43 kilohms. We might be able to get by with this, but in general we must try to obtain the exact values required. To this end, let us choose either a combination of fixed resistors (e.g., 39 kΩ in series with a 3.6 kΩ) or a fixed resistor and a variable resistor in combination (e.g., a 39-kΩ fixed resistor in series with a 5-kΩ variable resistor).

Compute R_4. Resistor R_4 helps to compensate for the voltage drop across R_1 and R_2 that is produced by the op amp bias currents. To minimize the effects of the bias currents, we set R_4 equal to the series combination of R_1 and R_2. That is,

$$R_4 = R_1 + R_2 \tag{5.30}$$

For purposes of our present design, R_4 is computed as

$$R_4 = 42.6\ k\Omega + 42.6\ k\Omega = 85.2\ k\Omega$$

For many applications, this is not a critical value. In our case, let us use the nearest standard value of 82 kilohms.

Select the Op Amp. As with previous filter designs, there are two op amp parameters that we want to focus on in order to select an appropriate op amp.

1. Bandwidth
2. Slew rate

As mentioned before, if the resistance values turn out to be quite high, then an op amp with particularly low bias current will be important. And, if the capacitance values must be below about 270 picofarads, we select an op amp with low internal capacitances.

Bandwidth. The required bandwidth of our op amp is determined by the highest frequency that must pass the circuit. The design specifications for our present case specify the highest input frequency as 18 kilohertz. The required bandwidth for the op amp is computed in the same manner as described in Chapter 2:

$$\begin{aligned} f_{UG} &= A_V f \\ &= 1 \times 18\ kHz \\ &= 18\ kHz \end{aligned}$$

This is well within the capabilities of the standard 741 op amp.

Slew Rate. The minimum slew rate for the op amp can be computed with Equation (5.7).

$$\begin{aligned} slew\ rate(\text{min}) &= \pi f_H v_O(\text{max}) \\ &= 3.14 \times 18\ kHz \times 26\ V \\ &= 1.469\ V/\mu S \end{aligned}$$

This exceeds the capability of the standard 741, which has a 0.5-volts-per-microsecond slew rate. We will use an MC1741SC for our design, as it satisfies the design's bandwidth and slew rate requirements.

This completes the design of our 5500-hertz band-reject filter, whose schematic is shown in Figure 5.18. The oscilloscope displays in Figure 5.19 indicate the performance of the circuit at resonance, at the two cutoff frequencies, and at two far removed frequencies in the passband of the filter. Table 5.4 contrasts the design goals for the filter with the actual measured performance of the final design. It should be noted that 5-percent tolerance components were used to con-

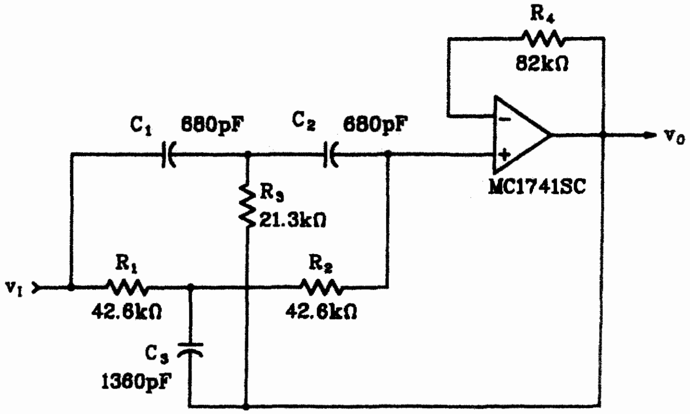
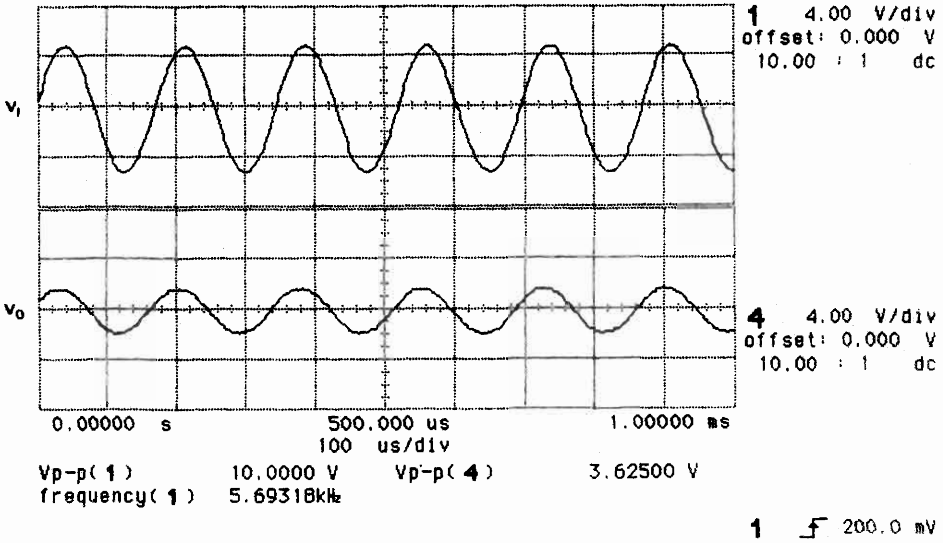

R₄
82kΩ
C₁ 680pF
C₂ 680pF
v₀
MC1741SC
R₃
21.3kΩ
v_I
R₁
42.6kΩ
R₂
42.6kΩ
C₃
1360pF

FIGURE 5.18 A twin-T band-reject filter designed for a center frequency of 5500 hertz.

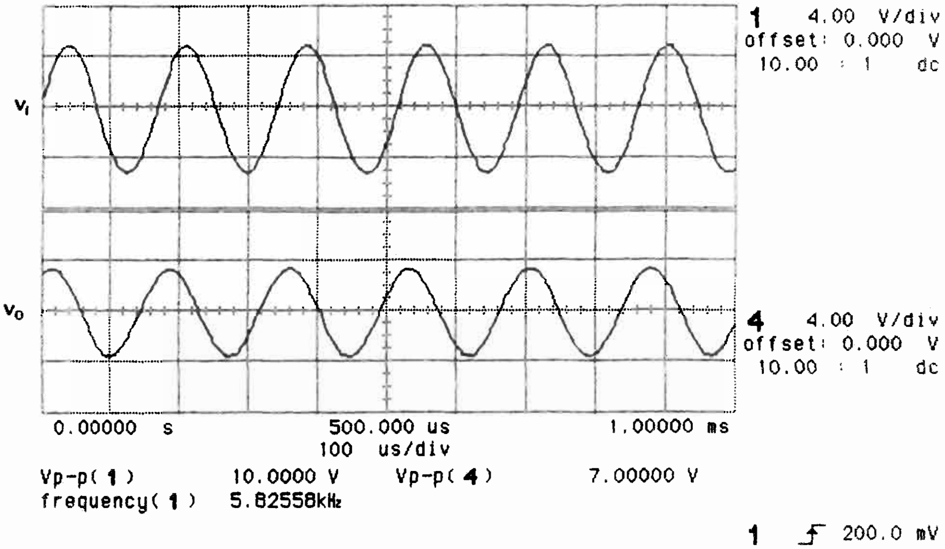
At Center Frequency



(a)

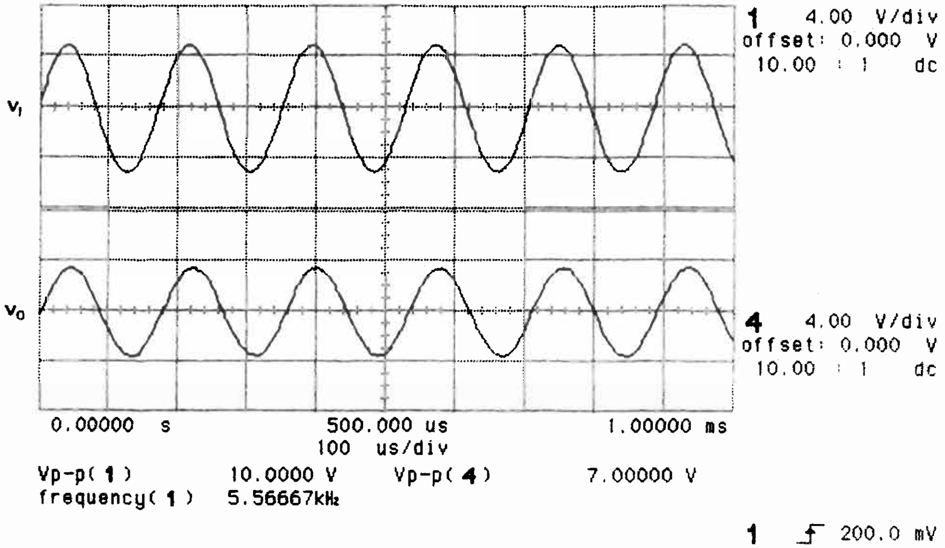
FIGURE 5.19 Oscilloscope displays showing the performance of the twin-T filter shown in Figure 5.18. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*

At the Upper Cutoff Frequency



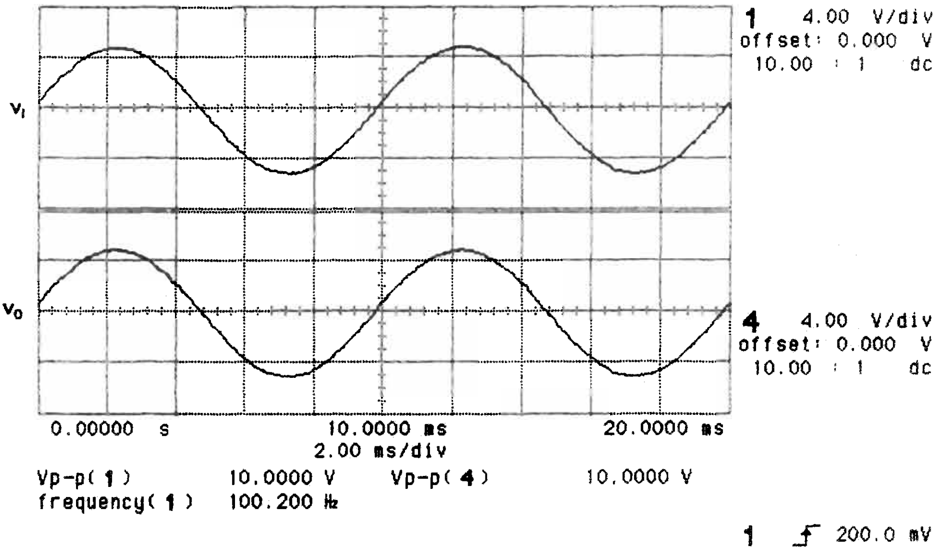
(b)

At the Lower Cutoff Frequency



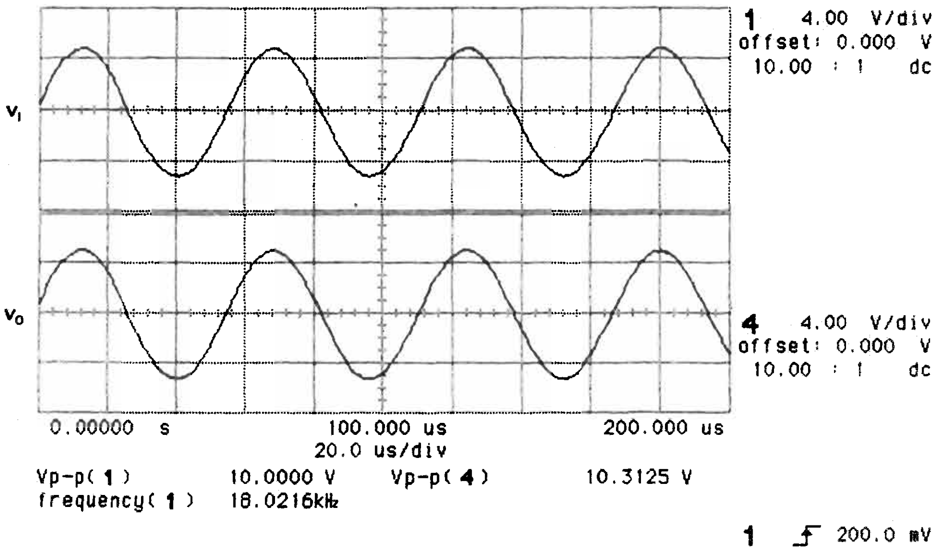
(c)

FIGURE 5.19 *Continued*


Well Below Cutoff

Vᵢ
Vₒ
1 4.00 V/div
offset: 0.000 V
10.00 : 1 dc
4 4.00 V/div
offset: 0.000 V
10.00 : 1 dc
0.00000 s
10.0000 ms
20.0000 ms
2.00 ms/div
Vp-p(1) 10.0000 V
Vp-p(4) 10.0000 V
frequency(1) 100.200 Hz
1 200.0 mV

(d)


Well Above Cutoff

Vᵢ
Vₒ
1 4.00 V/div
offset: 0.000 V
10.00 : 1 dc
4 4.00 V/div
offset: 0.000 V
10.00 : 1 dc
0.00000 s
100.000 us
200.000 us
20.0 us/div
Vp-p(1) 10.0000 V
Vp-p(4) 10.3125 V
frequency(1) 18.0216kHz
1 200.0 mV

(e)

FIGURE 5.19 *Continued*

TABLE 5.4

	Design Goal	*Measured Performance*
Resonant frequency	5500 hertz	5693 hertz
Minimum Z_{IN}	10 kilohms	10.65 kilohms
Q	Not specified	22

struct the circuit. More precise values would yield performance correspondingly closer to the design goals. The Q of the circuit can go as high as 40 or 50 with careful selection of components.

5.6 TROUBLESHOOTING TIPS FOR ACTIVE FILTERS

We can generally classify potential troubles in active filters into two broad classes:

1. DC problems
2. AC problems

Our first measurements will quickly tell us which type of problem exists. We can then focus our efforts on areas that might cause this type of problem.

DC Problems. Problems that cause the output of the op amp to be at some abnormal DC level are generally located in the same manner as described in previous chapters. Basically, you need to ensure that the proper V^+ and V^- are present **directly** on the appropriate pins of the op amp. If these voltages are correct, compare the polarity of the differential input voltage (v_d) with the polarity on the output pin. If the polarities contradict normal op amp behavior, then suspect the op amp; if they are correct for a normal op amp, then measure the DC level on the input to the op amp circuit. A prior stage may be sending an abnormal DC level into this stage, which makes it appear to be defective.

If all of these appear normal, then verify the integrity of the feedback circuit. If it is open, the output of the op amp will be at one of the two extremes.

AC Problems. If the DC voltages are correct in the filter circuit, but the filter does not correctly discriminate against certain frequencies, then suspect the frequency determining components. If the resonant, or cutoff, frequencies have simply shifted slightly, you might suspect a change in component values. On the other hand, if the AC operation of the circuit has been altered dramatically, then suspect an open component. Normal DC values with abnormal AC values often point to an open capacitor or to a resistor that is isolated from DC (e.g., R_3 in Figure 5.18).

As with all op amp troubleshooting tasks, it is essential that you understand the proper operation of the circuit and continuously contrast the actual performance with the known expected performance.

REVIEW QUESTIONS

1. Refer to Figure 5.2. What is the effect on circuit operation if capacitor C_2 becomes open?
2. If the DC level on the output of the op amp in Figure 5.2 is normal but there are no AC signals present, is capacitor C_1 open a possible cause? Explain your answer.
3. Refer to Figure 5.7. If capacitor C_2 opens, will the DC level on the output of the op amp be affected? Explain.
4. If resistor R_3 shorts in Figure 5.7, what is the effect on circuit operation?
5. A circuit that passes all frequencies below the cutoff frequency is called a ____ filter.
6. A circuit that rejects a very narrow band of frequencies is called a ____ filter.
7. Refer to Figure 5.12. The ratio of resistor R_4 and resistor R_3 establishes the gain of the amplifier. (True or False)
8. Refer to Figure 5.15. What is the effect on circuit operation if capacitor C_2 becomes open?
9. Refer to Figure 5.15. What is the effect on the DC level on the output of the op amp if resistor R_2 becomes shorted?
10. Refer to Figure 5.18. Which of the following defects can cause the circuit to respond like a high-pass filter?
    a. C_1 open
    b. R_1 open
    c. R_4 shorted
    d. C_2 open
    e. R_3 shorted

CHAPTER SIX

Power Supply Circuits

6.1 VOLTAGE REGULATION FUNDAMENTALS

Nearly all electronic systems require one or more sources of stable DC voltage. Yet many systems get their input power from the standard 120-VAC power line. Even battery-powered units may require stable DC voltages at levels other than those provided directly by the battery. Figure 6.1 shows the basic role played by a voltage regulator circuit and where it fits in the power distribution scheme.

If the system receives its power from the 120-VAC power line, the first step is usually voltage reduction via a step-down transformer. The output of the transformer (there may be more than one) is then rectified to produce pulsating DC. The rectified waveform is then filtered with large capacitors to produce a relatively smooth but *unregulated* source of DC voltage. An unregulated voltage source is one that varies with changes in load current or in applied voltage. All of the functions just described are represented by the first block in Figure 6.1.

The voltage at the output of the rectifier/filter is smooth DC, but it is not regulated. Thus, the value of voltage will change with changes in input voltage or with changes in load current. To eliminate these changes and produce a solid source of DC voltage, we route the filtered DC to a voltage regulator circuit (the second block in Figure 6.1).

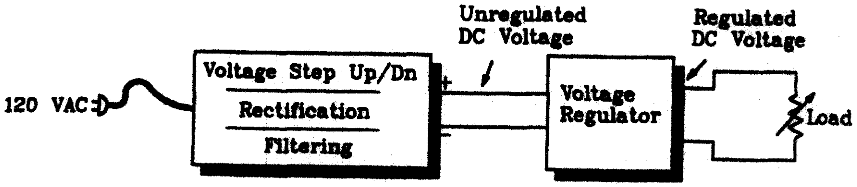


FIGURE 6.1 A voltage regulator circuit provides constant voltage to a load.

There are many types of voltage regulator circuits, but the purpose remains the same—to maintain a constant output voltage even though both the input voltage and the load current may be changing. The regulated output voltage is always less than the unregulated input voltage.

We will examine three basic classes of voltage regulator circuits:

1. Series
2. Shunt
3. Switching

6.1.1 Series Regulation

Figure 6.2 illustrates the basic concept of series voltage regulation. The voltage regulator circuit is designed to act as a variable resistance in series with the load. The regulator senses changes in load voltage (whether caused by changes in input voltage or by changes in load current) and adjusts its resistance such that the voltage across the load remains constant. This is one of the most common voltage regulation techniques. The regulator can also be designed to protect against short circuits on the regulated output. In practice, the "variable resistor" shown as the regulating element in Figure 6.2 is actually a transistor or an integrated voltage regulator circuit.

6.1.2 Shunt Regulation

The concept of a shunt-voltage regulator is illustrated in Figure 6.3. Here the regulating element (shown as a variable resistor) is connected in parallel, or shunt, with the load. The regulator circuit senses changes in load voltage and adjusts the effective resistance of the regulating element to compensate. If, for example, the load current drops, the output voltage tends to rise (i.e., less drop across R_S). The regulator circuit detects this change, however, and decreases the resistance of the shunt regulator element, causing the regulator branch to draw

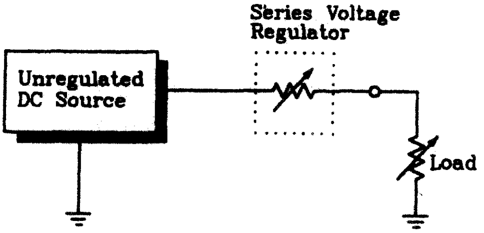


FIGURE 6.2 A series voltage regulator acts as a variable resistor in series with the load.

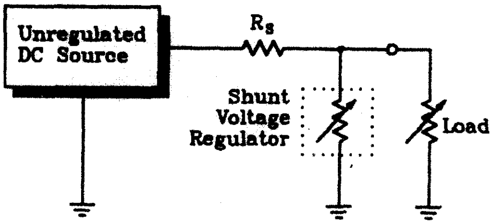


FIGURE 6.3 A shunt voltage regulator acts as a variable resistor in parallel with the load.

more current and the current through R_S to remain constant, and preventing the output voltage from rising.

The shunt regulator is generally used for low-current applications because it consumes a significant amount of power. A simple zener diode is an example of a shunt regulator. By adding an op amp, however, the degree of regulation can be improved.

6.1.3 Switching Regulation

The basic operation of a switching voltage regulator circuit is shown in Figure 6.4. Here, the regulating element (usually a transistor) is operated either *full on* (closed switch) or *full off* (open switch). The switching usually occurs at tens or hundreds of kilohertz.

While the switch is closed, the unregulated source supplies current to the load via L_1. The inductance of L_1 smooths the current changes that might be caused by the switching circuit. During this time, energy is stored in the magnetic field that builds up around the coil. When the switch opens, the magnetic field begins to collapse and the stored energy is returned to the circuit. The collapsing field now acts as a voltage source and keeps the load current flowing steadily through the alternate path of D_1.

Many switching regulator circuits adjust the duty cycle of the switching action to compensate for changing load or input voltage conditions. That is, if the on time of the switching action is lengthened (relative to the off time), the average (DC) output voltage will be higher. As with the other regulator circuits, the switching regulator must sense changes in the output voltage in order to compensate (i.e., regulate).

6.1.4 Line and Load Regulation

In order to express the regulator's ability to compensate for changes in the line voltage or the load current, we compute two percentages. The first, called *line regulation,* provides an indication of the regulator's ability to compensate for changes in the input voltage. It is a simple ratio of the change in output voltage to the change in line voltage. That is,

$$\%\ line\ regulation = \frac{V_{REG}(\text{max}) - V_{REG}(\text{min})}{V_{IN}(\text{max}) - V_{IN}(\text{min})} \times 100$$

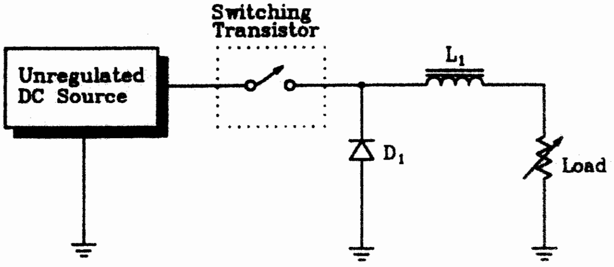


FIGURE 6.4 A switching voltage regulator offers high efficiency of operation.

The second percentage, called *load regulation*, provides an indication of the regulator's ability to compensate for changes in load current. It is computed as

$$\%\ load\ regulation = \frac{V_{REG}(no\ load) - V_{REG}(full\ load)}{V_{REG}(full\ load)} \times 100$$

6.1.5 Voltage References

All of the regulator circuits described in this chapter require a stable reference voltage. The actual load voltage is continuously compared against this reference to determine what changes are required by the regulator circuit. In essence, the voltage reference is in itself a voltage regulator circuit.

Although a zener diode is a low-cost, practical reference source, the actual zener voltage changes significantly with changes in current through the zener. Therefore, if we want a more stable source, we must go beyond the simple zener regulator. Figure 6.5 shows a circuit that combines a zener diode and an op amp to produce a simple but stable reference voltage. We will utilize this circuit in all of the regulator circuits described in this chapter.

The MC3401 op amp is somewhat different than the other op amps discussed so far in the text. It is designed for operation from a single power supply—that is, only one power source is required for normal operation. A more complete discussion of single-supply op amps is presented in Chapter 11. For now, suffice it to say that the input terminals are essentially PN junctions connected to ground. This means that the voltage on either input will remain at 0.6 volts or less. You may think of the input as responding to current changes in the same way as the emitter-base circuit of a transistor.

Since the voltage across R_1 is constant (approximately 0.6 volts), its current is constant. It is essentially equal to the zener diode current because the op amp bias current is insignificant. Since the zener current is constant, the zener voltage will be constant.

If the output voltage attempts to change, this change is felt on the (–) pin via D_1. Because the voltage on the (–) input is essentially limited by an internal junction, the changes fed back have only minimal effect on the voltage on the (–) pin, but rather cause changes in bias currents. In any case, the result is that the output of the op amp changes in a polarity that tends to compensate for the changing output

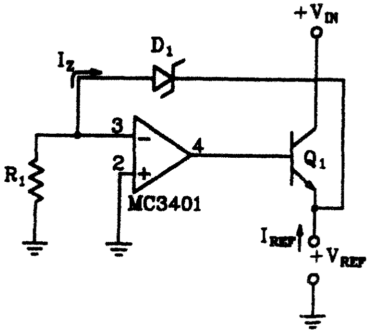


FIGURE 6.5 A simple, but stable, voltage reference can be built around a single-supply op amp and zener diode.

voltage. All of this closed-loop action occurs almost instantly, so the actual load voltage never really changes significantly. Although the circuit compensates for changes in load current and in input voltage, it may still drift as a result of changes in temperature. This latter effect can be essentially eliminated by selecting a zener diode with a temperature coefficient that is opposite (+2 $mV/°C$) from that in the op amp. For our purposes, we will ignore the effects of temperature changes.

The output or reference voltage for the circuit shown in Figure 6.5 can be approximated with Kirchhoff's Voltage Law. That is,

$$V_{REF} = V_{D_1} + 0.6 \tag{6.1}$$

Transistor Q_1 is a simple current booster (as discussed in Chapter 2). The output current of the op amp is limited to about 5 milliamperes, but required zener currents may be substantially higher than this. Assuming that the junction breakdown voltages are adequate, there are only three critical parameters for the selection of Q_1:

1. Current gain (β or h_{FE})
2. Power dissipation (P_D)
3. Collector current

The minimum required current gain for Q_1 can be determined from the basic transistor equation for current gain,

$$\beta_{MIN} = \frac{I_{REF} + I_Z}{5\ mA} \tag{6.2}$$

where 5 milliamps is the maximum recommended output current for the MC3401 op amp.

The power dissipation for Q_1 can be determined from the basic power equation.

$$P_D = (I_{REF} + I_Z)(V_{IN} - V_{REF}) \tag{6.3}$$

Resistor R_1 simply establishes the desired zener current. Ohm's Law gives us an approximate value.

$$R_1 = \frac{0.6}{I_Z} \tag{6.4}$$

Let us now design a voltage reference to be used as a stable source for the regulator circuits presented in this chapter. We use the following design goals:

1. Unregulated input voltage	+10 to 15 volts DC
2. Regulated output voltage	+4 volts
3. Percent of voltage regulation	0.1 percent
4. Maximum reference current	1 milliampere

Choose D_1. The required voltage for D_1 can be determined by applying Equation (6.1). In our case

$$\begin{aligned} V_{D_1} &= V_{REF} - 0.6 \\ &= 4\ V - 0.6\ V \\ &= 3.4\ V \end{aligned}$$

This is **not** necessarily the *value* of the zener diode. Rather, it is the required voltage across it. We will refer to a manufacturer's data sheet (Appendix 5) and select a diode that is close to the required voltage and then adjust the zener current to obtain the exact value needed. For the present case, let us choose a 1N5227 zener, which is rated for 3.6 volts when a 20-milliampere current is passed through it. We will adjust the value of R_1 to cause more or less current through the zener and therefore obtain a higher or lower voltage drop across it. Recall that the zener voltage varies nonlinearly with zener current, and that the exact zener voltage at a certain current varies between similar devices. Although the exact value for R_1 will have to be obtained experimentally, the circuit is exceptionally stable once it is constructed.

Compute R_1. We can now calculate a starting value for R_1 with Equation (6.4).

$$R_1 = \frac{0.6\ V}{I_{ZT}} = \frac{0.6\ V}{20\ mA} = 30\ \Omega$$

We will use a standard value of 27 ohms for R_1. Once the circuit has been constructed, we may have to adjust R_1 slightly to obtain the exact output voltage.

Select Q_1. Because the highest DC input voltage was listed as +15 volts, our collector-to-emitter and collector-to-base breakdown voltages should be greater than 15 volts. The minimum current gain is computed with Equation (6.2).

$$\beta_{MIN} = \frac{I_{REF} + I_Z}{I_{OP}} = \frac{1\ mA + 20\ mA}{5\ mA} = 4.2$$

This, of course, is not a challenging goal. In fact, if the actual zener current were less than 5 milliamps, we could omit Q_1 from the design.

The power dissipation for Q_1 can be estimated with Equation (6.3) as

$$\begin{aligned} P_D &= (I_{REF} + I_Z)(V_{IN} - V_{REF}) \\ &= (1\ mA + 20\ mA)(15\ V - 4\ V) \\ &= 231\ mW \end{aligned}$$

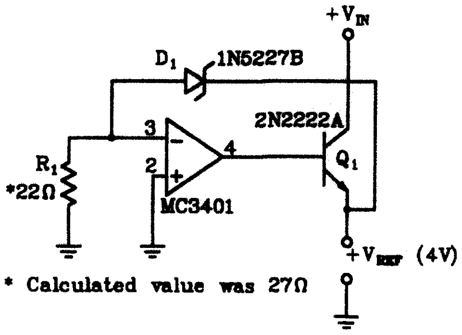
Finally, Q_1 must be able to handle the combined currents of I_Z and I_{REF} as collector current. In our particular case,

$$I_C = I_Z + I_{REF} = 20\ mA + 1\ mA = 21\ mA$$

Let us choose a common 2N2222A as the current booster for our design. The data sheet in Appendix 3 indicates that it will exceed our requirements. By following the process presented in Appendix 10, we can determine that no heat sink will be necessary, but the transistor will operate fairly hot. It might be desirable to add a small heat sink.

Figure 6.6 shows the final schematic of our 4-volt reference circuit. The input and output voltage levels are shown on the oscilloscope displays in Figure 6.7 for minimum and maximum input voltage conditions. Finally, Table 6.1 contrasts the actual circuit performance with the original design goals.

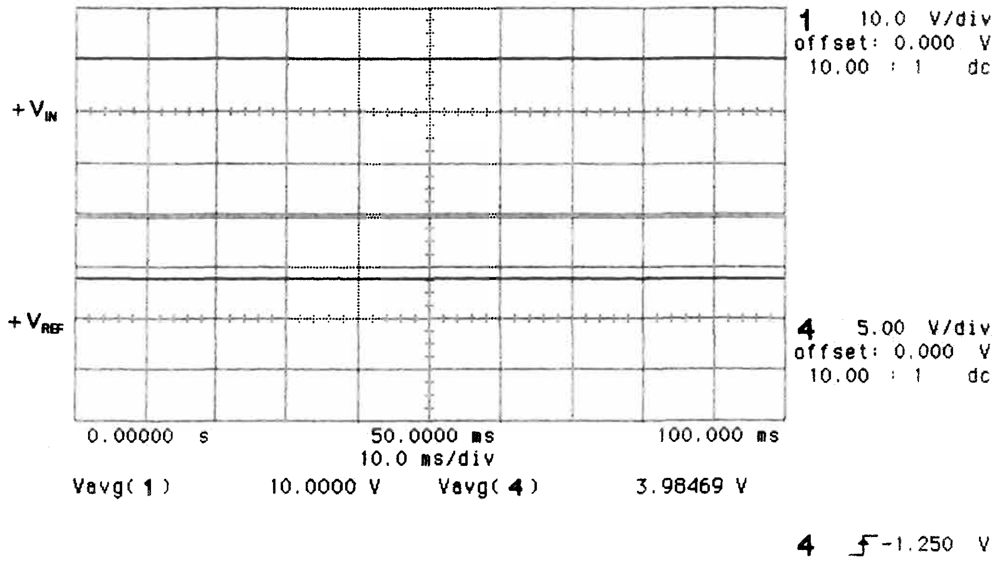
As Table 6.1 and the oscilloscope displays in Figure 6.7 indicate, the actual circuit performance exceeds our design requirements. Be sure to note in Figure 6.6 that the actual value of R_1 was adjusted to 22 ohms to trim the output voltage to the required value.



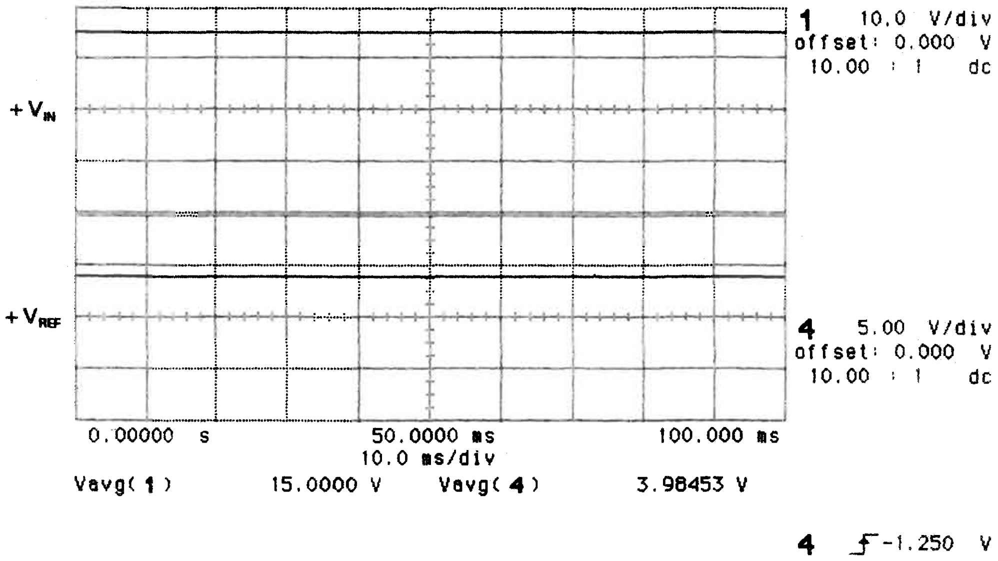
* Calculated value was 27Ω

FIGURE 6.6 A simple, stable voltage reference, which is used throughout Chapter 6.

Low Input Voltage



High Input Voltage



(b)

FIGURE 6.7 Oscilloscope displays showing the stability of the voltage reference shown in Figure 6.6. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 6.1

	Design Goal	*Measured Value*
Input voltage (DC)	+10–15 volts	+10–15 volts
Output voltage (V_{REF})	+4 volts	+3.985 volts
Percent regulation	0.1 percent	0.004 percent
Reference current	0–1 milliamperes	0–1 milliamperes

6.2 SERIES VOLTAGE REGULATORS

6.2.1 Operation

Figure 6.8 shows the schematic diagram of a basic series regulator circuit. The input to the circuit is filtered but unregulated DC voltage; the output, of course, is regulated DC voltage that remains constant in spite of changes in the load current or changes in the input voltage.

Transistor Q_1 in Figure 6.8 is known as the series *pass* transistor. Kirchhoff's Voltage Law tells us that the voltage across the load plus the voltage across the series-pass transistor must always be equal to the applied voltage. Thus, if we can control the amount of voltage dropped across the pass transistor, we have inherent control over the load voltage.

The output voltage of the regulator circuit is sampled with the voltage divider made up of resistors R_1, R_2, and potentiometer P_1. The portion of the output that appears on the wiper arm of P_1 is called the *feedback voltage.* Potentiometer P_1 is used to adjust the amount of feedback voltage and thus is used to adjust the output voltage level.

The voltage reference circuit indicated in Figure 6.8 was discussed in an earlier section. Its purpose is to provide a constant voltage level that can be used as a

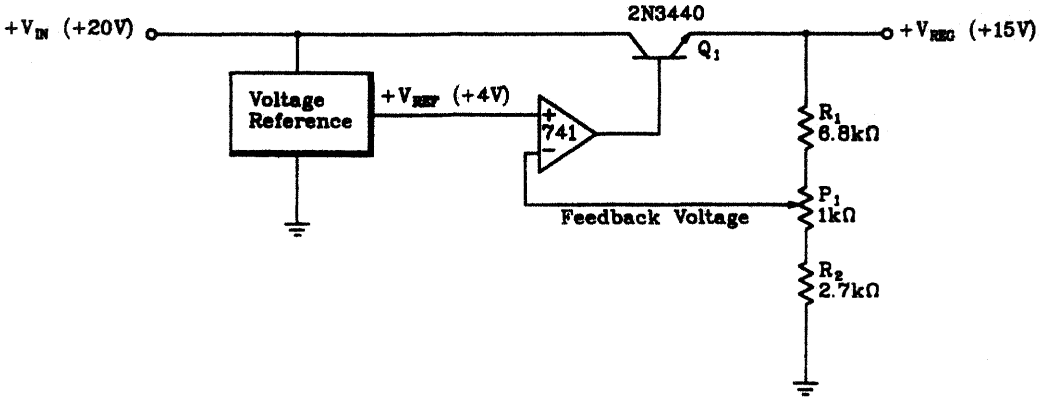


FIGURE 6.8 A series voltage regulator with an adjustable output.

stable reference. The schematic of a representative voltage reference circuit was presented in Figure 6.5.

The op amp in Figure 6.8 is called the *error amplifier.* It continuously compares the magnitude of the reference voltage with the level of the feedback signal (which represents the output voltage). Any difference between these two voltages (both magnitude and polarity) is amplified and applied to the base of the pass transistor. The polarity is such that the output voltage is returned to its correct value. As an example, let us assume that the load current suddenly decreases, which tends to make the output voltage rise. However, as soon as the output voltage starts to increase (i.e., become more positive), the feedback voltage on the wiper arm of P_1 also becomes more positive. This increasing positive on the inverting pin of the op amp causes the output of the op amp to become less positive (i.e., moves in the negative direction). Recall that the reference voltage remains constant, so any changes in the feedback voltage are immediately reflected in the output of the op amp. This reduced positive voltage on the base of Q_1 reduces the amount of forward bias and therefore increases the effective resistance of the pass transistor, causing an increased voltage drop across it. Because we are now dropping more voltage across the pass transistor, we will have less dropped across the load (Kirchhoff's Voltage Law). Thus, the initial tendency for the load voltage to rise has been offset by an increased voltage drop across the pass transistor. This process happens nearly instantaneously so that the load voltage never really sees a significant increase. Of course, the better the degree of regulation, the smaller the changes in load voltage.

To further clarify the operation of the error amplifier, let us examine the circuit from a different viewpoint. First, consider the wiper arm to be at some fixed point. We can now view the resistor network as a simple, two-resistor voltage divider. A redrawn circuit for the error amplifier is shown in Figure 6.9. Here R_1' is equivalent to R_1 and that portion of P_1 above the wiper arm. Similarly, R_2' is equivalent to R_2 and that portion of P_1 below the wiper arm. It is readily apparent that the resulting circuit is a simple noninverting amplifier circuit with a current boost transistor. This circuit was discussed in detail in Chapter 2.

Potentiometer P_1 in Figure 6.8 is used to adjust the output voltage to a particular level. If we move the wiper arm up, we increase the feedback voltage (i.e., more positive), decrease the bias on Q_1, increase the voltage drop across Q_1, and ultimately bring the output voltage down to a new, lower level. Similarly, if we

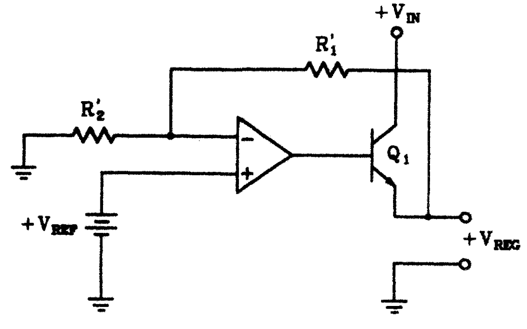


FIGURE 6.9 A simplified circuit of the error amplifier portion of Figure 6.8. It is actually a simple noninverting voltage amplifier with a current boost transistor.

move the wiper arm down, we reduce the amount of feedback voltage (i.e., less positive), increase the bias on Q_1, decrease the voltage drop across Q_1, and cause the load voltage to increase to a higher regulated level.

It is important to note that the series-regulator circuit shown in Figure 6.8 is not immune to short circuits. That is, if the output of the regulator was accidentally shorted to ground, the pass transistor would undoubtedly be destroyed by the resulting high-current flow. Many, if not most, regulated supplies are designed to be current limited. Section 6.5 discusses this option in greater detail.

6.2.2 Numerical Analysis

Let us now analyze the series-voltage regulator circuit presented in Figure 6.8. The output voltage of the regulator can be computed with Equation (6.5).

$$\boxed{+V_{REG} = +V_{REF}\left(\frac{R_1'}{R_2'} + 1\right) \qquad (6.5)}$$

where R_1' and R_2' are the equivalent values shown in Figure 6.9 and as discussed. If we assume that the wiper arm of P_1 is moved to the uppermost extreme, we can apply Equation (6.5) to compute the minimum output voltage as shown:

$$\begin{aligned}+V_{REG} &= 4\ V\left(\frac{6.8\ k\Omega}{3.7\ k\Omega} + 1\right)\\ &= 4\ V \times 2.84\\ &= 11.36\ V\end{aligned}$$

Similarly, we can move the wiper arm to the lowest position and compute the highest output voltage with Equation (6.5) as follows:

$$\begin{aligned}+V_{REG} &= 4\ V\left(\frac{7.8\ k\Omega}{2.7\ k\Omega} + 1\right)\\ &= 4\ V \times 3.89\\ &= 15.56\ V\end{aligned}$$

So the range of regulated output voltages that can be obtained by adjusting P_1 is 11.36 through 15.56 volts.

The maximum allowable output current is determined by one of the following:

1. Maximum collector current rating of Q_1
2. Maximum power dissipation rating of Q_1
3. Current limitation of $+V_{IN}$

Whichever of these limitations is reached first will determine the maximum allowable current that can be drawn from the regulator output.

The manufacturer's data sheet for a 2N3440 lists the maximum collector current as 1.0 amp. The data sheet also lists the maximum power dissipation as 1.0 watt (at 25°C), gives a thermal resistance from junction to case as 17.5°C per watt, and lists the thermal resistance from junction to air as 175°C per watt. No current limit is shown in Figure 6.8 for $+V_{IN}$. The current limit imposed by the power rating can be computed as follows:

$$I_O(\max) = \frac{P_D}{+V_{IN}(\max) - V_{REG}(\min)} \tag{6.6}$$

where P_D is the maximum power as determined with Equation (A10.3) in Appendix 10. In the case of the circuit shown in Figure 6.8, the current limit imposed by the power rating of the transistor (for $T_A = 40°\text{C}$) is computed as

$$P_D = \frac{T_j(\max) - T_A}{\theta_{JA}} = \frac{200°\text{C} - 40°\text{C}}{175°\text{C}/W} = 0.91\ W,\ \textit{therefore}$$

$$I_O(\max) = \frac{.91\ W}{20\ V - 11.36\ V} = 105\ mA$$

Since this current is lower than the 1.0-amp maximum collector current rating, it will be the limiting factor. Thus, the regulator circuit shown in Figure 6.8 has a maximum output current of about 105 milliamperes.

6.2.3 Practical Design Techniques

Let us now design a series-voltage regulator similar to the one shown in Figure 6.8. We will use the following as design goals:

1. Input voltage	+12 to +18 volts
2. Output voltage	+6 to 9 volts
3. Output current	0 to 0.5 amps
4. Line regulation	<1 percent
5. Load regulation	<1 percent
6. Error amplifier	741

Select the Pass Transistor. The characteristics of the pass transistor are determined by the input voltage, the output voltage and current requirement, and the output drive capability of the op amp. First, the collector current rating of the transistor must be greater than the value of load current. In our case, this means that our transistor must have a maximum DC current rating of greater than 500 milliamperes.

The transistor power dissipation can be found by applying Equation (6.6).

$$\begin{aligned} I_O(\text{max}) &= \frac{P_D}{+V_{IN}(\text{max}) - V_{REG}(\text{min})}, \textit{ or} \\ P_D &= I_O(\text{max})(+V_{IN}(\text{max}) - V_{REG}(\text{min})) \\ &= 0.5\ A(18\ V - 6\ V) \\ &= 6\ W \end{aligned}$$

The minimum current gain (h_{FE} or β) for the transistor can be found by applying our basic transistor formula for current gain:

$$\beta = \frac{I_C}{I_B}$$

With a circuit like that shown in Figure 6.8, base current is provided by the output of the op amp. We will establish the maximum current to be provided by the op amp as one-fourth of the short-circuit output current rating of the op amp, which, in the case of a 741, is listed in the data sheet as 20 milliamperes. Therefore, we shall limit the output current (and therefore the base current of Q_1) to one-fourth of 20 milliamperes, or 5 milliamperes. The minimum current gain for Q_1 can now be determined as shown:

$$\begin{aligned} \beta(\text{min}) &= \frac{I_C}{I_B} \\ &= \frac{0.5\ A}{5\ mA} \\ &= 100 \end{aligned}$$

The minimum collector-to-emitter voltage breakdown rating for Q_1 is found by determining the maximum voltage across Q_1. That is,

$$\boxed{V_{CEO} = V_{IN}(\text{max}) - V_{REG}(\text{min}) \qquad (6.7)}$$

In our particular case, the collector-to-emitter voltage rating is computed as

$$V_{CEO} = 18\ V - 6\ V = 12\ V$$

There are many transistors that will satisfy the requirements for Q_1. Let us select an MJE1103 (refer to Appendix 2) for this application. The calculations presented in Appendix 10 indicate that the transistor will require a heat sink for safe operation.

Determine the Required Op Amp Voltage Gain. The equivalent circuit shown in Figure 6.9 is useful for determining the required voltage gain of our op amp. We must consider the circuit under both minimum and maximum output voltage conditions. The minimum and maximum voltage gains are determined from the basic amplifier gain formula ($A_V = V_O/V_I$). That is,

$$A_V(\text{min}) = \frac{+V_{REG}(\text{min})}{+V_{REF}} \tag{6.8}$$

Similarly,

$$A_V(\text{max}) = \frac{+V_{REG}(\text{max})}{+V_{REF}} \tag{6.9}$$

In our present application, the required voltage gains for the op amp are determined as follows:

$$A_V(\text{min}) = \frac{6\ V}{4\ V} = 1.5, \textit{ and}$$

$$A_V(\text{max}) = \frac{9\ V}{4\ V} = 2.25$$

Select the Value for P_1. Selection of P_1 is largely arbitrary, but some guidelines may be established. Its minimum value should be at least 20 times the minimum equivalent load resistance. That is,

$$P_1(\text{min}) = 20\left(\frac{V_{REG}(\text{min})}{I_O(\text{max})}\right) \tag{6.10}$$

In our particular case, the minimum recommended value for P_1 is

$$P_1(\text{min}) = 20\left(\frac{6\ V}{0.5\ A}\right) = 240\ \Omega$$

The maximum value is also somewhat arbitrary, but there is generally no reason for going beyond a few tens of thousands of ohms. Let us decide to use a 5-kilohm potentiometer for P_1 in this particular application.

Compute R_1 and R_2. The values for R_1 and R_2 can be determined by applying the basic equation for voltage gain in a noninverting amplifier (refer to Figure 6.9).

Recall that minimum voltage gain occurs when the wiper arm of P_1 is at its upper extreme. Under these conditions, the equation for R_1 can be determined as follows:

$$A_V(\text{min}) = \frac{R_1}{R_2 + P_1} + 1, \textit{ or}$$

$$R_1 = [A_V(\text{min}) - 1](R_2 + P_1) \qquad (6.11)$$

Similarly, an equation for R_2 can be derived from the basic gain equation as shown:

$$A_V(\text{max}) = \frac{R_1 + P_1}{R_2} + 1, \textit{ or}$$

$$R_2 = \frac{R_1 + P_1}{A_V(\text{max}) - 1}$$

Substituting Equation (6.11) for R_1 in this equation and performing some algebraic transposing gives us our final equation for the value of R_2.

$$R_2 = \frac{P_1 A_V(\text{min})}{A_V(\text{max}) - A_V(\text{min})} \qquad (6.12)$$

We can now compute the required values for R_1 and R_2. First, we apply Equation (6.12) to find R_2.

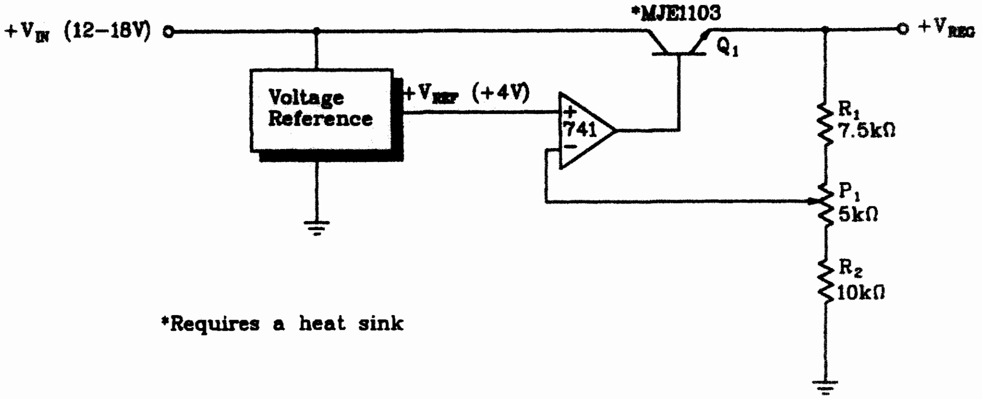
$$R_2 = \frac{5\ k\Omega \times 1.5}{2.25 - 1.5}$$
$$= 10\ k\Omega$$

We are now in a position to apply Equation (6.11) to find the value of R_1.

$$R_1 = (1.5 - 1)(10\ k\Omega + 5\ k\Omega)$$
$$= 7.5\ k\Omega$$

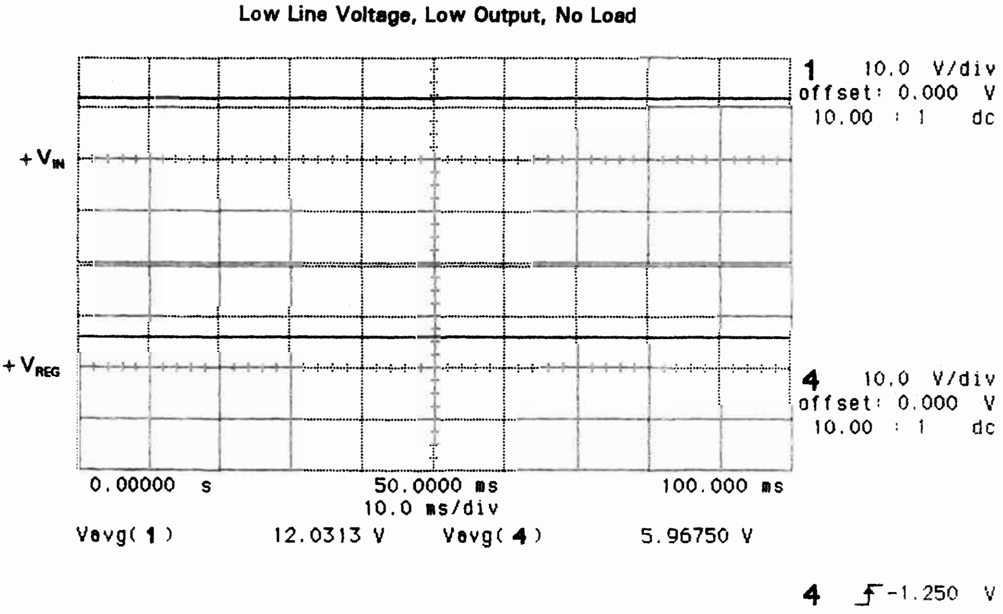
Because the computed values for R_1 and R_2 are both standard, we do not have to make any decisions regarding standard values. For most applications, we simply choose the nearest standard value.

This completes the design of our series regulator circuit. The final schematic is shown in Figure 6.10, and the performance of the circuit is indicated by the oscilloscope displays in Figure 6.11. The waveforms show the effects of minimum and maximum load current and minimum and maximum line voltage. Figure 6.11(a) shows the output under no-load conditions, and Figure 6.11(b) illustrates the effect of adding a 500-milliampere load. In both cases, the output voltage was adjusted to minimum (+6 volts). Figure 6.11(c) shows the results of maximum input voltage under no-load conditions; finally, Figure 6.11(d) illustrates the circuit performance under conditions of maximum input voltage and a 500-milliampere load. The measured performance of the circuit is summarized and contrasted with the original design goals in Table 6.2.



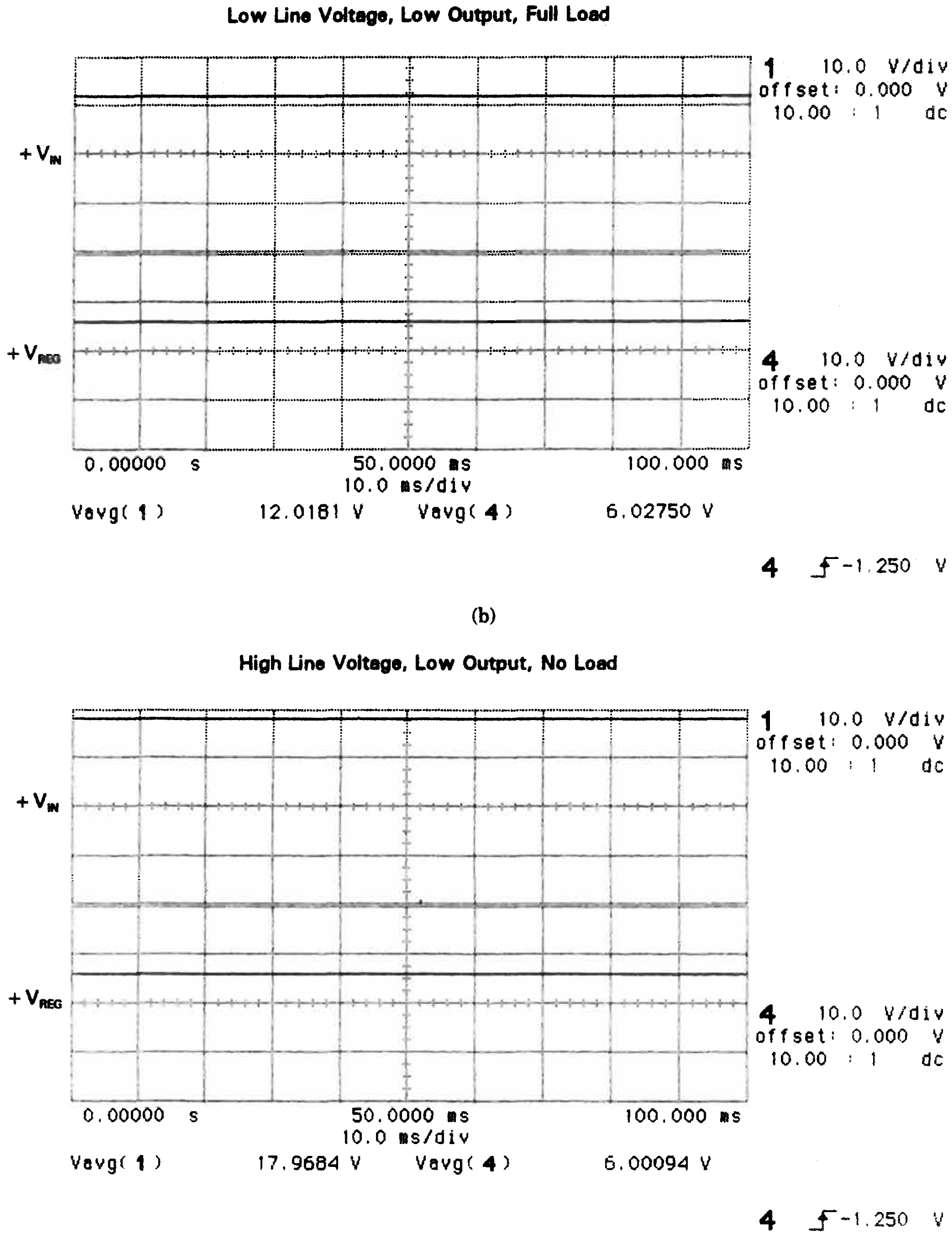
*Requires a heat sink

FIGURE 6.10 A series voltage regulator circuit designed to deliver 6 to 9 volts at 0 to 500 milliamperes.


Low Line Voltage, Low Output, No Load

(a)

FIGURE 6.11 Oscilloscope displays showing the performance of the series voltage regulator shown in Figure 6.10. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*



(b)

(c)

FIGURE 6.11 *Continued*

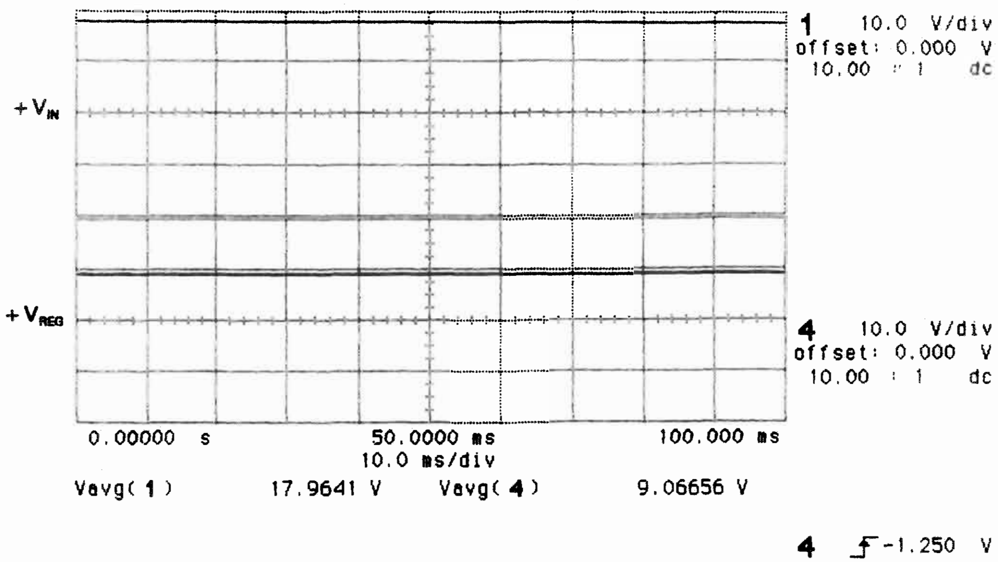

High Line Voltage, High Output, Full Load

FIGURE 6.11 *Continued*

TABLE 6.2

	Design Goal	*Measured Value*
Input voltage	+12 to +18 volts	+12 to +18 volts
Output voltage	+6 to +9 volts	+5.97 to +9.07 volts
Output current	0 to 500 milliamperes	0 to 500 milliamperes
Load regulation	<1 percent	0.99 percent
Line regulation	<1 percent	0.56 percent

6.3 SHUNT VOLTAGE REGULATION

6.3.1 Operation

Figure 6.12 shows the schematic of a basic shunt-voltage regulator circuit. To understand its operation, let us assume that the output voltage starts to increase (perhaps as a result of a decreased load current). When the load voltage starts to rise, the voltage across R_2 also increases. This is the feedback voltage for the regulator circuit and is essentially a sample of the output voltage. When the voltage across R_2 increases (i.e., becomes more positive), the output of the op amp becomes less positive because the voltage across R_2 is applied to the inverting input. This falling voltage on the output of the op amp is the base voltage for Q_1. Q_1 is connected as an emitter follower, so the emitter voltage, and therefore the

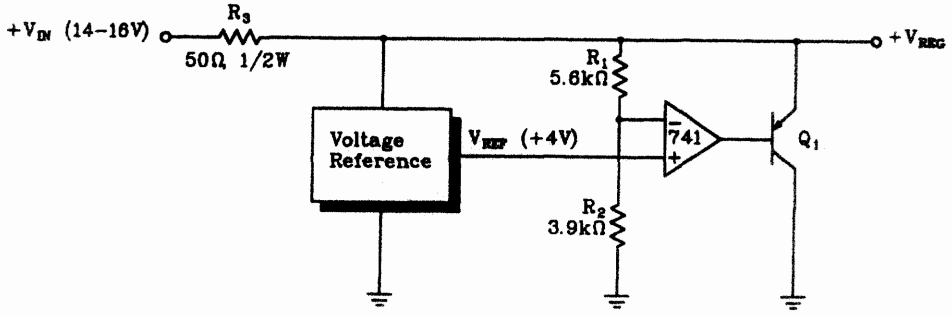


FIGURE 6.12 A shunt voltage regulator circuit.

regulated output voltage, will decrease. Actually, the decrease merely offsets the original increase, so the output remains essentially constant. If one tried to decrease the output voltage, a similar closed-loop action would compensate for the change and maintain a constant output voltage.

Another way to view the regulator action is to consider that the current in Q_1 will increase in response to an increase in the regulated output voltage. This increased transistor current causes an increased voltage drop across R_3, thus returning the output voltage to its initial level. Because the current through Q_1 increases and decreases to compensate for load voltage changes, the highest transistor current will occur during times when the load current is minimum.

The circuit would still work if the voltage reference circuit were powered directly from the unregulated input voltage. However, as we have a convenient source of regulated voltage, we can increase the overall performance of the circuit by allowing the reference circuit to use the regulated output as its input voltage.

Resistor R_3 ultimately determines the maximum current that can be drawn from the regulator. If too much current is drawn, then Q_1 is cut off and current is limited by R_3. Under these conditions, the output voltage is not regulated and will decrease with increasing load currents. The circuit does have a distinct advantage in that it is inherently current limited. That is, if a short-circuit to ground occurs on the regulated voltage line, the current is limited by resistor R_3. No other regulator components will experience an overload condition. If this resistor has an adequate power rating, no damage will result from shorted outputs.

We can change the level of the regulated output voltage by altering the values of R_1 and/or R_2. In fact, we can include a potentiometer in the feedback circuit and make an adjustable shunt-regulator circuit.

6.3.2 Numerical Analysis

Let us now extend our understanding of the shunt regulator circuit shown in Figure 6.12 to a numerical analysis of the important characteristics. Two of the most important characteristics of the regulator circuit are

1. Output voltage
2. Current capability

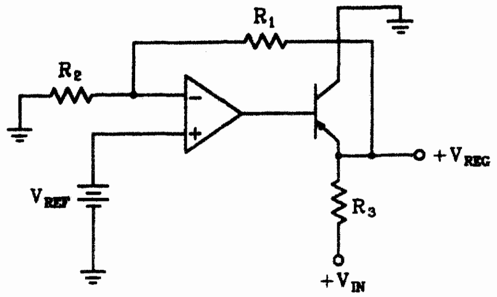


FIGURE 6.13 The error amplifier portion of the regulator circuit shown in Figure 6.12 is essentially a simple noninverting voltage amplifier.

We can redraw the circuit somewhat to more clearly see how the op amp is connected. Figure 6.13 clearly shows that the op amp is essentially connected as a simple noninverting amplifier with a current-boost transistor. The voltage gain of this circuit is simply

$$A_V = \frac{R_1}{R_2} + 1$$

The output voltage of the circuit, then, is computed by applying the basic gain equation.

$$+V_{REG} = +V_{REF} \times A_V = +V_{REF}\left(\frac{R_1}{R_2} + 1\right) \qquad (6.13)$$

In the case of the circuit shown in Figure 6.12, we can compute the regulated output voltage as

$$+V_{REG} = +4\ V \times \left(\frac{5.6\ k\Omega}{3.9\ k\Omega} + 1\right) = 9.7\ V$$

We estimate the current capability of the circuit by considering the case when $+V_{IN}$ is at its lowest level. Under these conditions, the maximum load current can be estimated with Ohm's Law.

$$I_O(\text{max}) = \frac{V_{IN}(\text{min}) - V_{REG}}{R_3} \qquad (6.14)$$

For the present case, we compute the highest allowable load current as

$$I_O(\text{max}) = \frac{14\ V - 9.7\ V}{50\ \Omega} = 86\ mA$$

Although there can be a higher load current under higher input voltage conditions, the computed value of 86 milliamperes is the highest load current that we can supply under all input voltage conditions and still expect the circuit to remain in a regulated condition. Ohm's Law can be used to determine the minimum-value load resistor that can be used with the circuit. That is,

$$R = \frac{V}{I} = \frac{9.7\ V}{86\ mA} = 112.8\ \Omega$$

Transistor Q_1 must be able to safely conduct the difference between the highest possible input current and the minimum possible load current. For many applications, we assume that the load *can* be disconnected and we therefore consider the minimum load current to be 0. If the regulator were an integral part of a system that made it impossible for the load to be disconnected (e.g., all part of the same printed circuit board), then the minimum load current could be greater than 0. For purposes of this analysis, we assume a worst-case situation, which means that Q_1 must be able to handle a value of current given by Equation (6.15).

$$I_O(\max) = \frac{V_{IN}(\max) - V_{REG}}{R_3} \tag{6.15}$$

For the circuit shown in Figure 6.12, the maximum transistor current can be calculated as

$$I_{Q_1}(\max) = \frac{16\ V - 9.7\ V}{50\ \Omega} = 126\ mA$$

We can estimate the worst-case power dissipation in Q_1 by applying our basic power formula.

$$P_D(\max) = I_{Q_1}(\max) \times V_{REG} \tag{6.16}$$

For our present circuit, the transistor dissipation is estimated as

$$P_D(\max) = 126\ mA \times 9.7\ V = 1.22\ W$$

For many applications, the heat dissipated in the transistor will require a heat sink to keep the transistor within its safe operating range.

The shunt-regulator circuit is inherently current limited. That is, if we try to draw more current than it is designed to deliver, the output voltage will drop. Even if we short the output directly to ground, the current will be limited by resistor R_3. If resistor R_3 has a sufficiently high power rating, then the duration of the short can be any length. If it has a lower power rating, then the regulator is still short-circuit proof, but the duration of the overload must be less. If the output of the circuit in Figure 6.12 is shorted directly to ground, then the maximum current flow can be computed with Ohm's Law as

$$\begin{aligned} I_{R_3} &= \frac{V_{R_3}}{R_3} \\ &= \frac{16\ V}{50\ \Omega} \\ &= 320\ mA \end{aligned}$$

The resulting power dissipation in R_3 is computed with the basic power formula as

$$\begin{aligned} P_{R_3} &= \frac{V_3^2}{R_3} \\ &= \frac{(16\ V)^2}{50\ \Omega} \\ &= 5.12\ W \end{aligned}$$

Since this clearly exceeds the 0.5-watt rating of the resistor as listed in Figure 6.12, we can expect the resistor to overheat and burn open. However, it can withstand momentary short circuits without having a higher power rating. A common way for momentary short circuits to occur is for your probe to slip off of a test point while troubleshooting a circuit.

6.3.3 Practical Design Techniques

Let us now design a shunt regulator circuit similar to the one shown in Figure 6.12. We will design it to meet the following design specifications:

1. Unregulated input voltage	+18 to +22 volts DC
2. Regulated output voltage	+12 to +15 volts DC
3. Load current	0 to 150 milliamps
4. Line regulation	<2 percent
5. Load regulation	<2 percent
6. Op amp	741

Determine the Error Amp Voltage Gain. Since the design calls for a variable output voltage, we will need to compute a range of error amp gains. As with the previous design, we will use the +4-volt reference circuit designed earlier in the chapter. The required voltage gains can be computed with Equations (6.8) and (6.9).

$$A_V(\text{min}) = \frac{+V_{REG}(\text{min})}{+V_{REF}} = \frac{12\ V}{4\ V} = 3,\ and$$

$$A_V(\text{max}) = \frac{+V_{REG}(\text{max})}{+V_{REF}} = \frac{15\ V}{4\ V} = 3.75$$

Let us plan to use a potentiometer between R_1 and R_2 of Figure 6.12 to adjust the gain of the error amp. This is similar to the method used with the series voltage regulator discussed in a prior section.

Select the Potentiometer. Selection of P_1 is not critical, and the guidelines discussed for the series regulator may be followed. That is, the minimum value for P_1 should be at least 20 times the minimum equivalent load resistance. This is computed with Equation (6.10).

$$P_1(\text{min}) = 20\left(\frac{V_{REG}(\text{min})}{I_O(\text{max})}\right) = 20\left(\frac{12\ V}{.15\ A}\right) = 1.6\ k\Omega$$

The maximum value is generally no more than a few tens of thousands of ohms. We will use a 10-kilohm potentiometer for P_1 in this particular application.

Compute R_2. Equation (6.12) provides the tool necessary to compute the value for R_2. We calculate it as follows:

$$\begin{aligned} R_2 &= \frac{P_1 A_V(\text{min})}{A_V(\text{max}) - A_V(\text{min})} \\ &= \frac{10\ k\Omega \times 3}{3.75 - 3} \\ &= 40\ k\Omega \end{aligned}$$

For this application, we select the nearest standard value of 39 kilohms for R_2.

Compute R_1. Resistor R_1 can be calculated with Equation (6.11). For our present application, R_1 is computed as shown:

$$\begin{aligned} R_1 &= (A_V(\text{min}) - 1)(R_2 + P_1) \\ &= (3 - 1)(39\ k\Omega + 10\ k\Omega) \\ &= 98\ k\Omega \end{aligned}$$

Again, we use the nearest standard value of 100 kilohms because the application is not critical.

Determine the Value of R_3. Resistor R_3 establishes the maximum possible load current from the shunt-regulator circuit. We can determine its value for a given application by applying Ohm's Law at a time when the load current and output voltage are at maximum and the input voltage is at minimum. That is,

$$\boxed{R_3 = \frac{V_{IN}(\text{min}) - V_{REG}(\text{max})}{I_O(\text{max})} \qquad (6.17)}$$

In our particular case, the required value for R_3 is found as follows:

$$R_3 = \frac{18\ V - 15\ V}{150\ mA} = 20\ \Omega$$

The power rating for R_3 is determined by using the basic power formula under worst-case conditions:

$$P_{R_3} = \frac{V_3^2}{R_3} = \frac{(V_{IN}(\text{max}) - V_{REG}(\text{min}))^2}{R_3}$$

$$= \frac{(22\ V - 12\ V)^2}{20\ \Omega} = 5\ W$$

Select Transistor Q_1. There are several transistor characteristics that must be considered when selecting a particular device for Q_1:

1. Maximum collector current
2. Current gain (h_{FE} or β)
3. Breakdown voltages
4. Power dissipation

The maximum collector current that the transistor will be expected to carry can be computed with Equation (6.15).

$$I_{Q_1}(\text{max}) = \frac{V_{IN}(\text{max}) - V_{REG}(\text{min})}{R_3}$$

$$= \frac{22\ V - 12\ V}{20\ \Omega}$$

$$= 500\ mA$$

We estimate the highest current that should be supplied by the op amp as 25 percent of the short-circuit output current of the op amp. The short-circuit output current for a 741 is listed in the manufacturer's data sheet as 20 milliamperes, so we will restrict the output current of the op amp to 25 percent of 20 milliamperes, or 5 milliamperes. We can now apply the basic current gain equation for transistors to determine the required transistor current gain.

$$\beta = \frac{I_C}{I_B} = \frac{500\ mA}{5\ mA} = 100$$

This is a fairly high-current gain for a power transistor and may necessitate the use of a Darlington pair for Q_1.

The power dissipation in Q_1 can be found by applying Equation (6.16) under conditions of maximum output voltage.

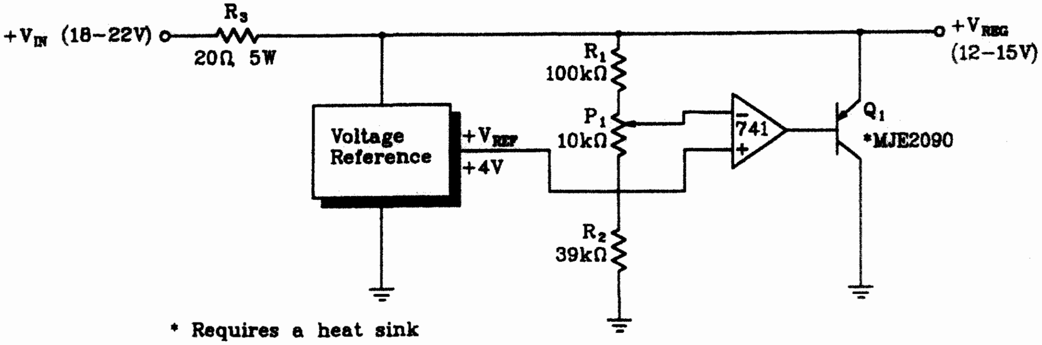
$$
\begin{aligned}
P_D(\max) &= I_{Q_1}(\max) \times V_{REG}(\max) \\
&= 500\ mA \times 15\ V \\
&= 7.5\ W
\end{aligned}
$$

This high-power dissipation is one major disadvantage of shunt-regulator circuits.

The collector-to-emitter breakdown voltage must be higher than V_{REG}(max). In the present case, the transistor breakdown rating for V_{CEO} must be greater than 15 volts.

Many transistors will satisfy the requirements of our design. For purposes of illustration, let us select an MJE2090, which, as the manufacturer's data sheet (Appendix 2) indicates, is a Darlington power transistor that satisfies all of our requirements. The calculations presented in Appendix 10 dictate the use of a heat sink for the transistor.

The complete schematic of our shunt regulator circuit is shown in Figure 6.14. Its performance is demonstrated by the oscilloscope displays in Figure 6.15. Figures 6.15(a) and 6.15(b) show the effect of adjusting P_1 between its limits. Figures 6.15(c) and 6.15(d) illustrate the circuit's response to a change in load current from 0, in Figure 6.15(c), to 150 milliamperes, Figure 6.15(d). Finally, the original design goals are contrasted with the actual measured performance in Table 6.3.

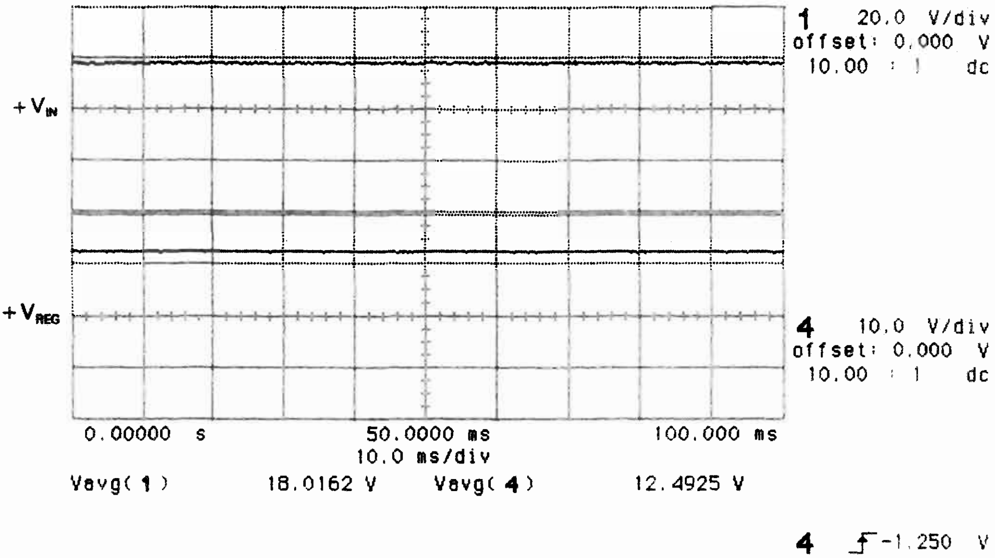


* Requires a heat sink

FIGURE 6.14 A shunt regulator circuit designed to provide a variable output voltage and to supply a load current of 0 to 150 milliamperes

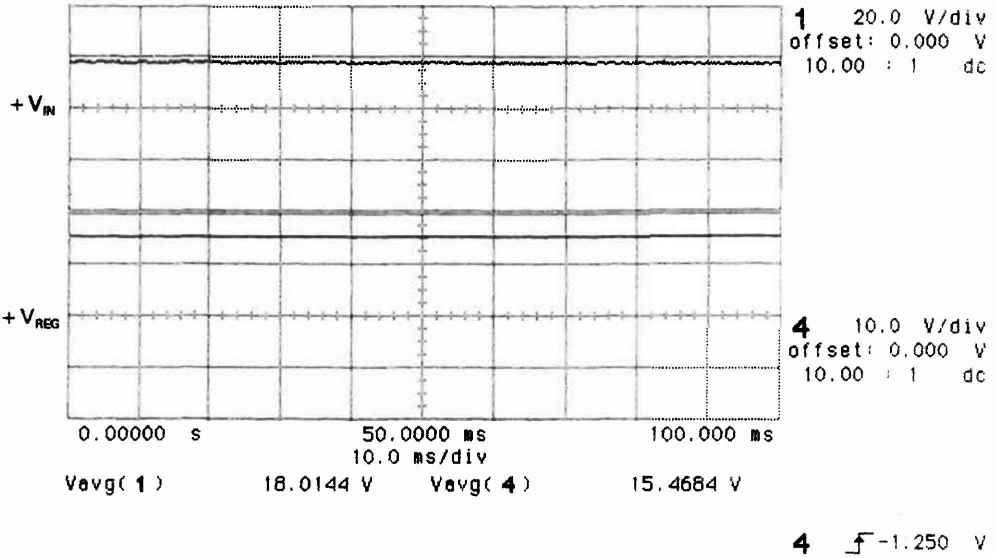
TABLE 6.3

	Design Goal	*Measured Value*
Input voltage	18–22 volts	18–22 volts
Output voltage	12–15 volts	12.5–15.5 volts
Output current	0–150 milliamperes	0–150 milliamperes
Line regulation	<2 percent	0.8 percent
Load regulation	<2 percent	0.012 percent



Low Line Voltage, Low Output, No Load

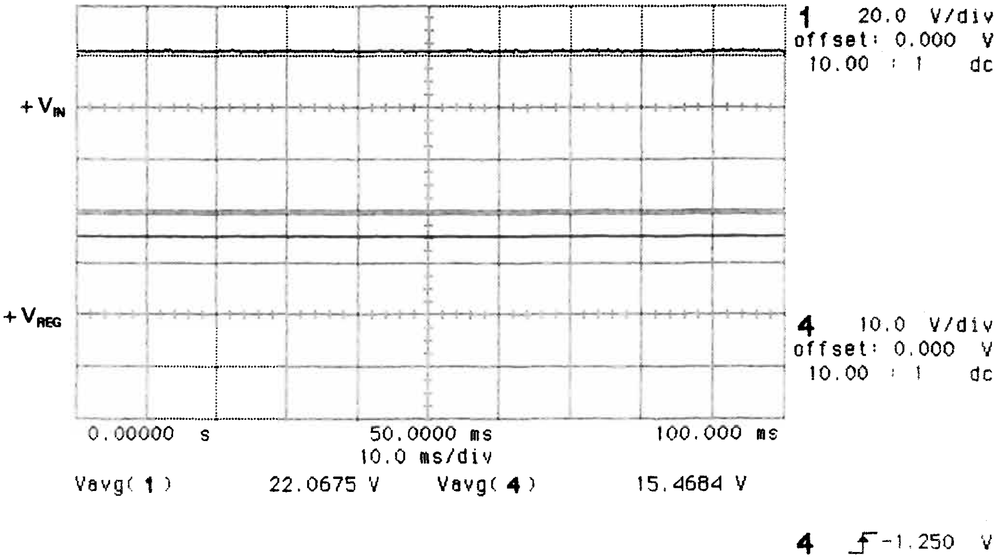
(a)



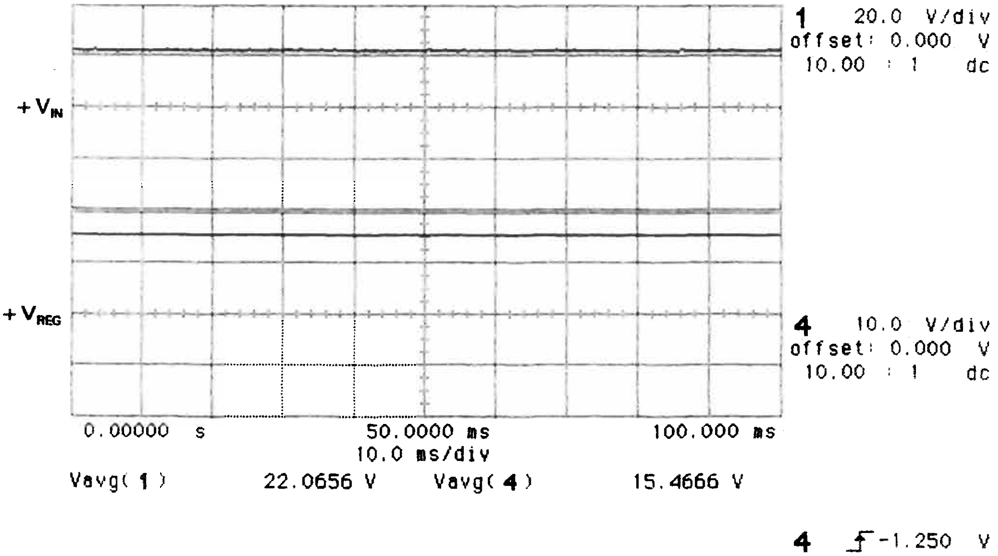
Low Line Voltage, High Output, No Load

(b)

FIGURE 6.15 Oscilloscope displays showing the performance of the regulator circuit shown in Figure 6.14. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*


High Line Voltage, High Output, No Load

(c)


High Line Voltage, High Output, Full Load

(d)

FIGURE 6.15 *Continued*

6.4 SWITCHING VOLTAGE REGULATORS

Our discussion on switching regulators will be limited to the theory of operation. Although a switching regulator can be designed around an op amp, most are built using specialized regulator ICs, which not only simplifies the design but generally improves the overall performance of the regulator circuit. Nevertheless, an understanding of the operation of switching regulators is very important to an engineer or technician working with equipment being designed today, and no discussion of regulated power supplies would be complete without this understanding.

6.4.1 Principles of Operation

Let us begin by examining the simplest of equivalent circuits. Figure 6.16 shows a simple switching circuit. Assume that the switch is operated at periodic intervals with equal open and closed times. When the switch is closed, the capacitor is charged by current flow through the coil. As current flows through the coil, a magnetic field builds out around it (i.e., energy is stored in the coil). When the switch is opened, the magnetic field around the coil begins to collapse, which makes the coil act as a power source (i.e., the stored energy is being returned to the circuit). You will recall from basic electronics theory that inductors tend to oppose changes in current. When the switch opens and the field begins to collapse, the resulting coil voltage causes circuit current to continue uninterrupted. The path for this electron current is right to left through the inductor, down through diode D, up through C (and the load) to the coil. This current will continue (although decaying) until the magnetic field around the coil has completely collapsed.

Now, if the switch were to close again before the coil current had time to decay significantly, and if it continued to open and close at a rapid rate, then there would be some average current through the coil. Similarly, this average current value would produce some average value of voltage across the capacitor and therefore across the parallel load resistor.

Suppose now that the ratio of closed time to open time on the switch is shortened. That is, the switch is left opened longer than it is closed. Can you see that the inductor's field will collapse more completely, and that the *average* current through the coil (and therefore load voltage) will decrease? On the other hand, if we lengthen the closed time of the switch relative to the open time, the average load voltage will increase.

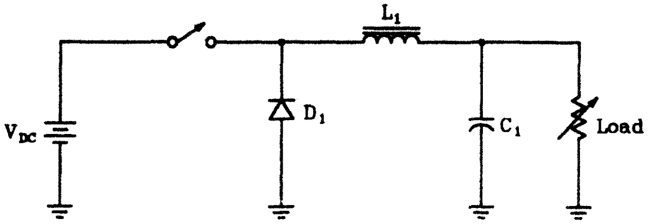


FIGURE 6.16 A simple circuit to help explain the principles of switching voltage regulators.

The basic behavior of capacitors is to oppose changes in voltage. That is, we cannot change the voltage across a capacitor instantaneously; the voltage can only change as fast as the capacitor can charge or discharge. The capacitor in Figure 6.16 is a filter and smooths the otherwise pulsating load voltage. So, even though the switch is interrupting the DC supply at regular intervals, the voltage is steady across the load because of the combined effects of the coil and capacitor. By varying the ratio of on time to off time (i.e., the duty cycle), we can vary the DC voltage across the load. If we sample the actual load voltage and use its value to control the duty cycle of the switch (a transistor in practice), then we will have constructed a switching regulator circuit.

Figure 6.17 shows a more accurate representation of a switching voltage regulator. Here the DC input voltage is provided by a standard transformer-coupled, bridge-rectifier circuit followed by a brute filter (C_1). The interrupting device is an n-channel, power MOSFET (Q_1). Gate drive for the MOSFET comes from a pulse width modulator circuit. This can be built around an op amp comparator/oscillator circuit, but is generally an integral part of an integrated circuit designed specifically for use in switching regulators.

The pulse width modulator has two inputs. One is the sample output voltage derived from a voltage divider (R_1 and R_2); the other is provided by a stable voltage reference. The pulse width modulator compares the reference voltage with the sampled output voltage (just as the series and shunt-linear regulators discussed in previous sections do) and alters the pulse width (effective duty cycle) of the signal going to the MOSFET. As the duty cycle of the MOSFET is altered, the average (i.e., DC) output voltage is adjusted and maintained at a constant value. If the load voltage tried to change, perhaps in response to a changing current demand, then this change would be fed back through the voltage divider to the pulse width modulator circuit. The pulse width going to the MOSFET would quickly be adjusted to bring the load voltage back to the correct value.

6.4.2 Switching versus Linear Voltage Regulators

Why go to all the trouble of interrupting the DC voltage and then turning right around and smoothing it back into DC again? Well, switching regulators do have some outstanding advantages over linear regulators. One of their primary advantages as compared to their linear equivalents is lower power dissipation.

In a linear regulator, the series pass transistor or the shunt regulator transistor dissipates a significant amount of power. Typical efficiencies for linear regulators are 30 to 40 percent, which means, for example, that a linear supply designed to deliver 12 volts at 3 amps DC actually draws at least 90 watts from the power line. The internal power loss results in heat, which in turn leads to cooling requirements like fans and heat sinks. Most of the power loss in a linear regulator is in the regulator transistors. Recall that their power dissipation is computed as

$$P_D = I_C V_{CE}$$

The switching regulator, on the other hand, typically achieves efficiencies on the order of 75 percent. This improvement is caused primarily by a dramatic reduction in power dissipation in the regulator transistor. Although the power dissipa-

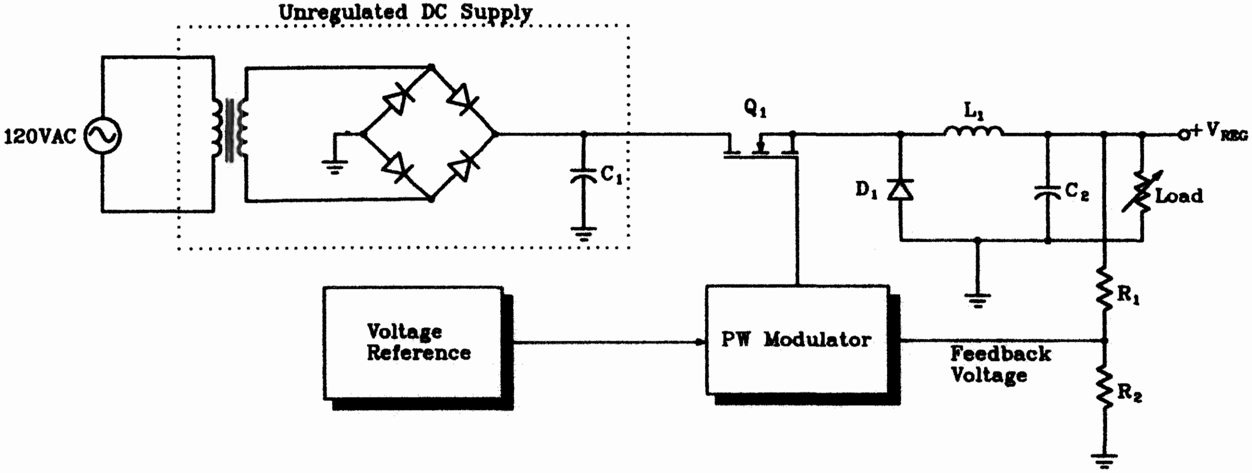

Unregulated DC Supply
120VAC
C_1
Q_1
L_1
$+V_{REG}$
D_1
C_2
Load
R_1
R_2
Voltage Reference
PW Modulator
Feedback Voltage

FIGURE 6.17 A switching regulator controls the switching operation of the pass transistor to regulate load voltage.

tion is computed in the same basic way, the results are quite different because the transistor is operated in either saturation or cutoff at all times. Thus, although the power at any given time is expressed as

$$P_D = I_C V_{CE}$$

either I_C is very low (at cutoff $I_C \approx 0$) or V_{CE} is very low (during saturation V_{CE} is *ideally* 0). Therefore, the only time the switching transistor dissipates significant power is **during** the actual switching time (a few microseconds).

The reduced power dissipation results in other advantages. Since the cooling requirement is less for a given output power, both size and cost of the associated circuitry and support components are less. It is reasonable to expect size reductions on the order of five or more.

Another advantage of switching regulators is that the output voltage can be stepped up, stepped down, and/or changed in polarity in the process of being regulated. This can simplify some designs.

Switching regulators are not without their disadvantages, however. First, they require more complex circuitry for control, although this is becoming less disadvantageous as more specialized regulator ICs are being provided to the power supply designer.

Another major disadvantage of switching regulators is electrical noise generation. Anytime a circuit changes states quickly, high-frequency signals are generated. You may recall from basic electronics theory that a square wave is made up of an infinite number of odd harmonics. So, if we have a 100-kilohertz square wave, we will be generating harmonic frequencies of 300 kilohertz, 500 kilohertz, 700 kilohertz, and so on. The Federal Communications Commission (FCC) in the United States and similar agencies in other countries restrict the amount of electromagnetic emissions that may leave an electronic device. For example, suppose you have designed a new computer that fits in the palm of your hand. The FCC will prevent you from marketing your new computer unless it can pass the FCC-defined emissions tests. Many new computer designs fail to pass these tests because of the electrical noise generated by switching power supplies. Now, this doesn't mean you can never use a switching regulator in a computer. Quite the contrary, most computers do use switching regulators. But additional components will have to be included to filter the high-frequency noise that is generated. This noise can easily extend into the 450-kilohertz to 150-megahertz band.

Finally, although switching regulators are good, they cannot respond as quickly to sudden changes in line voltage or load current. That is, they do not regulate as well as their linear counterparts if the line and load changes are rapid.

6.4.3 Classes of Switching Regulators

We can categorize switching regulators into four general groups based on the method used to control the switching transistor:

1. Fixed off time, variable on time
2. Fixed on time, variable off time

3. Fixed frequency, variable duty cycle
4. Burst regulators

First, it should be noted that all of the types listed work by switching the regulator transistor from *full off* to *full on*. Additionally, they all regulate by altering the ratio of on time to off time of the transistor. The various methods refer to the actual circuitry and waveform driving the switching transistor.

The first two regulator types listed are similar in that one alternation of the transistor drive signal is fixed. Regulation is achieved by adjusting the time for the remaining alternation. Because one alternation is fixed and one is variable, the frequency of operation inherently varies. These types are sometimes called variable frequency regulators.

The third class of switching regulators uses a constant frequency, but alters the duty cycle of the signal applied to the switching transistor. That is, if the on time is increased, the off time is decreased proportionately, so the output voltage can be controlled without altering the basic frequency of operation. This is one of the most common classes of switching regulators.

Finally, the burst regulator operates by gating a fixed-frequency, fixed-pulse-width oscillator on and off. The duty cycle of the switching waveform is such that the output voltage would be too high if the switching were continuous. The circuit senses this excessive output voltage and interrupts or stops the switching completely. With the switching transistor turned off continuously, the output voltage will quickly decay. As soon as it decays to the correct voltage, the switching is resumed. Thus, the regulation is actually achieved by periodically interrupting the switching waveform going to the switching transistor.

6.5 OVER-CURRENT PROTECTION

Regulated power supplies are often designed to be short-circuit protected. That is, if the output of the supply is accidentally shorted to ground or tries to draw excessive current, the supply will not be damaged. There are several classes of over-current protection:

1. Load interruption
2. Constant current limiting
3. Foldback current limiting

6.5.1 Load Interruption

The simplest form of over-current protection is shown in Figure 6.18. The protective device is generally a fuse (as shown in the figure), a fusible resistor, or a circuit breaker. In any case, once a certain value of current has been reached the protective device opens and completely isolates the load from the output of the supply. As long as the protective device is designed to operate at a lower current value than the absolute maximum safe current from the supply, the power supply will

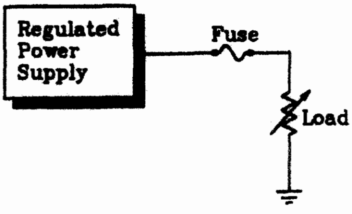


FIGURE 6.18 Load interruption is the simplest form of over-current protection.

be protected from damage. Since the protective element has resistance, it can adversely affect the overall regulation of the circuit.

6.5.2 Constant Current Limiting

Figure 6.19 shows a common example of a constant-current limiting circuit. This is identical to the series regulators discussed earlier in the chapter with the addition of R_1 and Q_2, which are the current limiting components. Under ordinary conditions, the voltage drop across R_1 is less than the turn-on voltage for the base-to-emitter junction of Q_2 (about 0.6 volts). This means that Q_2 is off and the circuit operates identically to the standard unprotected series regulator.

Now suppose the load current increases. This will cause an increased voltage drop across R_1. As soon as the R_1 voltage drop reaches the threshold of Q_2's base junction, transistor Q_2 will start to conduct. The conduction of Q_2 essentially bypasses the emitter-base junction of Q_1, which prevents any further increase in current flow through Q_1. We can better understand the operation of Q_2 if we view it in terms of voltage drops. At the instant Q_2 begins to turn on, there must be approximately 0.6 volts across R_1 and another 0.6 to 0.7 volts across the emitter-base junction of Q_1. Kirchhoff's Voltage Law shows us that there must therefore be about 1.2 to 1.3 volts between the emitter and collector of Q_2 when it starts to conduct, because the emitter-collector circuit of Q_2 is in parallel with the voltage drops of R_1 and the emitter-base circuit of Q_1. Any further attempt to increase current beyond this point will cause a decrease in the emitter-collector voltage of Q_2. As this voltage is in parallel with the series combination of Q_1's base-emitter junction and R_1, these voltages also tend to decrease. However, if the base-emitter voltage of Q_1 actually decreases, then the emitter current of Q_1 decreases, causing the voltage drop across R_1 to decrease, resulting in *less* conduction in Q_2 (the opposite of what is really occurring). So, in essence, the current reaches a certain maximum limit and is then forced to remain constant. Any effort to increase the current beyond this point merely lowers the output voltage.

The value of current required to activate Q_2 is determined with Ohm's Law. We simply find the amount of current through R_1 that it takes to get a 0.6-volt drop. That is, short-circuit current (I_{SC}) is computed as follows:

$$\boxed{I_{SC} = \frac{0.6}{R_1} \qquad (6.18)}$$

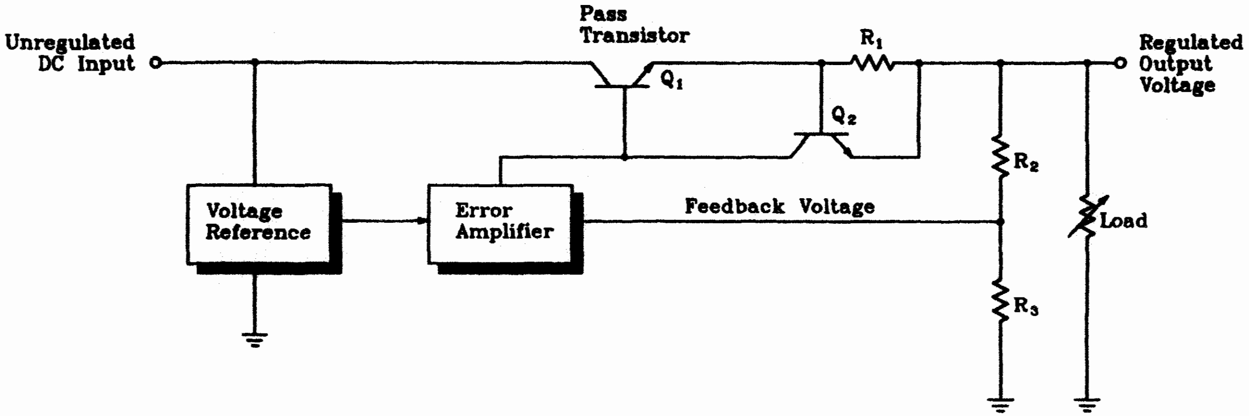

Pass Transistor
Unregulated DC Input
Q_1
R_1
Q_2
Regulated Output Voltage
R_2
Voltage Reference
Error Amplifier
Feedback Voltage
Load
R_3

FIGURE 6.19 A constant-current limiting technique is often used to protect series regulator circuits from over-current conditions.

6.5.3 Foldback Current Limiting

Figure 6.20 shows a simplified schematic diagram of a voltage regulator circuit that uses foldback current limiting. Note that resistors R_4 and R_5 have been added to the constant-current limiting circuit presented in Figure 6.19. Under normal conditions, transistor Q_2 is off and the circuit works just like the unprotected regulator circuit discussed in an earlier section. Voltage divider action causes a voltage drop across R_4, with the upper end being the most positive.

As load current increases, the voltage drop across R_1 increases, as it did in the constant current circuit. However, the voltage across R_1 must not only exceed the turn-on voltage of the base-emitter junction of Q_2 in order to turn Q_2 on, but also overcome the voltage across R_4. Once this point occurs, however, Q_2 begins to conduct and reduces the conduction of Q_1. This, of course, causes both the output voltage and the base voltage of Q_2 to decrease. However, because the base voltage of Q_2 is obtained through a voltage divider, it decreases more slowly than the output voltage. And, because the emitter of Q_2 is connected to the output voltage, it must also be decreasing faster than the base voltage. This causes Q_2 to conduct even harder, further limiting the output current.

If the load current increases past a certain threshold, the circuit will "fold back" the output current. That is, even if the output is shorted directly to ground, the current will be limited to a value that is **less** than the maximum normal operating current, which under overload conditions is a very desirable characteristic. Because the pass transistor will have the full input voltage across it when the output is shorted to ground, it is prone to high power dissipation. In fact, the constant-current limiting circuit previously discussed has maximum power dissipation under short-circuit conditions. By the current folding back under overload conditions, the dissipation of the pass transistor is reduced and a smaller device can be used.

6.6 OVER-VOLTAGE PROTECTION

Some applications require a regulator circuit with over-voltage protection to protect the load against regulator malfunctions. That is, under normal operating conditions, the output of the regulator should stay at the regulated level, but if the regulator fails (e.g., via emitter-to-collector short in the series pass transistor), the output may increase significantly over the regulated value and potentially cause damage to the load circuitry.

Figure 6.21 shows a common method of over-voltage protection that is built around a silicon-controlled rectifier (SCR). Under ordinary conditions, the voltage drop across R_4 is less than the base-emitter turn-on voltage of Q_2, and the circuit works identically to the unprotected circuit discussed earlier.

If a regulator malfunction causes the output voltage to rise above a threshold set by the ratio of R_4 and R_5, Q_2 turns on and provides gate current for the SCR, which causes it to fire. When an SCR has fired and is in the forward conducting state, the voltage drop across it is about 1 volt. Thus, the base voltage of Q_1 is quickly dropped to about 1 volt. Since the Q_1 base voltage is 1 volt, the output voltage will be dropped to a few tenths of a volt, and this condition will continue as long as the SCR remains in conduction. To reset the SCR, the anode current must

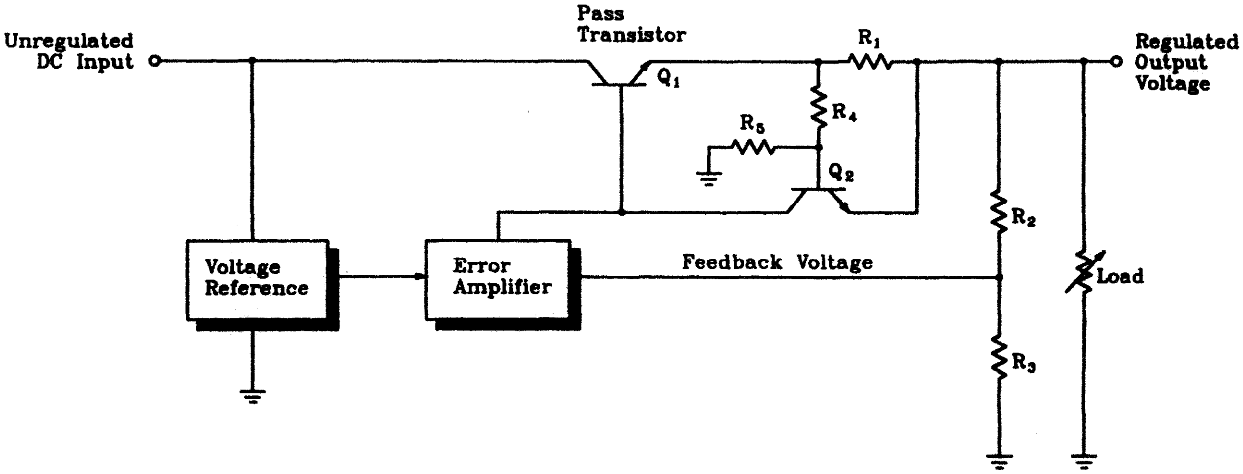

Unregulated
DC Input
Pass
Transistor
Q_1
R_1
R_4
R_5
Q_2
Regulated
Output
Voltage
R_2
Voltage
Reference
Error
Amplifier
Feedback Voltage
Load
R_3

FIGURE 6.20 Foldback current limiting actually decreases the output current under overload conditions.

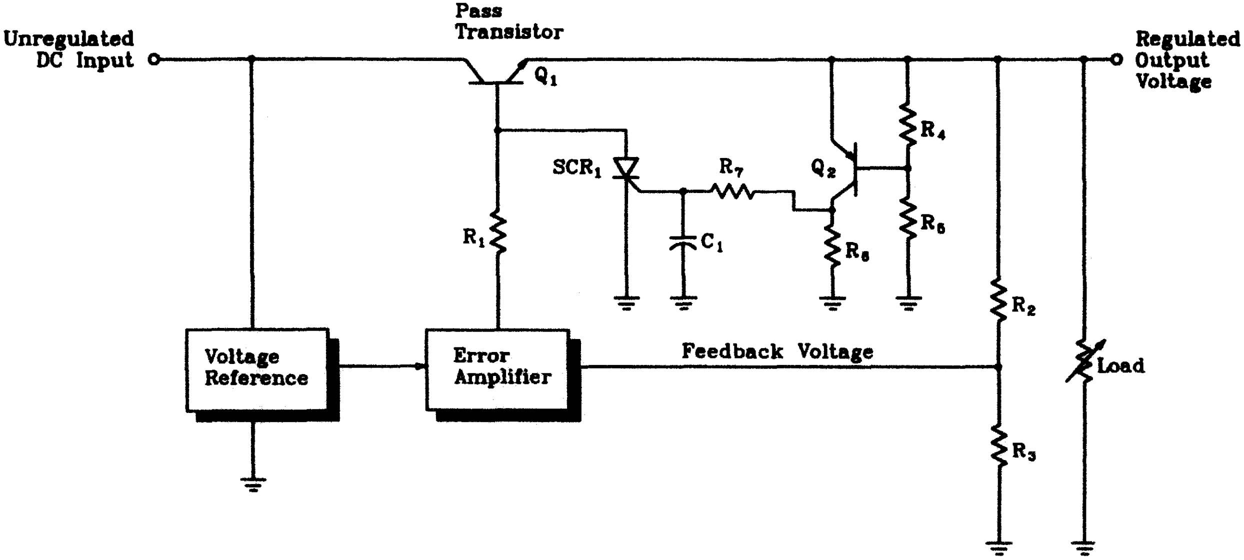

Pass Transistor
Unregulated DC Input
Q₁
Regulated Output Voltage
SCR₁
R₇
Q₂
R₄
R₅
R₁
C₁
R₆
R₂
Voltage Reference
Error Amplifier
Feedback Voltage
Load
R₃

FIGURE 6.21 A series regulator circuit with over-voltage protection.

fall below a minimum value, called *holding current*. In the circuit shown in Figure 6.21, the main power source must be momentarily turned off to reset the SCR.

Capacitor C_1 is a transient suppressor and prevents accidental firing of the SCR during initial turn-on of the regulator or as a result of a noise pulse.

Some power supply designs return the anode of the SCR directly to the unregulated DC input **with no limiting resistance.** If an over-voltage condition occurs and the SCR fires, the main supply is essentially shorted to ground via the SCR. This activates the current limiting features of the main supply (often a fuse in the primary of the supply transformer). When the SCR is connected in this way, the circuit is called a "crowbar" because it essentially throws a short circuit (like a steel crowbar) directly across the power supply.

6.7 POWER-FAIL SENSING

An op amp can be configured as a voltage comparator circuit and used to sense an *impending* power failure. This is commonly used in computer systems to protect the computer from erratic operation caused by power loss. If an impending power failure is detected, the computer quickly transfers all of the critical data to a permanent storage area that does not require power. Once power has been restored, the computer retrieves the stored data from the permanent memory and resumes normal operation. Figure 6.22 shows how an op amp can be used to detect an impending power failure and send a signal to a computer in time to save the critical data before the power actually goes away.

Under normal conditions, the inverting (–) input of the voltage comparator is more positive than the noninverting input. This is true even under conditions of minimum unregulated voltage. If a primary power loss occurs, the unregulated DC voltage will, of course, drop to 0; however, the filter capacitors (usually quite large) in the power supply will prevent the unregulated DC supply from decaying instantaneously. The regulator will continue to supply a constant voltage until the unregulated input voltage has decayed past a certain minimum point. Thus, up to

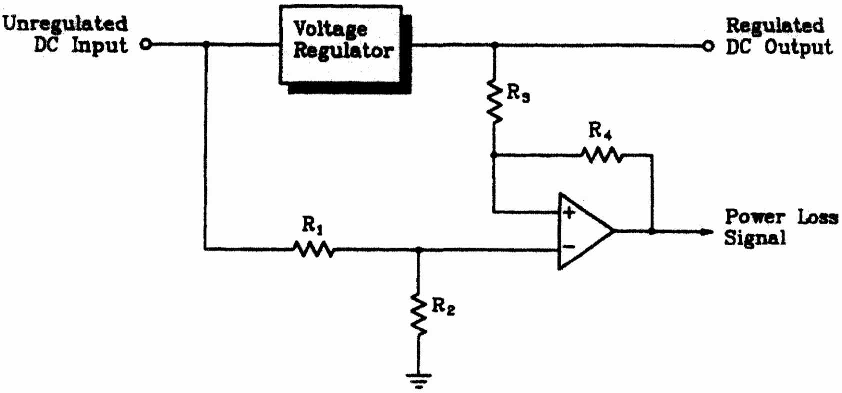


FIGURE 6.22 An op amp voltage comparator can be used to detect an impending power loss.

a point, the voltage on the (–) input to the comparator decays while the voltage on the (+) input remains constant. When the voltage on the (–) input passes the lower threshold of the voltage comparator, the output quickly changes states, signaling a coming power loss. A computer monitoring this signal can then take the necessary action to protect critical data. Resistors R_3 and R_4 provide hysteresis for the comparator.

The amount of time between primary power interruption and the point where the regulated output begins to drop is called *hold-up time* and is generally tens or even hundreds of milliseconds. Since a computer executes in the microsecond range, there is plenty of time to save the critical information **after** the unregulated input has started to decay but **before** the regulated output begins to drop.

6.8 TROUBLESHOOTING TIPS FOR POWER SUPPLY CIRCUITS

Power supply circuits are considered by some technicians and engineers to be simple, fundamental, nonglamorous, and even boring. However fundamental or boring the *purpose* of power supplies may be, the troubleshooting of a defective supply is not always a simple task. What complicates the troubleshooting of a regulator circuit is the closed-loop nature of the system. A defect in any part of the loop can upset the voltages at all other points in it, thus making it difficult to distinguish between cause and effect.

Nevertheless, armed with a thorough understanding of circuit operation and guided by systematic troubleshooting procedures, a defective regulator circuit can be quickly and effectively diagnosed. The following sequential steps will provide the basis for a logical, systematic troubleshooting procedure applicable to voltage regulator circuits:

1. **Observe the symptoms.** Because of the potentially high-power levels available in a supply, visible signs of damage are common. DO NOT, however, simply replace a burned component and reapply power—in many cases, the burned component is the result of a malfunction elsewhere in the supply. Nevertheless, detecting the burned component will help you narrow the range of possibilities.

   Symptom observation also includes taking careful note of the output symptoms. Is the output voltage too high, too low, 0, unregulated? Did the user of the equipment say how the problem was caused (e.g., an accidental short on the output)?
2. **Verify that the input to the regulator is correct.** If it is not correct, the regulator may not be the cause. On the other hand, if the problem is *no* input and the unregulated supply shows signs of damage, then suspect a short in the regulator circuit. In these cases, it is often helpful to disconnect the regulator circuit and get the unregulated supply back to normal as a first step. A simple way to disconnect series regulator circuits is to remove the pass transistor. This is a particularly simple task for socket-mounted power transistors.

3. **Check for possible short circuits.** Once the unregulated input voltage is shown to be correct, we can concentrate on the regulator portion of the supply. If the regulator was disconnected during step 2 and you have reason to believe a short circuit exists in the regulator, DO NOT reconnect the regulator and apply full power. If you do and a short does exist, the newly repaired unregulated source will be damaged again. A better approach is to connect the regulator to the unregulated supply via a current meter. Use a variable autotransformer to supply the AC power to the unregulated power supply, and slowly increase the AC input voltage while monitoring the current meter. If a short exists in the regulator, the current meter will exceed normal values with a very low-input voltage. If this is the case, you must rely on your theory of operation and an ohmmeter as your major tools.
4. **Open the regulator loop.** If the full supply voltage can be applied safely, but the regulator still doesn't work properly, then you can add a voltmeter to your tool kit. Since the regulator is inherently a closed-loop system, it is often difficult to distinguish between cause and effect. If the loop can be easily broken (e.g., removing a wire from the wiper arm of a potentiometer, removing a socket-mounted transistor, etc.), this can help isolate the problem. After the loop has been opened, you can inject your own "good" voltage at the open-loop point from an external DC supply. The system can then be diagnosed using the split-half method, signal tracing, and so on, like any other open-loop system.
5. **Force the circuit to known extremes.** If it is impractical to open the loop of the regulator, you can sometimes force a condition at one point in the loop and watch for a response at another point. Your understanding of the operation of the components between the forced point and the monitored point can lead you to the problem. A good example of forcing a condition is to either short the emitter-base circuit of a transistor to force it to cut off, or to short the emitter-collector circuit to simulate a saturated condition. Be sure to examine the circuit carefully before shorting these elements, but in most circuits neither of these shorts will cause damage (see step 6), although they will force the circuit to go to one of two extremes. The extreme change will be passed through the rest of the circuit if everything is normal. A defect, however, will not respond to the change and thus reveal its identity to an alert technician or engineer.
6. **Use special care with switching regulators.** Here the regulator transistor has been selected on the assumption that it is switching from full on to full off and therefore dissipating minimum power. If any portion of the regulator circuit causes the switching to stop and the pass transistor is in the ON state, then the pass transistor will almost certainly be damaged. This has two important ramifications. First, if your diagnosis reveals that no switching signal is being applied to the switching transistor, then suspect a bad transistor *after you correct the switching signal problem*. Second, you should never intentionally stop the oscillation in a switching supply by shorting components as described in step 5.

7. **Substitute the load.** Another method that can be helpful in isolating some power supply defects is to remove the load. This eliminates the possibility that a malfunction in the system is causing the supply to appear defective. If the supply is shown to be defective, substituting an equivalent resistance in place of the system circuitry can simplify troubleshooting of the actual power supply. Additionally, it removes the possibility of causing damage to the system circuitry if the output of the supply becomes excessively high while troubleshooting the problem. (For example, a test probe may slip and cause a momentary short circuit.)

REVIEW QUESTIONS

1. List the three basic classes of voltage regulator circuits.
2. If the DC output voltage of a shunt regulator circuit varies between 11 and 12.5 volts as the input line voltage varies from 110 to 130 volts, what is the percent of line regulation for the regulator?
3. If a series regulator circuit provides 25 volts DC under no-load conditions, but drops to 24.3 volts when a full load is applied, what is the percent of load regulation for the regulator circuit?
4. If each of the following rectifier/regulator circuits requires 1.2 amps of current from the 120-VAC input line, which one will probably deliver the highest current to a 12-VDC load: series, shunt, switching? Explain your choice.
5. Refer to Figure 6.8. If the input voltage is 16.8 VDC and the regulated output voltage is 8.9 volts DC, what is the power dissipation of Q_1 with a 300-mA load connected?
6. Refer to Figure 6.8. If the reference voltage has a defect that causes it to go to +6 volts, what is the effect on output voltage (increase, decrease, remains the same)? Explain your answer.
7. Refer to Figure 6.8. If resistor R_2 increases in value, what relative effect does this have on output voltage?
8. Refer to Figure 6.9. What is the effect on output voltage if resistor R_2' increases in value?
9. Refer to Figure 6.12. What is the effect on the current flow through Q_1 if resistor R_2 is decreased in value? Explain your answer.
10. If resistor R_3 in Figure 6.12 is changed to 40 ohms (and no components are damaged), what will happen to the value of reference voltage? What will happen to the value of output voltage ($+V_{REG}$)? What will happen to the value of current through Q_1? Will the current through R_1 change?
11. Refer to Figure 6.19. What is the effect on the current flow through the load resistor (assume a constant value of load resistance) if resistor R_2 is increased in value?
12. Refer to Figure 6.19. What happens to the value of voltage dropped across the emitter-collector circuit of Q_1 if resistor R_3 is increased in value?
13. Refer to Figure 6.20. What is the effect on circuit operation if transistor Q_2 develops an emitter-to-collector short?
14. Refer to Figure 6.21. What is the effect on circuit operation if capacitor C_1 develops a short circuit?
15. Refer to Figure 6.21. What is the effect on circuit operation if resistor R_4 becomes open?

CHAPTER SEVEN

Signal Processing Circuits

Most of the circuits presented in this chapter serve to condition analog signals for subsequent input to another circuit. Many of them could be categorized as wave-shaping or conditioning circuits. We will, for example, examine circuits that can rectify low amplitude signals, limit the maximum excursion of signals, and change the DC level of waveforms. Many of the circuits are quite simple in terms of component count, but they play important roles in overall systems design.

7.1 THE IDEAL DIODE

Several of these circuits behave as though they had perfect or ideal diodes. Figure 7.1 contrasts the forward-biased characteristics of a perfect diode with that of a typical silicon diode.

Figure 7.1(a) shows a simple series circuit driven by an AC source. The output is taken across the diode. Basic circuit theory tells us that when the diode is reverse-biased, it acts as a very high impedance (i.e., essentially an open circuit). In the case of the circuit in Figure 7.1(a), we can expect to see nearly the full input voltage across the diode during times of reverse bias.

When the diode in Figure 7.1(a) is forward-biased, we expect it to act as a short circuit (or at least a very low impedance). In this case, there would be very little voltage across it. Figure 7.1(b) shows the output waveforms that we can expect. We see that the ideal diode has **no** voltage across it when it is forward-biased, which is in contrast with the silicon-diode waveform that has a 0.7-volt drop during forward-biased times. For purposes of this chapter, we will limit our comparisons to the forward-biased performance of the diodes. Therefore, Figure 7.1(b) shows similar waveforms for both ideal and silicon diodes during reverse bias.

With regard to effect on circuit operation, is the 0.7-volt drop across the forward-biased silicon diode important? Does it adversely affect the circuit's performance? Well, many times we ignore the 0.7-volt drop when analyzing or even designing circuits and get along quite well. But consider the circuit shown in Fig-

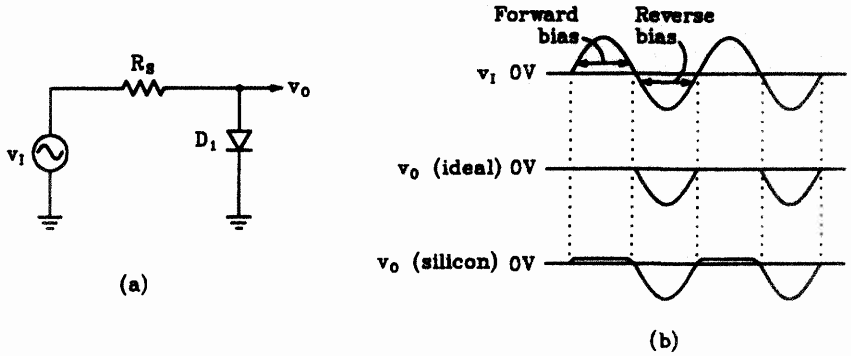


FIGURE 7.1 Comparison of silicon and ideal diodes.

ure 7.2 very closely. What is the peak amplitude of the output voltage (v_O)? Contrast the output voltage for both ideal and silicon diodes.

The ideal diode, of course, produces a peak output that is equal to the input peak. The silicon diode, on the other hand, will drop 0.7 volts when it conducts, leaving us with a maximum output voltage of $V_{PK} - 0.7$. Is that a problem? No, as long as the input signal is fairly large. However, what if the peak input signal is only 150 millivolts? You can see that the ideal diode will still produce the expected output waveform, but the silicon diode will have *no* output because the input never goes high enough to forward-bias the junction. Thus, the silicon diode acts as a high impedance throughout the input cycle. In this case, that 0.7-volt difference between an ideal and a real diode makes the difference in whether or not the circuit will even work.

Figure 7.3 shows how an ideal half-wave rectifier can be made by placing silicon diodes in the feedback loop of an op amp. During the positive half cycle of the input waveform, diode D_1 is forward-biased, making the feedback resistance very low. Thus, the gain of the inverting amplifier is computed as

$$A_V = -\frac{R_F}{R_{IN}} \approx \frac{0\ \Omega}{10\ k\Omega} = 0$$

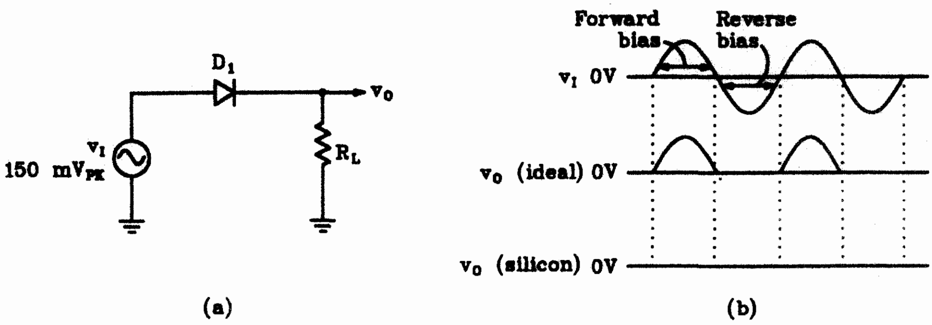


FIGURE 7.2 The forward voltage drop of a silicon diode can prevent rectification of small signals.

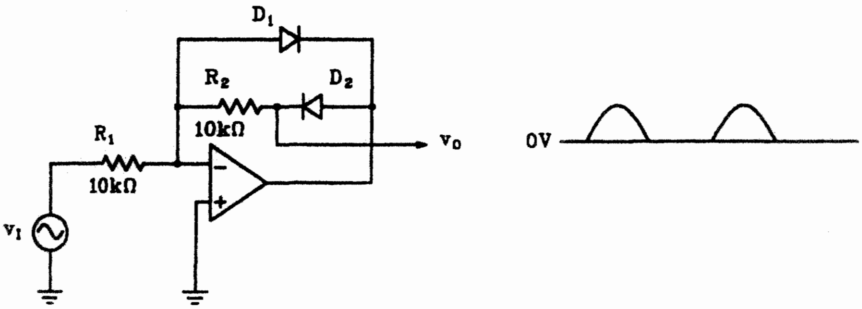


FIGURE 7.3 A half-wave rectifier that simulates an ideal diode.

Additionally, since diode D_2 is reverse-biased, no current will flow through R_2, so the output signal (v_O) will be 0.

On the negative half cycle, diode D_2 is forward-biased, completing the feedback loop through R_2. Since the current through R_2 is identical to the current through R_1 (ignoring bias currents), the voltage drop across R_2 will be identical to the input voltage. The left end of R_2 is connected to a virtual ground, while the right end provides the inverted rectified output signal.

It is important to see that the 0.7-volt drop across the diodes has no effect on the output signal. Even if the input were only a few tenths of a volt, the circuit would still produce a full amplitude output signal. This same principle is applied to several of the circuits that follow. By including the diode in the feedback loop of the op amp, we make the *effects* of its nonideal forward voltage drop disappear.

7.2 IDEAL RECTIFIER CIRCUITS

Both half- and full-wave ideal rectifier circuits can be made with standard silicon diodes and an op amp. Figure 7.4 shows a dual half-wave rectifier. It is similar to the circuit presented in Figure 7.3 with the addition of R_3 and R_4. The two outputs,

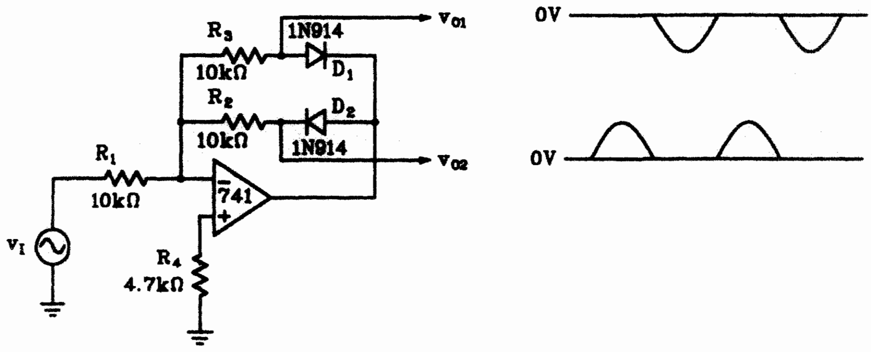


FIGURE 7.4 A dual, ideal diode, half-wave rectifier circuit delivering both positive and negative outputs.

one positive and one negative, can be used independently or combined in another op amp to produce a full-wave, precision-rectified signal.

7.2.1 Operation

Since the op amp in Figure 7.4 is operated with closed-loop negative feedback, the inverting (–) input pin is a virtual ground point. Thus, for practical purposes, one end of resistors R_1, R_2, and R_3 is connected to ground. This means that the total input voltage will be developed across R_1, causing an input current to flow through R_1. Since negligible current will flow in or out of the (–) terminal, all of the input current continues through either R_2 or R_3.

On positive input alternations, electron current will leave the output terminal of the op amp and flow through D_1, R_3, and R_1 and out to the positive source. Since resistors R_1 and R_3 are equal values, they will develop equal voltages, so we can expect the voltage across R_3 to be the same as the input voltage. Because one end of R_3 is grounded, the other end (v_{O1}) provides a signal equal in amplitude to the positive alternation of the input signal. However, because of the direction of current flow through R_3, the polarity of the v_{O1} is inverted from v_I and produces negative half-wave waveforms.

During the negative alternation of the input cycle, electron current leaves the source and flows through R_1, R_2, and D_2 and into the output of the op amp. Here again, because resistors R_1 and R_2 have the same current and are equal in value, they will have equal voltage drops. Thus, we expect to see a signal at v_{O2} that is the same amplitude as the input. Additionally, as a result of the direction of the current flow, the v_{O2} output will provide a positive half-wave signal.

7.2.2 Numerical Analysis

The numerical analysis of the dual, half-wave rectifier circuit shown in Figure 7.4 is fairly straightforward. We will determine the following characteristics:

1. Maximum unclipped output signals
2. Voltage gain
3. Maximum input without distortion
4. Highest frequency of operation

Maximum Output Signal. Outputs v_{O1} and v_{O2} are one diode drop away from the output of the op amp when their respective diode is conducting. Therefore, the maximum amplitude that we can expect at outputs v_{O1} and v_{O2} is 0.7 volts less than the maximum output of the op amp. That is,

$$\boxed{v_{O1}(\max) = -V_{SAT} + 0.7 \qquad (7.1)}$$

Similarly, the maximum amplitude for the v_{O2} output is computed as

$$\boxed{v_{O2} = +V_{SAT} - 0.7 \qquad (7.2)}$$

The manufacturer's data sheet provides us with worst-case and typical values for the maximum output swing. The minimum output swing for loads of 2 kilohms or more is listed as ±10 volts with a typical swing listed as ±13 volts. The typical value for loads of greater than 10 kilohms is ±14 volts. For our current analysis, let us use ±13 volts as the maximum output swing with ±15 volts V_{CC}. The maximum amplitudes for v_{O1} and v_{O2}, then, are computed as

$$v_{O1} = -13\ V + 0.7\ V = -12.3\ V,\ and$$

$$v_{O2} = +13\ V - 0.7\ V = +12.3\ V$$

Voltage Gain. The voltage gain on either half cycle is found using the basic gain equation for inverting amplifiers, Equation (2.6). In our present case, both half cycles will have the same gain because resistors R_2 and R_3 are the same value. We will compute the voltage gain of the amplifier using R_2 as the feedback resistor.

$$A_V = -\frac{R_F}{R_I} = -\frac{R_2}{R_1} = -\frac{10\ k\Omega}{10\ k\Omega} = -1$$

For most applications, resistors R_2 and R_3 are equal, but this is not necessary if unequal gains are desired.

Maximum Input without Distortion. We compute the highest input signal that we can have without distorting the output by applying our basic amplifier gain equation, Equation (2.1). As mentioned in the preceding section, both half cycles have the same gain in this particular circuit. Let's compute the maximum input by using the maximum positive output signal:

$$A_V = \frac{v_{OUT}}{v_{IN}},\ or$$

$$v_{IN} = \frac{v_{OUT}}{A_V}$$

$$v_I = \frac{12.3\ V}{-1}$$

$$= -12.3\ V$$

Highest Frequency of Operation. The amplifier, in this case, is basically amplifying sinewaves. In fact, the actual output terminal of the op amp will have a sinusoidal waveform present, but, of course, the circuit can be used with nonsinusoidal inputs as well. The bandwidth considerations of the amplifier are identical to those discussed in Chapter 2. The upper frequency limit will be established by the finite bandwidth of the op amp or by the limits imposed by the op amp slew rate. Since the amplifier is configured for unity voltage gain, we can expect the bandwidth limitation to be similar to the unity gain bandwidth of the op amp. The manufacturer's data sheet lists this limit as 1.0 megahertz.

The slew rate will likely impose a lower limit unless we apply only very-low-amplitude signals. Assuming that we intend to apply maximum-amplitude signals at some time, the highest frequency that can be amplified without slew rate distortion is computed using Equation (2.11).

$$\begin{aligned} f_{SRL} &= \frac{slew\ rate}{\pi v_O(\max)} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 26\ V} \\ &= 6.12\ kHz \end{aligned}$$

where $v_O(\max)$ is the maximum swing on the output of the op amp and the 0.5-volts-per-microsecond slew rate is given by the manufacturer for the 741 op amp. So, if we expect to rectify maximum amplitude signals, we will be limited to 6.12 kilohertz or less. On the other hand, if the application uses only lower amplitude signals, then a wider bandwidth can be expected.

7.2.3 Practical Design Techniques

Let us now design a dual, half-wave rectifier circuit that satisfies the following design goals:

1. Peak input voltage	±250 millivolts to ±5.0 volts
2. Peak output voltages	±375 millivolts to ±7.5 volts
3. Minimum input impedance	3000 ohms
4. Highest input frequency	25 kilohertz

Compute the Required Voltage Gain. The design goals give no indication that we are to design for unequal gains on the two different half cycles. The required amplifier gain, then, is computed by applying the basic gain equation, Equation (2.1).

$$A_V = \frac{v_O}{v_I} = \frac{375\ mV}{250\ mV} = 1.5$$

Of course, we could also have used the higher values of 5 volts and 7.5 volts for input and output voltage, respectively. This calculation gives us the absolute value of required voltage gain. By virtue of the circuit configuration, we know the gain will be inverting (i.e., $A_V = -1.5$).

Select R_1. You will recall from our discussions of amplifiers in Chapter 2 that the input impedance of an inverting amplifier is determined by the value of input resistor. In our present case, resistor R_1 must be large enough to satisfy the minimum input impedance requirement. Additionally, there is little reason to go beyond a few hundred kilohms. For the present design example, let us select R_1 as 20 kilohms.

Compute R_2 and R_3. In our current design, resistors R_2 and R_3 will be equal because the gains for the two half cycles must be equal. We compute the value of R_2 (or R_3) by applying a transposed version of the inverting amplifier gain equation, Equation (2.6).

$$A_V = -\frac{R_2}{R_1}, \text{ or}$$

$$\begin{aligned} R_2 &= -A_V \times R_1 \\ &= -(-1.5) \times 20\ k\Omega \\ &= 30\ k\Omega \end{aligned}$$

If this were not a standard value, we would have to choose a close value or some combination of resistors to equal the required value.

Select D_1 and D_2. These diodes are fairly noncritical and can be one of many different diode types. There are two primary factors to consider when selecting these diodes:

1. Average forward current
2. Peak inverse voltage

The highest reverse voltage that will be applied to either of the diodes is $\pm V_{SAT}$ (depending on the diode being considered). In most cases (including the present case) the two saturation voltages are equal. Therefore, we will need to select a diode with a peak inverse voltage rating greater than

$$V_{PIV}(rating) > V_{SAT} \tag{7.3}$$

Of course, in our particular case this means that we will need diodes with reverse breakdown ratings of over 13 volts. This should be a simple task.

The average rectified current that flows through a particular diode is computed with Equation (7.4).

$$I_{AVG} = 0.318 \frac{v_I(peak)}{R_1} \tag{7.4}$$

For our present application, the average forward current is computed as

$$I_{AVG} = 0.318 \frac{5\ V}{2\ k\Omega} = 79.5\ \mu A$$

Again, this rating is so low that most any diode should be capable of handling this current. For our present design, let us use the common 1N914A diodes because of cost and availability considerations.

Compute R_4. Resistor R_4 helps to minimize the output offset voltage that is caused by the op amp bias currents that flow through R_1, R_2, and R_3. Its value should be equal to the parallel combination of R_1 and either R_2 or R_3. In the present case, we compute R_4 as

$$R_4 = R_1 \| R_2 = \frac{1}{\dfrac{1}{20\ k\Omega} + \dfrac{1}{30\ k\Omega}} = 12\ k\Omega$$

Select the Op Amp. Two of the more important characteristics that must be considered when selecting the op amp are

1. Unity gain bandwidth
2. Slew rate

The minimum unity gain bandwidth requirement can be estimated with Equation (2.16) by substituting our actual closed-loop gain for A_{OL}:

$$\begin{aligned} A_{OL} &= \frac{f_{UG}}{f_{IN}},\ or \\ f_{UG} &= A_{OL} f_{IN} \\ &= 1.5 \times 25\ kHz \\ &= 37.5\ kHz \end{aligned}$$

The minimum slew rate for the op amp is computed by applying Equation 2.11. The required slew rate for our present design is computed as

$$f_{SRL} = \frac{slew\ rate}{\pi v_O(\text{max})},\ or$$

$$slew\ rate = \pi f_{SRL} v_O(\text{max}) = 3.14 \times 25\ kHz \times 15\ V = 1.18\ V/\mu S$$

The bandwidth requirement is easy to satisfy with nearly any op amp. The 1.18-volts-per-microsecond slew rate, however, exceeds the capabilities of the standard 741 op amp, but the MC1741SC op amp will work well for this application. Let us choose the latter device.

Figure 7.5 shows the final schematic of our dual, half-wave rectifier circuit. Its performance is indicated by the oscilloscope displays in Figure 7.6. Figures

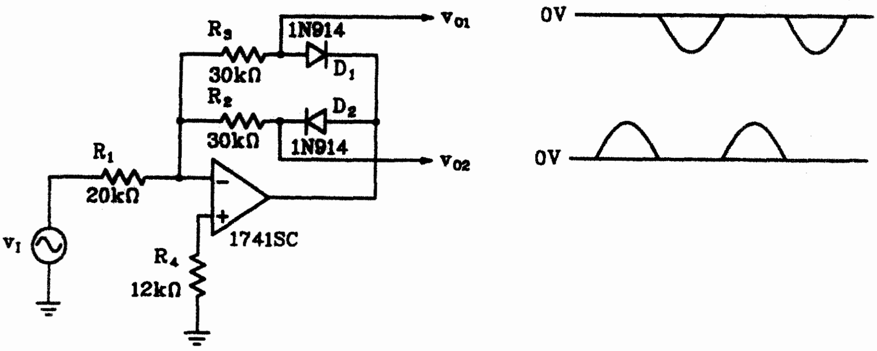
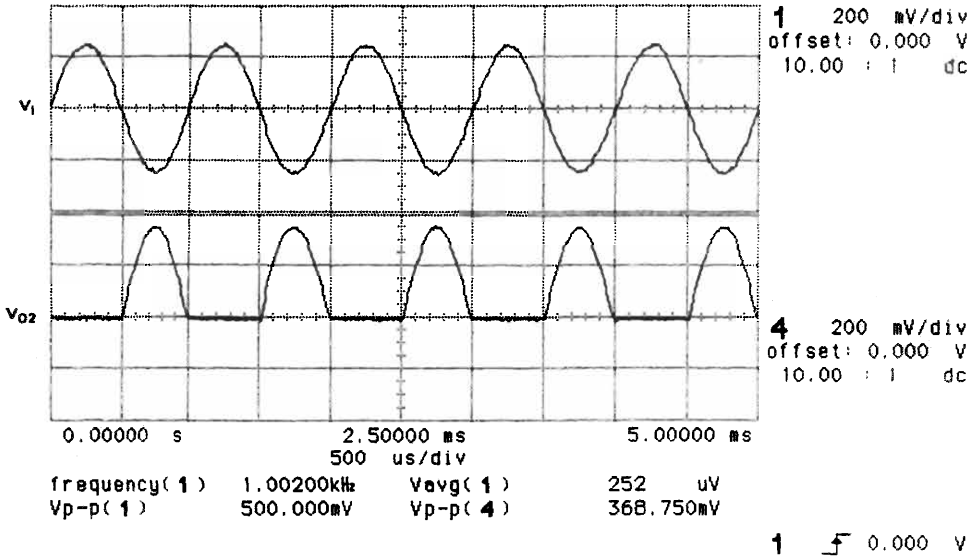


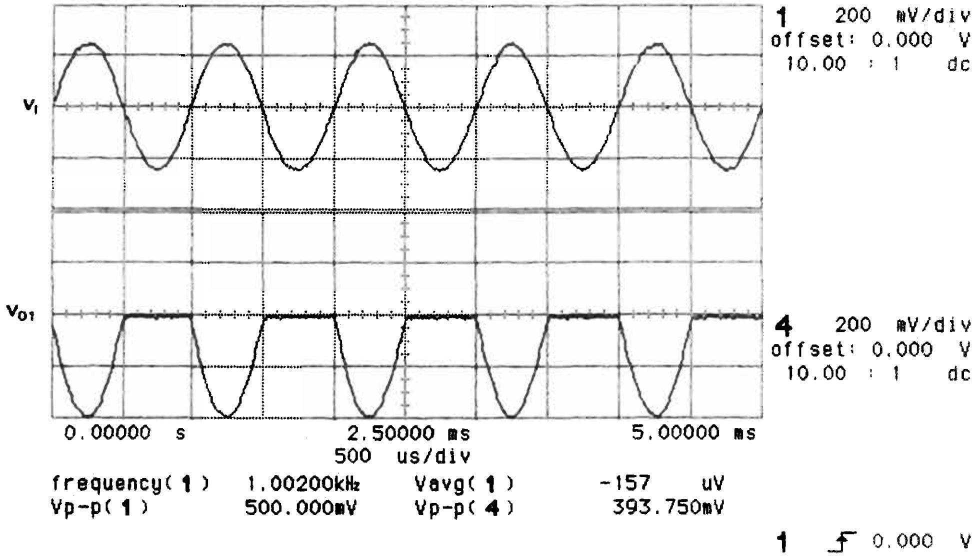
FIGURE 7.5 Final configuration of a dual half-wave rectifier circuit designed for 25 kilohertz operation.

Low Input Voltage, Low Frequency



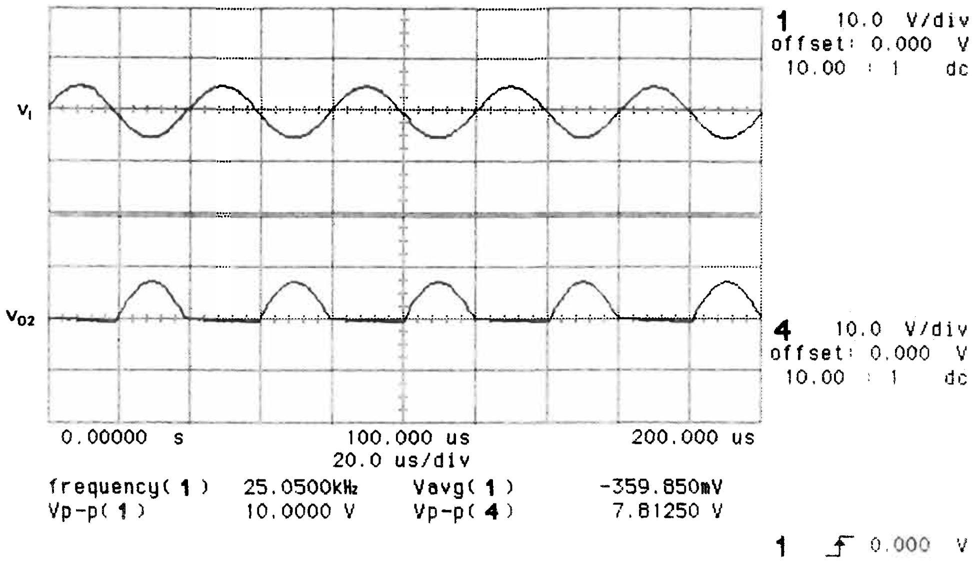
(a)

Low Input Voltage, Low Frequency



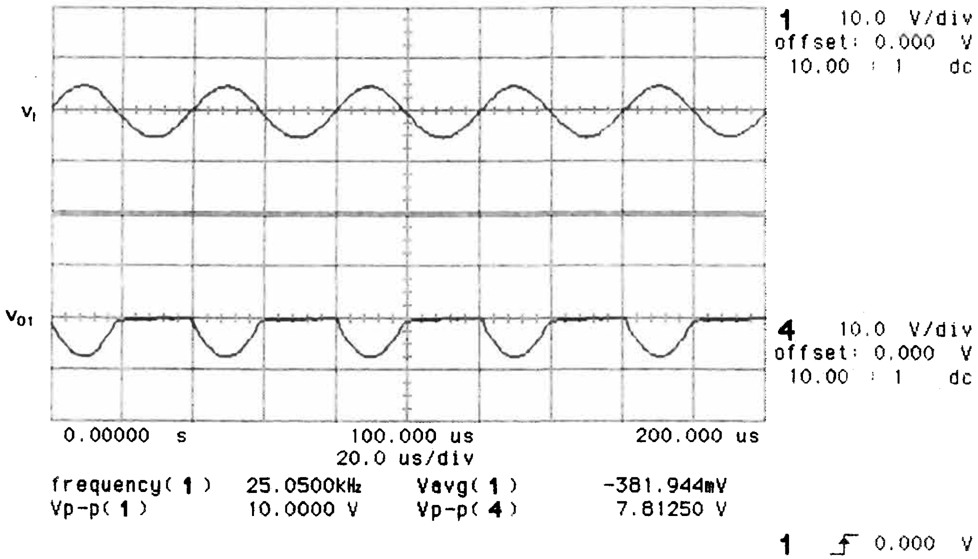
(b)

FIGURE 7.6 Oscilloscope displays showing the performance of the circuit shown in Figure 7.5. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*



High Input Voltage, High Frequency

(c)



High Input Voltage, High Frequency

(d)

FIGURE 7.6 *Continued*

TABLE 7.1

	Design Goal	*Measured Value*
Input voltage	250 millivolts–5 volts (peak)	250 millivolts–5 volts (peak)
Output voltage	375 millivolts–7.5 volts (peak)	368 millivolts–7.8 volts (peak)
Input impedance	≥3.0 kilohms	20 kilohms
Input frequency	0–25 kilohertz	0–25 kilohertz

7.6(a) and 7.6(b) show the positive and negative outputs, respectively, with a 250-millivolt peak input signal at a frequency of 1.0 kilohertz. Notice that the effect of the 0.7-volt forward voltage drop of diodes D_1 and D_2 is nonexistent. Figures 7.6(c) and 7.6(d) show the circuit's response to a 25-kilohertz signal with maximum input voltage. Finally, the actual performance of the circuit is contrasted with the original design goals in Table 7.1.

7.3 IDEAL BIASED CLIPPER

You may recall from basic electronics theory that a biased clipper or limiter circuit has no effect on the input signal as long as it is less than the clipping or reference voltage. Under these conditions, the input and output waveforms are identical. If, however, the input voltage exceeds the clipping level of the circuit, then the output waveform is clipped or limited at the clipping level. Figure 7.7 shows a basic biased shunt clipper and its associated waveforms. We can make both series and shunt, and both biased and unbiased, clippers with an op amp, just as we can with simple diode circuits. The difference, however, is that the op amp version eliminates the effect of the diode's forward voltage drop (0.7 volts). This is a very important consideration when processing low-amplitude signals.

7.3.1 Operation

Figure 7.8 shows the schematic diagram of an op amp version of the biased shunt-clipper circuit. The basic purpose is similar to the simple diode clipper shown in Figure 7.7, but because the effects of the diode's forward voltage drop have been

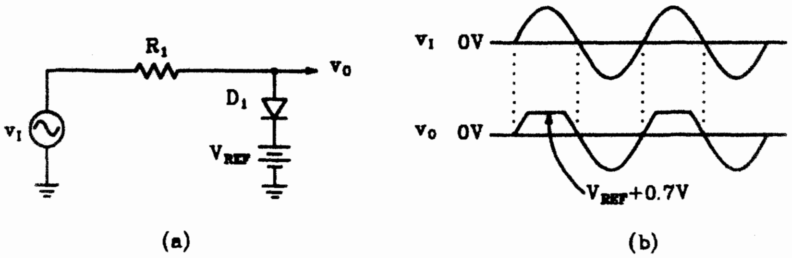
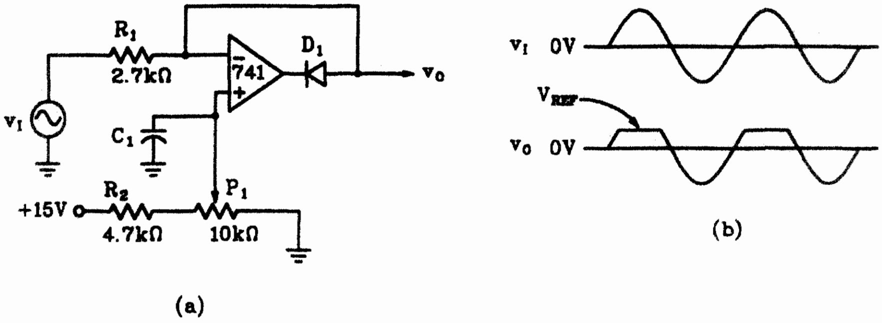


FIGURE 7.7 A simple biased shunt-clipper circuit. The output signal cannot go above $V_{REF}+0.7$ volts.



(a)

(b)

FIGURE 7.8 An ideal biased shunt-clipper circuit. The forward voltage drop of D_1 has no effect on circuit operation.

eliminated, the circuit performs like an ideal clipper circuit. Potentiometer P_1 is used to establish the reference voltage or clipping level on the (+) input pin. Capacitor C_1 prevents fluctuations in the clipping level.

Let us first consider the operation of the circuit for input voltages that are less than the value of the reference voltage. Under these conditions, the inverting (−) input is always less positive than the noninverting (+) input of the op amp. Therefore, the output of the op amp will remain at a positive level. The positive voltage on the output of the op amp reverse-biases diode D_1 and essentially opens the feedback loop. This allows the output of the op amp to go to $+V_{SAT}$ and remain there. With diode D_1 reverse-biased (essentially open), the op amp circuit has no effect on the output signal.

Figure 7.9 shows the equivalent circuit under these conditions. We would expect v_O to be identical to v_I as long as we avoid excessive loading. The equivalent circuit shown in Figure 7.9 does reveal a disadvantage of the shunt-clipper circuit: It has a fairly high output impedance, which means either that it will load easily or that we will have to follow it with a buffer amplifier.

Now let us consider circuit operation (Figure 7.8) for input signals that exceed the reference voltage. Under these conditions, the output of the op amp will start to move in the negative (i.e., less positive) direction. This causes diode D_1 to become forward-biased and closes the feedback loop. With a closed loop, we know that the voltage on the (−) input will be equal to the voltage on the (+) input (i.e., $+V_{REF}$). Since the output is taken from this same point, it will therefore be equal to $+V_{REF}$ under these conditions. In other words, as long as the input voltage is more positive than $+V_{REF}$, diode D_1 will remain forward-biased, and the voltage on the (−) input and at the output of the circuit will remain at the $+V_{REF}$ level.

If diode D_1 is reversed, then the circuit will clip the negative excursion of the input signal. Similarly, if the polarity of the reference voltage is reversed, the clipping will occur below 0.

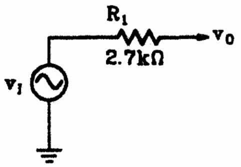


FIGURE 7.9 The equivalent circuit for the clipper circuit shown in Figure 7.8 for input signals that are less than $+V_{REF}$.

7.3.2 Numerical Analysis

Let us now extend our understanding of circuit operation to include the numerical analysis of the circuit shown in Figure 7.8. We will compute the following characteristics:

1. Minimum and maximum clipping levels
2. Highest frequency of operation
3. Maximum input voltage swing
4. Input impedance
5. Output impedance

Clipping Levels. The clipping level in the circuit is determined by the voltage on the wiper arm of P_1. When the wiper arm is in the extreme right position, the reference voltage (and clipping level) will be 0 volts, as the wiper arm will be connected directly to ground. The maximum clipping level will occur when the wiper arm is moved to the leftmost position. Under these conditions, the reference voltage is determined by applying the basic voltage divider formula:

$$\begin{aligned} +V_{REF} &= V_{APP}\frac{P_1}{P_1 + R_2} \\ &= +15\ V\frac{10\ k\Omega}{10\ k\Omega + 4.7\ k\Omega} \\ &= 10.2\ V \end{aligned}$$

Highest Frequency of Operation. Because the feedback loop is essentially open-circuited for a majority of the input cycle, the highest frequency of operation is more dependent on slew rate than on the bandwidth of the op amp. As the frequency increases, the output will begin to develop some degree of overshoot. That is, the output will rise beyond the clipping level momentarily and then quickly drop to the desired level. This overshoot is caused when the output of the op amp switches more slowly than the input signal is rising. Thus, we continue to see the full input waveform at the output until the amplifier actually switches. The switching time, of course, is determined by the slew rate of the op amp. There is no precise maximum frequency of operation. The upper limit is determined by the degree of overshoot considered acceptable for a particular application. For purposes of our analysis and subsequent design, we will consider a 1-percent overshoot to be acceptable. With this in mind, we can estimate the highest frequency of operation as follows:

$$\boxed{f_{MAX} = \frac{slew\ rate}{100(+V_{SAT} - V_{REF}(\min))} \qquad (7.5)}$$

For the circuit shown in Figure 7.8, we estimate the highest frequency of operation (for a 1-percent overshoot) as

$$f_{\max} = \frac{0.5\ V/\mu s}{100(13\ V - 0\ V)} = 385\ Hz$$

We can get higher operating frequencies either by accepting a higher overshoot or by selecting an op amp with a higher slew rate.

Maximum Input Signal. During the time that D_1 (Figure 7.8) is reverse-biased, the full input signal is felt on the (–) input of the op amp. The manufacturer's data sheet indicates that the maximum voltage that should be applied to this input is equal to the supply voltage. So, in the case of the circuit in Figure 7.8, the peak input voltage should be limited to 15 volts.

Input Impedance. The instantaneous input impedance will vary depending upon whether D_1 is forward- or reverse-biased. During the time it is forward-biased (worst-case input impedance), the input impedance is determined by the value of R_1 because the (–) input is a virtual AC ground point during this time. When diode D_1 is reverse-biased, the input impedance is the sum of R_1 and the input impedance of the following stage. As the first value will always be lower, we will compute minimum input impedance as

$$\boxed{Z_{IN}(\min) = R_1 \qquad (7.6)}$$

For the circuit shown in Figure 7.8, the minimum input impedance is simply

$$Z_{IN}(\min) = R_1 = 2.7\ k\Omega$$

Output Impedance. The output impedance also varies depending upon the conduction state of D_1. If diode D_1 is conducting, then the output impedance is nearly the same as the output impedance of the op amp itself, which is a very low value. On the other hand, when D_1 is reverse-biased, the output impedance is equal to the value of R_1. Since this latter value is always higher, we will use it to estimate the output impedance.

$$\boxed{Z_{OUT}(\max) = R_1 \qquad (7.7)}$$

By using this value in the design of subsequent stages, we are assured that the signal will couple faithfully between stages on both alternations. In the case of the circuit shown in Figure 7.8, the maximum output impedance is simply

$$Z_{OUT}(\max) = R_1 = 2.7\ k\Omega$$

7.3.3 Practical Design Techniques

We are now ready to design an ideal biased shunt-clipper circuit similar to the one shown in Figure 7.8. We will design to achieve the following performance goals:

1. Clipping levels	+3 to –3 volts
2. Polarity of clipping	Negative peaks clipped
3. Input frequency	100 hertz to 3 kilohertz
4. Minimum input impedance	8 kilohms

Compute the Reference Voltage Divider. Since the design requires bipolar (±3 volts) clipping levels, we will use a voltage divider like that shown in Figure 7.10. The first step is to select a readily available potentiometer. Its value is not critical, but choices between 1 and 50 kilohms would be typical. If the potentiometer is too small, the power consumption is unnecessarily high. If the value is too high, then the nonideal op amp characteristics become more noticeable. Let us choose a 10-kilohm potentiometer for P_1.

The values of R_2 and R_3 are computed with Ohm's Law. By inspection (Kirchhoff's Voltage Law), we can see that these resistors have 12 (i.e., 15 – 3) volts across them. Additionally, they have the same current flow as P_1. This current is also computed with Ohm's Law by dividing the voltage across P_1 (6 volts) by the value of P_1 (10 kΩ). Combining all of this into equation form gives us

$$R_2 = \frac{P_1(V^+ - V_{CU})}{V_{CU} - V_{CL}} \tag{7.8}$$

where V^+ is the +15-volt source, V_{CU} is the upper clipping level, and V_{CL} is the lower clipping level. Similarly, the equation for R_3 is

$$R_3 = \frac{P_1(V^- - V_{CL})}{V_{CL} - V_{CU}} \tag{7.9}$$

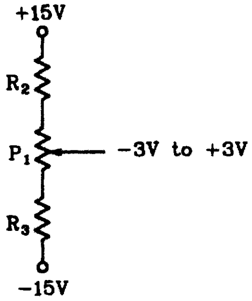


FIGURE 7.10 A voltage divider is used to provide the variable reference voltage.

Applying these equations to our present design gives us the following results:

$$R_2 = \frac{10\ k\Omega(15\ V - 3\ V)}{3\ V - (-3\ V)} = 20\ k\Omega,\ and$$

$$R_3 = \frac{10\ k\Omega[-15\ V - (-3\ V)]}{-3\ V - 3\ V} = 20\ k\Omega$$

Select R_1. The minimum value for R_1 is determined by the minimum required input impedance (8 kΩ in the present case). The upper limit depends on the op amp selected, desired output impedance, and required immunity to nonideal characteristics. It would be unusual to choose R_1 as anything greater than a few tens of kilohms, since the resulting high-output impedance of the circuit would make it difficult to interface. Let us select R_1 as a 9.1-kilohm standard value.

Select the Op Amp. The op amp can be selected by assuming that the amplifier is passing strictly sinusoidal waveforms. Chapter 2 discussed this in more detail, but the primary consideration is op amp slew rate. The required slew rate can be estimated by applying Equation (7.5):

$$\begin{aligned} slew\ rate &= 100 f_{MAX}[+V_{SAT} - V_{REF}(\text{min})] \\ &= 100 \times 3\ kHz(+13\ V - (-3\ V)) \\ &= 4.8\ V/\mu s \end{aligned}$$

This, of course, exceeds the 0.5-volts-per-microsecond rating of the standard 741, but it does fall within the 10-volts-per-microsecond slew rate limit of the MC1741SC. Let us design around this device.

Select D_1. Diode D_1 must have a reverse breakdown voltage that is twice the value of the supply voltage. In the present case, it must withstand 30 volts. The current rating for D_1 is more difficult to determine, since it is partially determined by the input impedance of the circuit being driven by the clipper. As we are dealing with low currents, and as all of the diode current must be supplied by the op amp, it is reasonable to select a diode with a current rating that is greater than the short-circuit op amp current. The manufacturer's data sheet lists the maximum short-circuit current for the MC1741SC as ±35 milliamps.

Many diodes will perform well in this application. Let us select the common 1N914A diode, which should be adequate under any probable circuit conditions.

Compute C_1. Capacitor C_1 helps to ensure that the reference voltage on the (+) input of the op amp remains constant. Its value is not critical and may even be omitted in many applications. A reasonable value can be computed by ensuring that the reactance of C_1 is less than 10 percent of the resistance of the smaller of R_2 or R_3 at the lowest input frequency. In our present case, these resistors are both 20 kilohms, so we compute the value of C_1 by applying the basic equation for capacitive reactance.

$$X_c = \frac{1}{2\pi fC},\ or$$

$$C = \frac{1}{2\pi fX_c}$$

$$C = \frac{1}{6.28 \times 100\ Hz \times 2\ k\Omega}$$

$$= 0.796\ \mu F$$

We will select a standard value of 1.0 microfarad for our circuit.

The completed schematic of our shunt-clipper design is shown in Figure 7.11. The actual performance of the circuit is indicated by the oscilloscope displays in Figure 7.12, and the actual circuit performance is compared with the original design goals in Table 7.2.

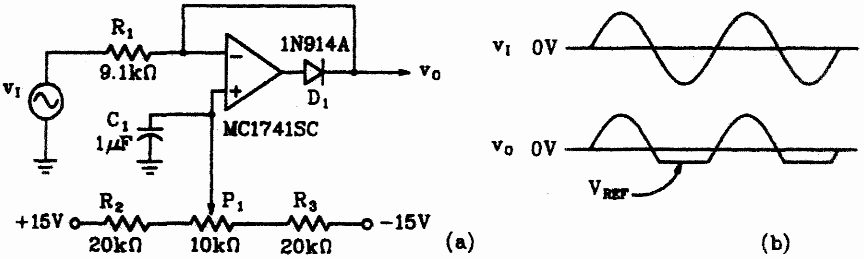
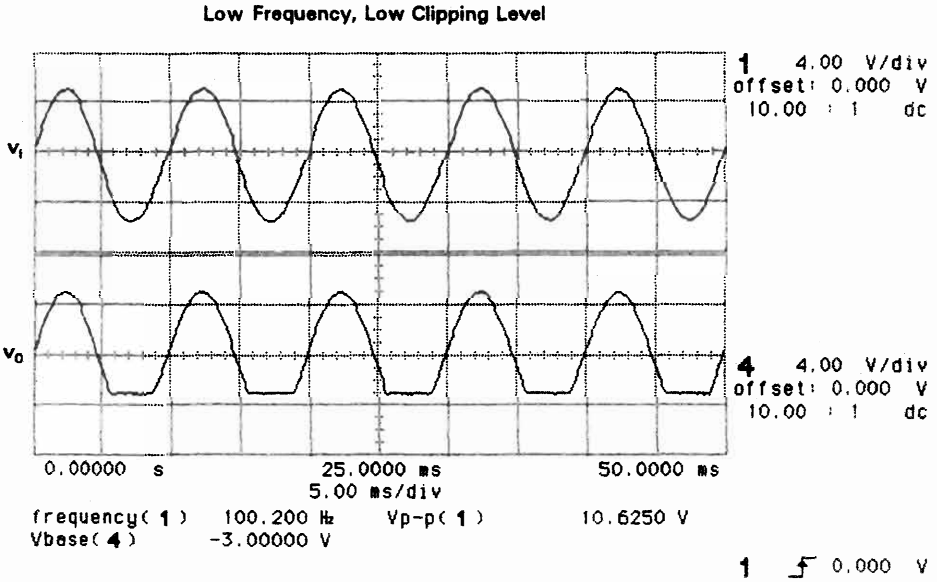

R₁
9.1kΩ
1N914A
v₀
D₁
vᵢ
C₁
1μF
MC1741SC
R₂
P₁
R₃
+15V
−15V
20kΩ
10kΩ
20kΩ
(a)
vᵢ 0V
v₀ 0V
V_REF
(b)

FIGURE 7.11 A biased shunt clipper designed for variable clipping levels.


Low Frequency, Low Clipping Level
vᵢ
v₀

1 4.00 V/div
offset: 0.000 V
10.00 : 1 dc

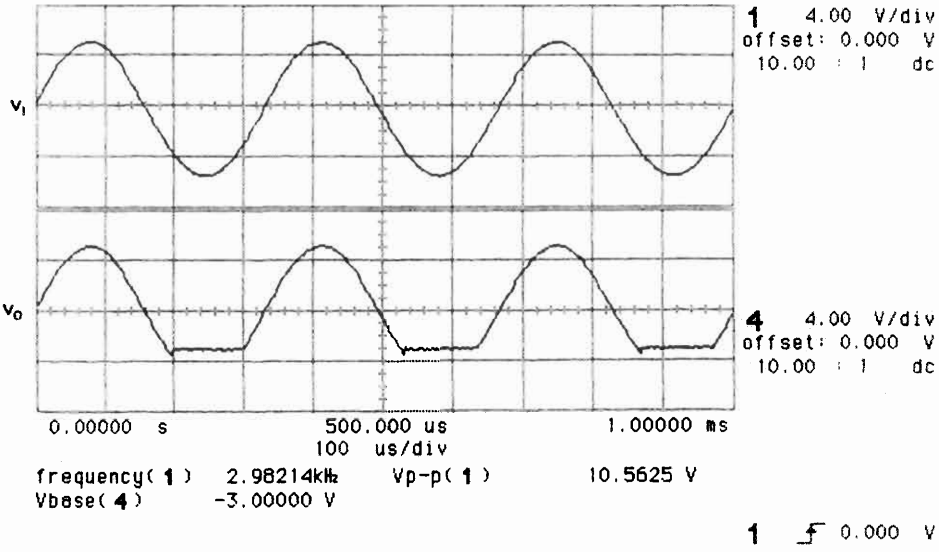
4 4.00 V/div
offset: 0.000 V
10.00 : 1 dc

0.00000 s 25.0000 ms 50.0000 ms
5.00 ms/div
frequency(1) 100.200 Hz Vp-p(1) 10.6250 V
Vbase(4) -3.00000 V

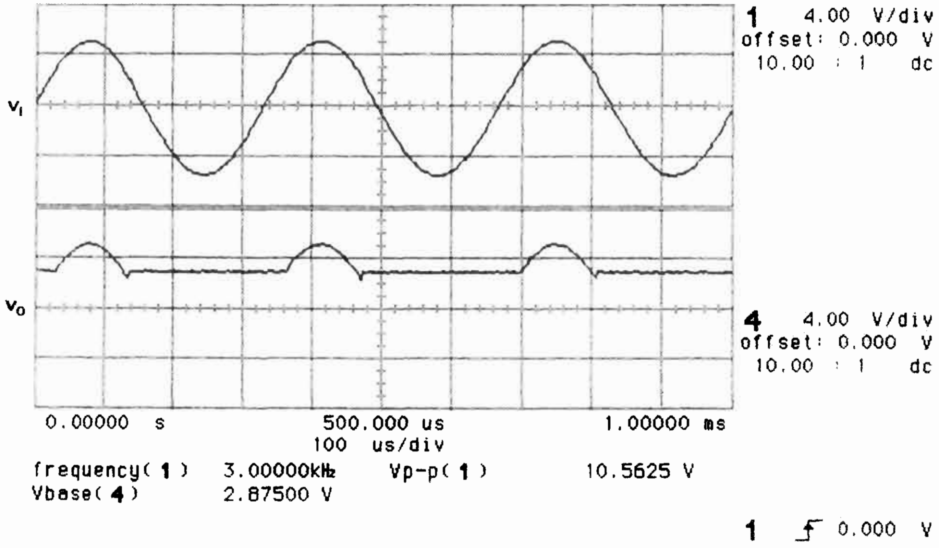
1 ⨍ 0.000 V

(a)

FIGURE 7.12 Oscilloscope displays showing the actual performance of the shunt clipper shown in Figure 7.11. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*

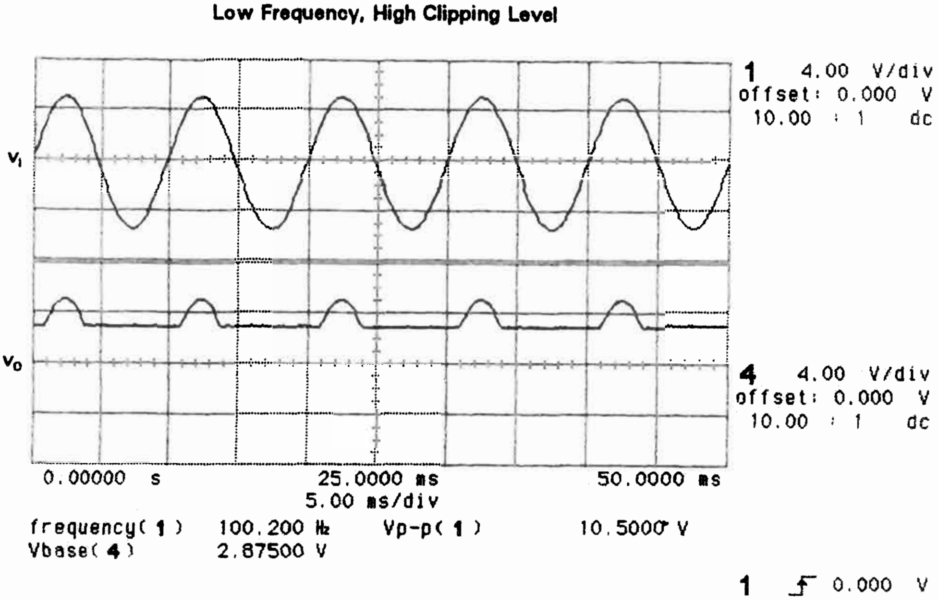

High Frequency, Low Clipping Level

(b)


High Frequency, High Clipping Level

(c)

FIGURE 7.12 *Continued*


Low Frequency, High Clipping Level

(d)

FIGURE 7.12 *Continued*

TABLE 7.2

	Design Goal	*Measured Value*
Clipping levels	–3 volts, +3 volts	–3 volts, +2.875 volts
Input frequency	100 hertz–3 kilohertz	100 hertz–3 kilohertz
Input impedance	≥8 kilohms	≥9.1 kilohms

7.4 IDEAL CLAMPER

Figure 7.13 shows a basic diode clamper circuit. Its purpose is to shift the average or DC level of the input signal without altering the waveshape. Alternatively, an application may require that the peaks of the signal be shifted to some new reference level. In either case, this is accomplished by clamping the peaks of the signal to a fixed reference level. Either positive or negative peaks may be clamped, to either a positive or negative reference level.

The operation of the simple clamper shown in Figure 7.13 is best understood by starting when the input signal is at its negative peak (–10 V). At this instant, the 5-volt reference and the 10-volt source are series aiding. Since the only resistance in the circuit is the forward resistance of the diode, capacitor C_1 quickly charges to 14.3 volts (negative on the left). That is, it charges to the combined voltage of the series-aiding source and reference voltage minus the forward voltage drop across D_1.

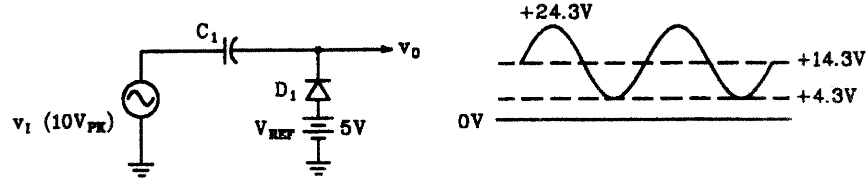


FIGURE 7.13 A simple biased clamper circuit is used to shift the DC or reference level of the input signal.

During all other portions of the input cycle, the diode will be reverse-biased and effectively removed from the circuit. The output waveform, then, is being taken across an open circuit (reverse-biased diode) and will be identical to the "applied" signal. But what is the applied signal? It is now v_I in series with the charge on C_1. Since C_1 has no discharge path, it acts like a battery. Therefore, the output waveform will be the same as the input waveform, but will have a positive 14.3 volts added to it. As the input signal passes through its 0 voltage point, the output signal will be +14.3 volts. When the input is at +10 volts, the output will be at a +24.3-volt level. And when the input returns to the negative peak (–10 volts), the output will be at +4.3 volts. Any charge that has been lost on the capacitor because of leakage will be replaced when the input passes through its negative peak. As indicated by the resulting output waveform in Figure 7.13, the output signal appears to have its negative peaks clamped to the reference voltage (less a diode drop). Also, notice that the DC level of the output is now at +14.3 volts DC. For this reason, the circuit is sometimes called a DC restorer circuit.

If the diode is reversed, the positive peaks will be clamped to the reference voltage. The reference voltage itself can be either positive or negative (even variable).

7.4.1 Operation

The operation of the basic clamper shown in Figure 7.13 relies on the charging of a capacitor through a diode. For low-amplitude signals, the diode drop (0.7 volts) becomes significant. In fact, the circuit cannot be used at all if the peak input signal is below 0.7 volts, since the diode cannot be forward-biased. The circuit shown in Figure 7.14 is called an ideal biased clamper because it performs as though the diode were ideal (i.e., no forward voltage drop). This means that the circuit can be used to clamp signals in the millivolt range.

Let us start our examination of the circuit in Figure 7.14 as the input reaches the negative peak. This will cause the output of the op amp to go in a positive direction and will forward-bias D_1. The diode places a near short circuit around the op amp and essentially converts the circuit into a voltage follower with reference to the (+) input. This means that the output of the op amp will be at approximately the same voltage as the reference voltage (actually 0.7 volts higher). The (–) input of the op amp will also be at the reference voltage level. Capacitor C_2 charges to the difference in potential between v_I and the reference voltage felt on the (–) input of the op amp. This action is similar to that described for the circuit in

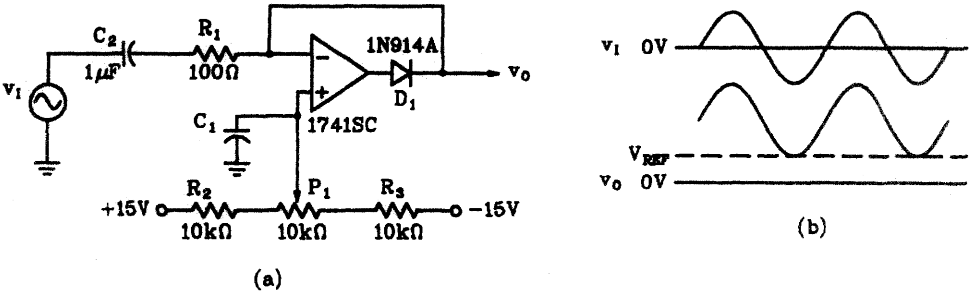


FIGURE 7.14 An ideal biased clamper circuit.

Figure 7.13, but notice the absence of a diode drop. The rate of charge for C_2 is limited by the value of R_1.

For the remainder of the input cycle, the diode is reverse-biased. This effectively disconnects the op amp from the circuit so the output will be the same as the input plus the voltage across C_2. Again, C_2 has no rapid discharge path, so it will act as a DC source and provide the clamping action described previously.

In order for the clamper to be practical, it must drive into a very-high-impedance circuit. For this reason, the clamper circuit shown in Figure 7.14 is nearly always followed by a voltage follower circuit.

7.4.2 Numerical Analysis

For the purpose of numerically analyzing the behavior of the ideal biased clamper circuit shown in Figure 7.14, let us determine the following characteristics:

1. Range of reference voltage adjustment
2. Maximum input voltage
3. Frequency range
4. Input impedance
5. Output impedance

Range of Reference Voltage. Both upper and lower limits for the reference voltage (at the wiper arm of P_1) may be found by applying the basic voltage divider equation. The minimum voltage occurs when P_1 is moved toward the minus 15-volt source and is computed as

$$V_{REF}(\text{min}) = V^- + V_T\left(\frac{R_3}{R_1 + R_2 + P_1}\right)$$

$$= -15\ V + 30\ V\left(\frac{10\ k\Omega}{10\ k\Omega + 10\ k\Omega + 10\ k\Omega}\right)$$

$$= -5\ V$$

The maximum reference voltage is found in a similar manner. That is,

$$\begin{aligned}
V_{REF}(\text{max}) &= V^+ - V_T\left(\frac{R_2}{R_1 + R_2 + P_1}\right) \\
&= +15\ V - 30\ V\left(\frac{10\ k\Omega}{10\ k\Omega + 10\ k\Omega + 10\ k\Omega}\right) \\
&= +5\ V
\end{aligned}$$

Maximum Input Voltage. On the positive peak of the input signal, the (–) input of the op amp will be at a voltage that is higher than v_I(peak) by the amount of charge on C_2. The value of the voltage on the (–) input is equal to the peak-to-peak amplitude of the input signal plus the reference voltage.

The manufacturer's data sheet tells us that the maximum voltage on the (–) input pin of the op amp is equal to the supply voltage (+15 volts). Therefore, the maximum input signal is given as

$$\boxed{v_I(\textit{peak-to-peak}) = V^+ - V_{REF}(\text{max}) \qquad (7.10)}$$

If the diode were reversed, V^- and V_{REF}(min) would be used to calculate the maximum input signal. In our particular circuit, the maximum input signal is computed as

$$v_I(\textit{peak-to-peak}) = 15\ V - 5\ V = 10\ V\ \textit{peak-to-peak, or}$$

$$v_I(RMS) = \frac{10\ V}{2 \times 1.414} = 3.54\ V(RMS)$$

Frequency Range. During the majority of the input cycle, capacitor C_2 is slowly leaking off charge. There are three paths for this discharge current:

1. Op amp bias current for the (–) input
2. Reverse leakage current through D_1
3. Current through the input impedance of the following stage

Since all of these currents are variable with voltage, temperature, frequency, and so on, the computation of a minimum operating frequency is not straightforward. Once the actual current values are known for a particular circuit under a certain set of conditions (presumably worst case), then the lower frequency limit will be determined by the amount of allowable discharge for C_2. That is, C_2 ideally maintains its full charge at all times unless the input signal changes amplitude. If C_2 is allowed to discharge excessively during a cycle, the circuit will begin to clip the negative peaks of the signal, and the output amplitude will begin to drop.

We can obtain a rough estimate of the lower cutoff frequency if we can estimate the effective discharge resistance (R_X) seen by C_2. This can be approximated by finding the parallel resistance of the (–) input, the diode's reverse resistance, and the input resistance of the following stage. All of these values are computed using DC parameters. For our present example, let us assume that the output of the clamper is driving a standard 741 configured as a voltage follower. First, we compute the reverse resistance of the diode. The manufacturer's data sheet indicates that the diode will have about 25 nanoamperes of reverse current with 20 volts applied. From this we can estimate the reverse resistance as

$$R_{D_1} \approx \frac{20\ V}{25\ nA} = 800\ M\Omega$$

The effective DC resistance of the (–) input can be estimated from the bias current data provided by the manufacturer. The data sheet indicates that the bias current will be about 300 nanoamperes (at 0°C). We can assume a worst-case voltage equal to the maximum peak-to-peak input (10 volts in our case). Thus, Ohm's Law will allow us to estimate the effective resistance of the (–) input as

$$R_{(-)} \approx \frac{10\ V}{300\ nA} = 33.3\ M\Omega$$

Finally, the approximate DC resistance of the (+) input of a standard 741 connected as a voltage follower (not shown in Figure 7.14) can be computed. The data sheet indicates a maximum bias current of 800 nanoamperes. Again, we will assume a voltage equal to the highest peak-to-peak input. Our estimate for the input resistance of the follower stage is, then,

$$R_{VF} \approx \frac{10\ V}{1500\ nA} = 6.67\ M\Omega$$

The value of R_X is simply the parallel combination of these three estimated resistances. That is,

$$\begin{aligned} R_X &= R_{D_1} \| R_{(-)} \| R_{VF} \\ &= \frac{1}{\frac{1}{800\ M\Omega} + \frac{1}{33.3\ M\Omega} + \frac{1}{6.67\ M\Omega}} \\ &= 5.5\ M\Omega \end{aligned}$$

Finally, the lower frequency limit of the clamper can be estimated with Equation (7.11).

$$\boxed{f_L = \frac{16.7}{R_X C_2} \qquad (7.11)}$$

This equation is derived by considering the tilt characteristics of a square-wave input. For the circuit being considered, the low-frequency limit is estimated as

$$f_L = \frac{16.7}{R_X C} = \frac{16.7}{5.5\ M\Omega \times 1\ \mu F} = 3\ Hz$$

The high-frequency limit of the circuit shown in Figure 7.14 is not well defined and is dependent on the application. To understand the effects of increasing input frequencies, consider that the input capacitor charges on the negative peak of the input waveform. This occurs when the output of the op amp goes positive and forward-biases diode D_1. As frequency is increased, however, the output of the op amp begins to experience increasing delays. In other words, the action on the output of the op amp occurs **after** the corresponding point on the input. This delay is caused partially by the internal phase shift of the op amp and partially by the effects of slew rate limiting. In any case, the result is that C_2 is charged at some point after the negative peak, which means that it won't be able to fully charge. This effect is evident on the output waveform as a reduction in the average DC level; it becomes worse the higher the input frequency goes.

This effect is clearly illustrated in Figure 7.15. The sinusoidal waveform is the input signal. The second waveform is the actual output pin of the op amp, and the capacitor charges during the uppermost portion of this latter waveform. Figure 7.15(a) shows the circuit response to low-input frequencies (100 Hz). Notice that the capacitor charging time occurs at the negative peak of the input signal. Figure 7.15(b) shows the same circuit with a higher input frequency (100 kHz). The charging point for the capacitor (positive peak on the output waveform) is now delayed and occurs **after** the negative peak of the input.

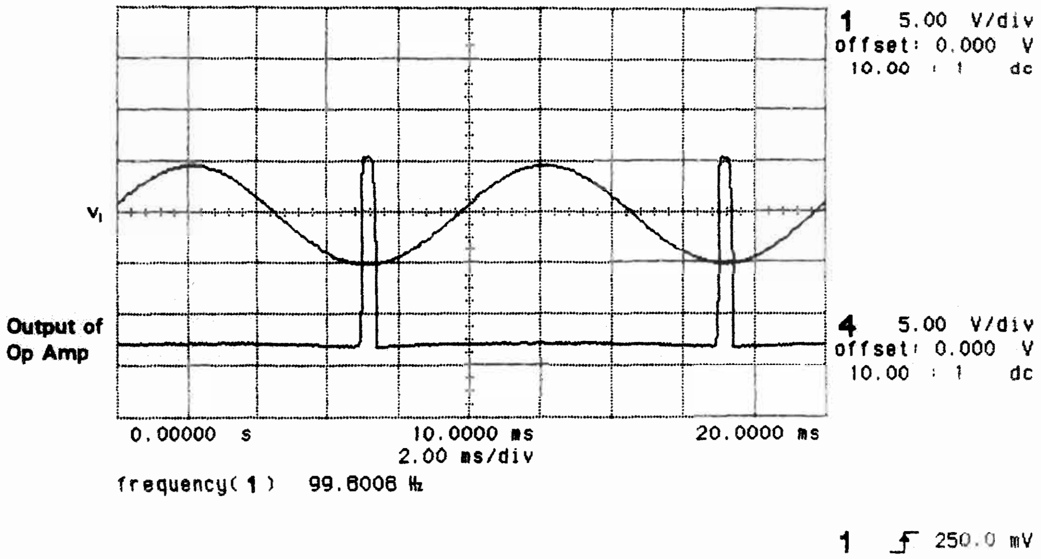
Input Impedance. The input impedance of the circuit varies with the input frequency and with the state of the circuit. As frequency increases, the reactance of C_2 decreases and lowers the input impedance. Additionally, during diode D_1's conduction times, the (–) input of the op amp is essentially an AC ground point; however, during the remainder of the cycle this same point is at a high-impedance level.

For our present analysis, we will consider the absolute minimum input impedance to be equal to the value of R_1.

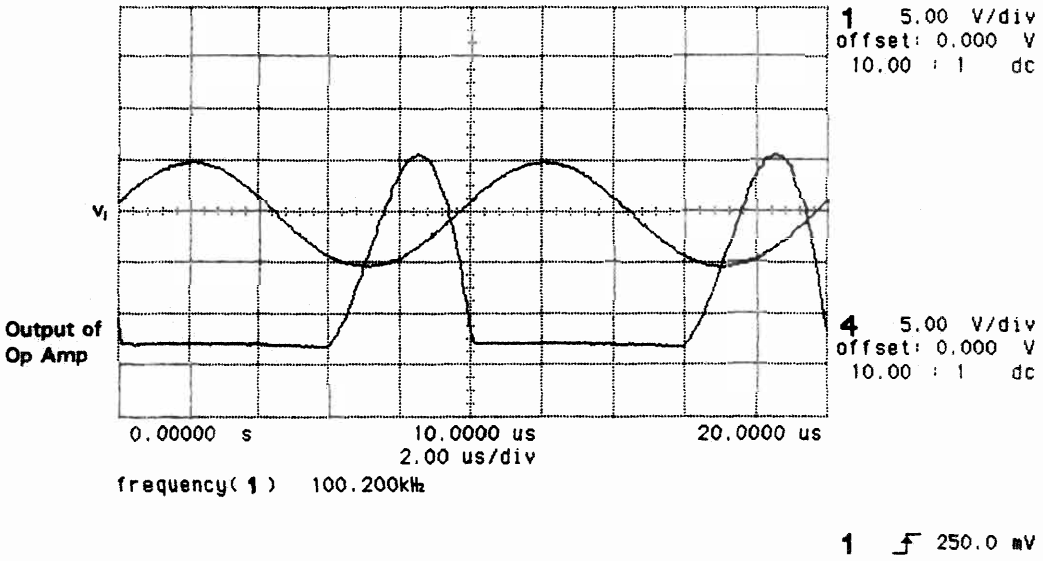
Output Impedance. The output impedance also varies with frequency and state of the circuit. During the charging time of C_2, the output impedance is quite low, but during the remainder of the cycle the impedance is determined by C_2 and R_1. In the present circuit, the maximum output impedance at the lower frequency limit (3 Hz) is approximately

$$Z_O = \sqrt{X_{C2}^2 + R_1^2} = \sqrt{(53.08\ k\Omega)^2 + (100\ \Omega)^2} \approx 53.08\ k\Omega$$

For reliable operation, the circuit must drive into a very high impedance. This requirement is normally met by using a voltage follower buffer immediately after the clamper circuit. In any case, the input impedance of the following stage should be at *least* 10 times the output impedance of the clamper at the lowest input frequency.


Low Frequency

(a)


High Frequency

(b)

FIGURE 7.15 Oscilloscope displays showing the effects of internal delays and slew rate limiting on the operation of the biased clamper circuit. (Test equipment courtesy of Hewlett-Packard Company.)

7.4.3 Practical Design Techniques

Let us now design an ideal biased-clamper circuit that performs according to the following design goals:

1. Minimum input impedance	1.1 kilohms
2. Input voltage range	500 millivolts through 2 volts (peak)
3. Reference levels	–1.0 volt through +2 volts
4. Minimum input frequency	20 hertz

Computation and selection of all components other than C_2 is similar to the methods described previously for the biased shunt clipper and will not be repeated here. The value for capacitor C_2 can be determined by applying Equation (7.11).

$$f_L = \frac{16.7}{R_X C_2}, \text{ or}$$

$$C_2 = \frac{16.7}{R_x f_L}$$

$$= \frac{16.7}{5.5\ M\Omega \times 20\ Hz}$$

$$= 0.152\ \mu F$$

where R_X was computed in a preceding paragraph. We will use a standard 0.15-microfarad capacitor for C_2.

The final design for the ideal biased clamper is shown in Figure 7.16. Its performance is indicated by the oscilloscope displays in Figure 7.17, where Figure 7.17(a) shows the circuit response for a minimum amplitude, minimum frequency input signal, and a minimum reference level. The output signal is just beginning to clip on the negative peaks. If this is critical in a particular application, simply increase the size of C_2. Figure 7.17(b) shows the other extreme—maximum input signal and maximum reference level at a higher frequency (5 kHz). Table 7.3 contrasts the actual measured performance of the circuit with the original design goals.

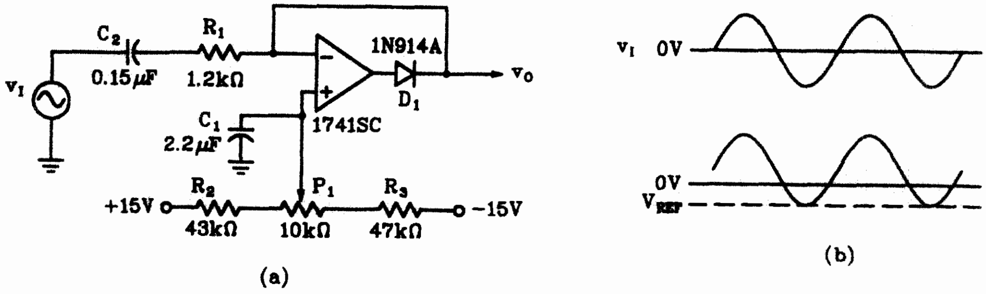
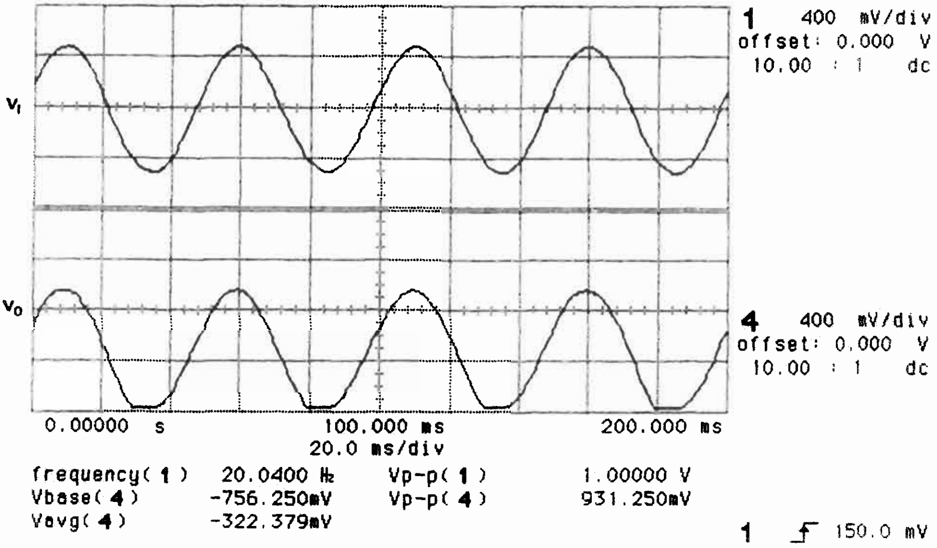


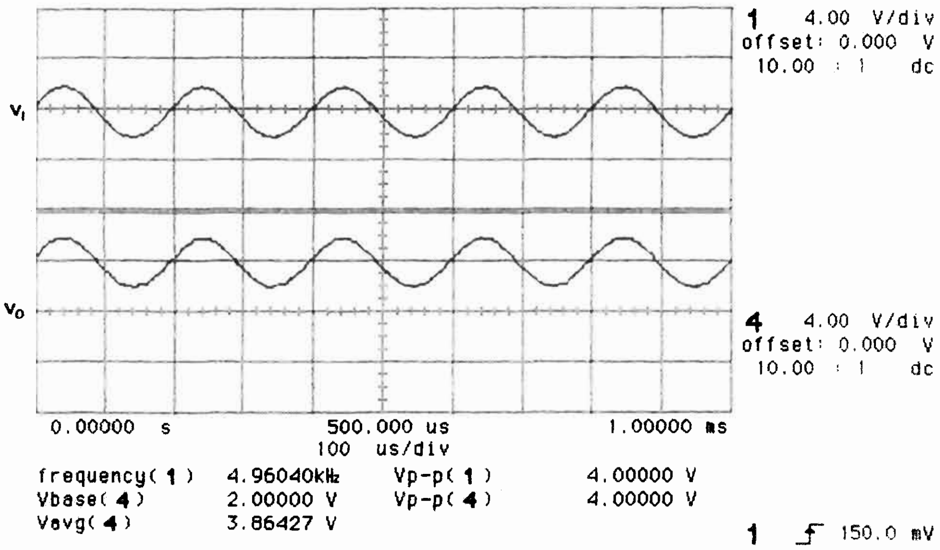
FIGURE 7.16 Final schematic of an ideal biased clamper-circuit design.

Low Input Voltage, Low Frequency, Low Reference



(a)

High Input Voltage, High Frequency, High Reference



(b)

FIGURE 7.17 Oscilloscope displays showing the performance of the clamper circuit shown in Figure 7.16. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 7.3

	Design Goals	*Measured Values*
Minimum input impedance	1.1 kilohms	1.2 kilohms
Input voltage range	500 millivolts–2 volts (peak)	500 millivolts–2 volts (peak)
Reference levels	–1 volt–2 volts (peak)	–0.76 volts–2 volts (peak)
Minimum input frequency	20 hertz	20 hertz

7.5 PEAK DETECTORS

It is often necessary to develop a DC voltage that is equal to the peak amplitude of an AC signal. This technique is used for many applications, including test equipment, ultrasonic alarm systems, and music synthesizers. As with the other circuits presented earlier in this chapter, the peak detector simulates an ideal diode by including it in the feedback loop of an op amp.

7.5.1 Operation

Figure 7.18 shows the schematic diagram of an ideal peak detector circuit. As the dotted lines in the figure indicate, the circuit is essentially an ideal clipper (an inverting clipper was discussed earlier in this chapter), followed by a parallel resistor and capacitor and driving a voltage follower (discussed in Chapter 2). You will recall from the discussion on ideal clippers that the output of the clipper portion of the circuit will be a positive half-wave signal that is equal in amplitude to the peak of the input signal. Because C_1 is connected to this same point, it will be charged to this peak voltage.

The time constant for charging C_1 is very short and primarily consists of C_1 and the forward resistance of the diode. Thus, C_1 charges almost instantly to the peak output of the clipper circuit. When the output of the clipper starts to decrease (as it goes beyond the 90° point), diode D_1 becomes reverse-biased. This essen-

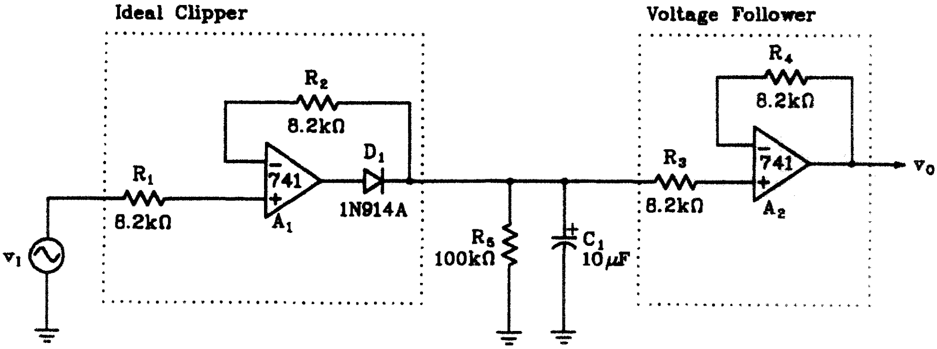


FIGURE 7.18 An ideal peak detector circuit develops a DC output that is equal to the peak input voltage.

tially isolates capacitor C_1 and leaves the charge trapped. The only discharge path for C_1 is through R_5 and via leakage or op amp bias currents. In any case, the time constant is much longer than the charge time constant, so C_1 holds its charge and presents a steady input voltage to A_2 that is equal to the peak amplitude of the input signal. A_2, of course, is simply a buffer amplifier and prevents unintentional discharging of C_1 caused by loading from the following circuit.

Resistor R_5 is the primary discharge path for C_1. If the input signal reduces its average (i.e., long-term) amplitude, then C_1 must be able to discharge to the new peak level. If the R_5C_1 time constant is too short, then the voltage on C_1 will not be constant and will have a high value of ripple. On the other hand, if the R_5C_1 time constant is too long, then the circuit cannot respond quickly to changes in the input amplitude. This characteristic is called fast attack (since C_1 responds quickly to amplitude increases) and slow decay (since C_1 is slow to respond to signal amplitude decreases).

Resistor R_3 limits the current into the (+) input of A_2 when power is disconnected from the circuit. Without this resistor, the input circuitry for A_2 may be damaged as C_1 discharges through it. For capacitors smaller than 1 microfarad, resistor R_3 can normally be omitted. Resistor R_4 is to minimize the effects of bias currents in A_2. As in past circuits, we try to keep the resistance equal for both op amp inputs.

Resistor R_2 limits the current into the (–) input of A_1 when power is removed from the circuit. Again, this current comes from the discharge of C_1. Resistor R_1 is to minimize the effects of bias currents in A_1 and should be the same size as R_2.

7.5.2 Numerical Analysis

The basic numerical analysis of the clipper and buffer amplifier portions of the circuit (both voltage follower circuits) were presented in Chapter 2, and will not be repeated here. Two additional characteristics that we want to analyze are

1. Lower frequency limit
2. Response time

Lower Frequency Limit. The lower frequency limit is the frequency that causes the ripple voltage to exceed the maximum allowable level (determined by the design requirements). It can be estimated by applying the basic discharge equation for capacitors, which is

$$\boxed{f = \frac{1}{R_5C_1 \ln\left[\dfrac{V - V_0}{V - v_C}\right]} \qquad (7.12)}$$

where V_0 is the initial charge of the capacitor (V_{pk}), V is the voltage to which the capacitor will discharge (assumed to be 0), and v_C is the minimum allowable voltage on the capacitor. For this discussion, the lower frequency limit will be considered to be the frequency that causes the ripple voltage across C_1 to be 1 percent of the DC voltage. Having made this definition, we can apply a simplified equation to determine the lower frequency limit:

$$f_L = \frac{100}{R_5 C_1} \tag{7.13}$$

In the case of the circuit in Figure 7.18, we estimate the lower frequency limit as

$$f_L = \frac{100}{100\ k\Omega \times 10\ \mu F} = 100\ Hz$$

Response Time. Response time describes how quickly C_1 can respond to decreases in the amplitude of the input signal. Here again, this can be computed from the basic discharge equation. However, if we assume that the capacitor is charged to peak and discharges toward an eventual value of 0, then we can use the simplified form, Equation (7.14).

$$t_R = R_5 C_1 \ln\left[\frac{v_{PK}(old)}{v_{PK}(new)}\right] \tag{7.14}$$

where $v_{PK}(old)$ is the peak input signal amplitude before the decrease, and $v_{PK}(new)$ is the peak input signal amplitude after the decrease. For example, let us determine how quickly the circuit shown in Figure 7.18 can respond if the input signal drops from 2.5 to 1.2 volts peak. We apply Equation (7.14) as follows:

$$t_R = 100\ k\Omega \times 10\ \mu F \ln\left[\frac{2.5\ V}{1.2\ V}\right] = 734\ ms$$

7.5.3 Practical Design Techniques

Let us now design an ideal peak detector circuit similar to the one shown in Figure 7.18. It should satisfy the following design goals:

1. Input frequency range	300 to 3000 hertz
2. Peak input voltage	1 to 5 volts
3. Response time	≤200 milliseconds
4. Ripple voltage	≤3 percent

Select the Clipper Op Amp. The minimum unity gain bandwidth is the same as the upper input frequency, since A_1 is essentially operated at a closed-loop gain of 1 (when the rectifier conducts).

The minimum slew rate for the op amp is computed by applying Equation (2.11). On the negative alternation of the input cycle, the output of A_1 will go to

$-V_{SAT}$, since D_1 will be reverse-biased and the op amp will be operating with open-loop gain. On the positive alternation, the output may have to go as high as 5.7 volts. That is, v_{PK} of the input plus the forward drop of D_1. Thus, the maximum output swing for purposes of determining the slew rate requirement is +5.7 – (–13) = 18.7 volts. The required slew rate for our present design is computed as

$$f_{SRL} = \frac{slew\ rate}{\pi v_O(\text{max})},\ or$$

$$\begin{aligned} slew\ rate &= \pi f_{SRL} v_O(\text{max}) \\ &= 3.14 \times 3\ kHz \times 18.7\ V \\ &= 0.176\ V/\mu s \end{aligned}$$

Both bandwidth and slew rate requirements are easily satisfied with the standard 741 op amp. Let us choose to use this device.

Select the Buffer Amplifier. The buffer amplifier has even less stringent requirements because it is amplifying a DC signal; therefore, we will not be concerned about bandwidth or slew rate limitations. If the application is critical with regard to DC drift, then we can select an op amp to minimize this characteristic. For the present design, however, let us employ the basic 741 device.

Select D_1. The peak inverse voltage of D_1 will be equal to the difference between $-V_{SAT}$ and the maximum peak input voltage. This difference in potential will exist when C_1 has charged to the maximum peak voltage and the output of A_1 swings to $-V_{SAT}$ on the negative alternation. In equation form, the peak inverse voltage of the diode is determined with Equation (7.15).

$$\boxed{V_{PIV}(rating) \geq V_{PK}(\text{max}) - (-V_{SAT}) \qquad (7.15)}$$

In the case of the circuit being designed, the PIV rating of the diode is computed as

$$V_{PIV} = 5\ V - (-13\ V) = 18\ V$$

The average current for D_1 is nearly negligible, since it only conducts enough to recharge capacitor C_1, and because C_1 loses very little charge between consecutive cycles. The instantaneous current through D_1, however, might be considerably higher when power is first applied to the system and C_1 is being charged initially. The safest practice is to insure that D_1 can survive the short-circuit current of A_1.

For our present design, let us use a 1N914A diode for D_1. This easily meets both the PIV and instantaneous current requirements.

Compute R_5 and C_1. There are two conflicting circuit parameters that affect the choice of values for R_5 and C_1: allowable ripple voltage across C_1 and response time. It is possible to establish values for these parameters in the initial design goals that cannot be physically implemented. In general, a faster response time leads to greater ripple.

For design purposes, we will independently compute the required values for R_5 and C_1 to satisfy the ripple and the response time criteria. We will then make a judgment as to the optimum choice of values.

The *minimum* required RC time constant based on the ripple specification can be found by applying Equation (7.12). (We could use Equation (7.13) if the ripple goal were 1 percent.)

$$f_L = \frac{1}{R_5C_1 \ln\left[\frac{V - V_0}{V - v_C}\right]}, \textit{ or}$$

$$R_5C_1 = \frac{1}{f_L \ln\left[\frac{V - V_O}{V - v_C}\right]}$$

$$= \frac{1}{300\ Hz \times \ln\left[\frac{0 - 5\ V}{0 - 4.85\ V}\right]} = 109.4\ ms$$

Any RC time constant that is longer than this minimum value will satisfy the ripple goal.

The *maximum* R_5C_1 time constant based on the response time design goal can be found by applying Equation (7.14).

$$t_R = R_5C_1 \ln\left[\frac{v_{PK}(old)}{v_{PK}(new)}\right], \textit{ or}$$

$$R_5C_1 = \frac{t_R}{\ln\left[\frac{V_{PK}(old)}{V_{PK}(new)}\right]}$$

$$= \frac{200\ ms}{\ln\left[\frac{5\ V}{1\ V}\right]}$$

$$= 124.3\ ms$$

Any RC time constant that is less than this value will satisfy the response time requirement.

At this point, we must choose values for R_5 and C_1 such that the RC time constant falls within the above window (i.e., 109.4 ms $\leq R_5C_1 \leq$ 124.3 ms). Additionally, we don't want to use resistor values smaller than a few kilohms or larger than the low megohms. In the present case, let us select a standard value of 1.0 microfarad for C_1. The limits for R_5 can then be computed as

$$R_5(\text{min}) = \frac{109.4\ ms}{1\ \mu F} = 109.4\ k\Omega, \textit{ and}$$

$$R_5(\text{max}) = \frac{124.3\ ms}{1\ \mu F} = 124.3\ k\Omega$$

Let us select a standard value of 120 kilohms for R_5.

Compute R_1, R_2, R_3, and R_4. For our purposes, the exact values of these four resistors are noncritical and any value in the range of 2 to 100 kilohms will suffice. It is important, however, that $R_1 = R_2$ and that $R_3 = R_4$. Let us arbitrarily choose all four resistors to be 10 kilohms.

This completes the design of our ideal peak detector circuit. The final schematic is shown in Figure 7.19. The waveforms that indicate its performance are presented in Figure 7.20. Figures 7.20(a) and 7.20(b) show the output response for minimum and maximum input conditions. Figure 7.20(c) illustrates the ripple volt-

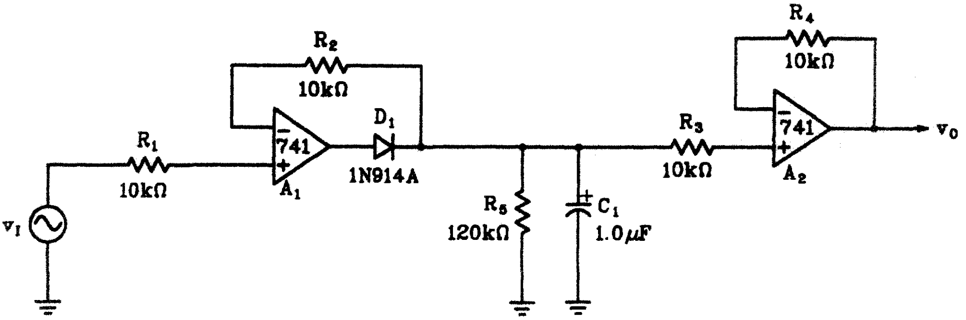
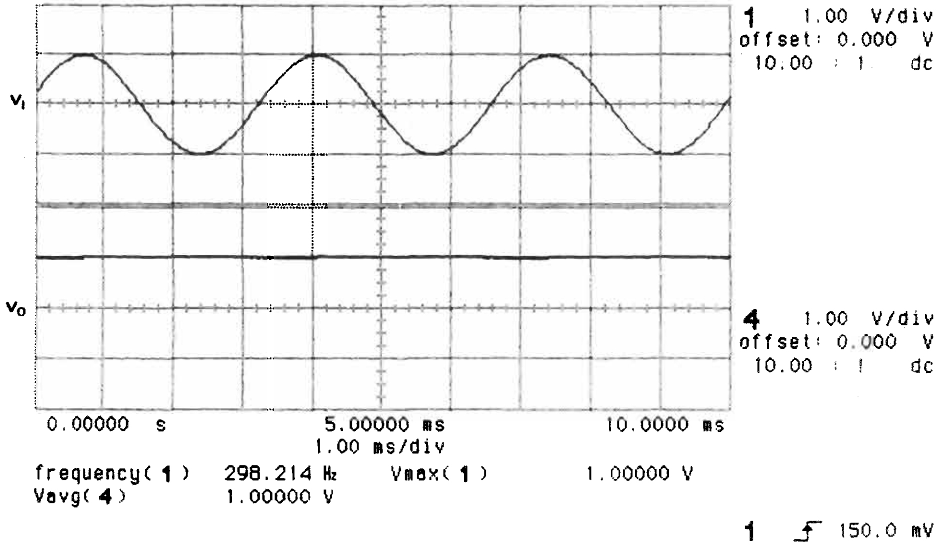


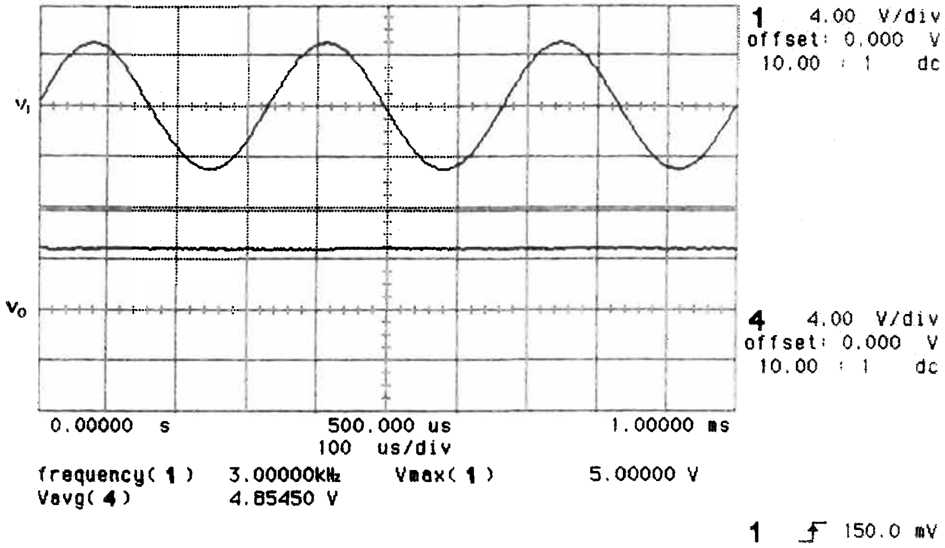
FIGURE 7.19 Final design of an ideal peak detector circuit.

Low Input Voltage, Low Frequency



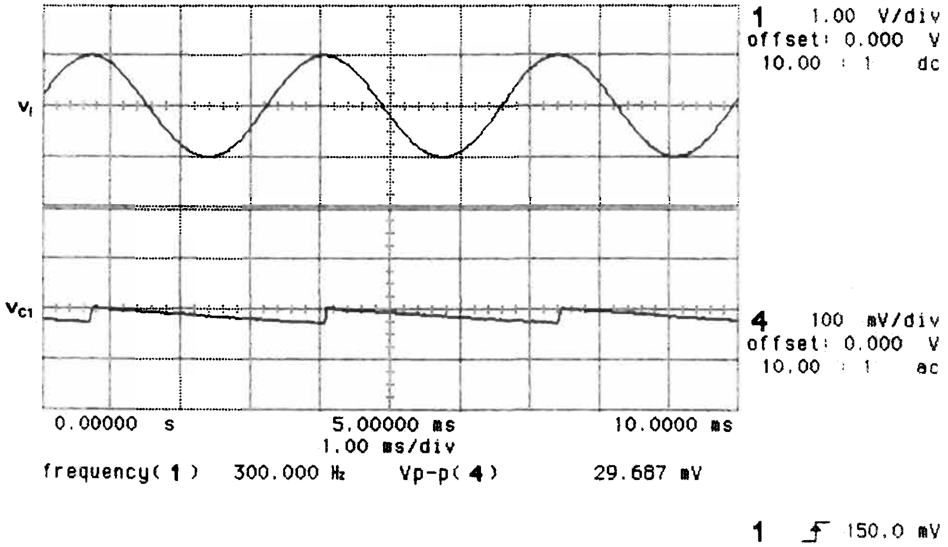
(a)

FIGURE 7.20 Oscilloscope displays showing the actual performance of the peak detector circuit shown in Figure 7.19. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*



High Input Voltage, High Frequency

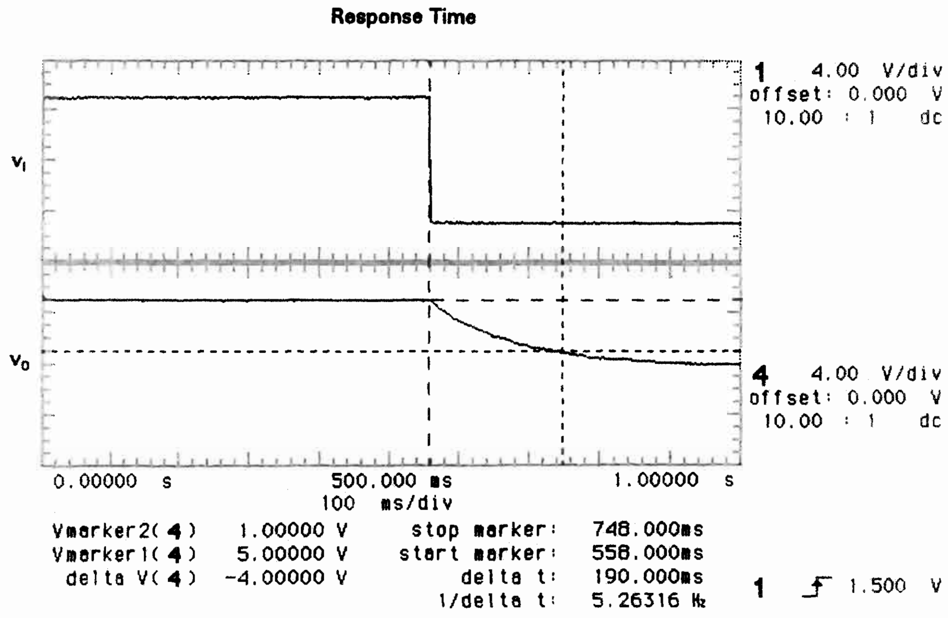
(b)



C1 Ripple Voltage

(c)

FIGURE 7.20 *Continued*



(d)

FIGURE 7.20 *Continued*

age across C_1, and the response time is measured in Figure 7.20(d)—here a square-wave input is applied and the time for the capacitor to discharge from 5 to 1 volt is measured. The design goals are compared with the measured results in Table 7.4.

TABLE 7.4

	Design Goal	*Measured Value*
Input voltage	1–5 volts peak	1–5 volts peak
Frequency range	300–3000 hertz	300–3000 hertz
Ripple voltage	≤3 percent	2.97 percent
Response time	≤200 milliseconds	190 milliseconds

7.6 INTEGRATOR

The integrator is one of the fundamental circuits studied in basic electronics. Its op amp counterpart is also an important circuit for many signal processing applications. As you may recall, an integrator produces an output voltage that is proportional to *both* the duration and amplitude of an input signal. For example, if the input were a pulse waveform, then the output would be a voltage that was proportional to the amplitude and pulse width of the input signal. In essence, the integrator computes the area (height × width) of the input signal. This corresponds to the mathematical operation in calculus called *integration*.

The integrator may also alter the shape of the input waveform. For example, a square wave will be converted to a triangular wave in the process of being integrated. When integrated, a triangle wave will produce a parabolic waveform that very closely approximates a sinewave. In the case of a sinewave input, the output will still be sinusoidal but may be shifted in phase and reduced in amplitude. For sinewave inputs, the integrator acts as a simple low-pass filter.

7.6.1 Operation

Figure 7.21 shows the schematic of an op amp integrator circuit. If you mentally open capacitor C_1 (which is open for DC signals, anyway), you will see that the circuit is a simple inverting amplifier circuit. Resistors R_2 and R_1 determine the voltage gain of the circuit, and resistor R_3 is to minimize the effects of bias current. Recall that the (–) input of the op amp is a virtual ground point.

Now suppose that a step voltage is applied to the input terminal. This will cause a current to flow through resistor R_1. Since the current flowing in or out of the (–) input is negligible, we will assume that all of the current flowing through R_1 continues through R_2 and C_1. Now, the voltage across R_2 and C_1 can only increase as fast as capacitor C_1 can take on a charge. When the input voltage first makes a change in amplitude, the current resulting from this voltage change is routed **entirely** through C_1. (Since the voltage across R_2 does not change instantly, neither can the current.) As the capacitor accumulates a charge, the current through R_2 begins to change. The circuit, however, is designed to ensure that the current through R_2 is never allowed to be a substantial part of the capacitor current. As long as the input voltage is constant, the capacitor current is constant. As long as the input returns to its original state before the capacitor has had time to accumulate excessive voltage, this discussion is valid.

With a constant current through the capacitor, we will generate a linear ramp of voltage across it (and therefore at the output of the op amp). With a square-wave input, the capacitor will periodically charge and discharge with equal, but opposite polarity, currents. This, of course, produces a triangle wave at the output.

Resistor R_2 is included in the circuit to reduce the gain at low frequencies (DC in particular). Without R_2, the bias currents (small as they are) would eventually charge C_1 and cause an undesired DC offset in the output. This offset may even cause the amplifier to go into saturation. In terms of AC circuit theory, we

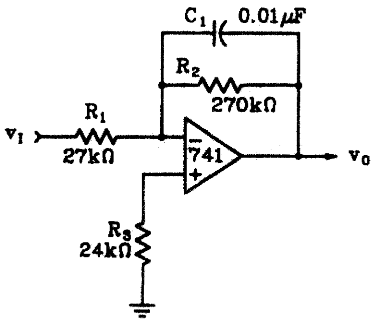


FIGURE 7.21 A basic op amp integrator circuit.

ensure that the reactance of C_1 is less than 10 percent of the value of R_2 at the lowest frequency of operation. This makes certain that the majority of the current will be used to charge and discharge C_1.

7.6.2 Numerical Analysis

Let us analyze the circuit shown in Figure 7.21 and determine the following circuit characteristics:

1. Lowest frequency of operation
2. Highest frequency of operation

Many other characteristics (e.g., input and output impedance) are analyzed in the same way as a simple inverting amplifier (Chapter 2).

Lowest Frequency of Operation. The lower frequency limit of the integrator circuit shown in Figure 7.21 is the frequency that causes the capacitive reactance of C_1 to be equal to one-tenth of R_2. This is computed with the basic capacitive reactance equation.

$$X_C = \frac{1}{2\pi f C}, \ or$$

$$\begin{aligned} f &= \frac{1}{2\pi C X_C} \\ &= \frac{1}{6.28 \times 0.01\ \mu F \times 27\ k\Omega} \\ &= 590\ Hz \end{aligned}$$

This is not an ultimate limit, however. As the frequency is reduced below this value, the operation of the circuit becomes progressively less like an integrator and more like an inverting amplifier. Finally, at DC, it is an inverting amplifier.

Highest Frequency of Operation. The upper frequency limit is dependent on the characteristics of the op amp. In particular, the upper operating frequency will be the lower of the frequencies that are established by the bandwidth or slew rate of the op amp. Both of these considerations were discussed in greater detail in Chapter 2. For many applications, however (including worst-case design consideration), the upper limit will be set by the slew rate of the op amp. This is computed with Equation (2.11) as

$$\begin{aligned} f_{SRL} &= \frac{slew\ rate}{\pi v_O(\text{max})} \\ &= \frac{0.5\ V/\mu s}{3.14 \times 26\ V} \\ &= 6.12\ kHz \end{aligned}$$

7.6.3 Practical Design Techniques

We will now design an op amp integrator that will perform according to the following design goals:

1. Input frequency	300 hertz to 20 kilohertz
2. Input impedance	≥1000 ohms
3. Input voltage	2 to 6.5 volts peak

Select the Op Amp. The first criteria for op amp selection is the upper frequency limit. That is, both slew rate and bandwidth considerations must allow the circuit to operate at the upper frequency specified in the design goals. Unless the circuit is specifically designed to handle small-amplitude signals, it will be the slew rate that limits the upper frequency of operation. In the present case, we will determine the required op amp slew rate by applying Equation (2.11).

$$f_{SRL} = \frac{\textit{slew rate}}{\pi v_O(\text{max})}, \textit{ or}$$

$$\begin{aligned} \textit{slew rate} &= f_{SRL}\pi v_O(\text{max}) \\ &= 20\ kHz \times 3.14 \times 26\ V \\ &= 1.63\ V/\mu s \end{aligned}$$

This exceeds the 0.5-volts-per-microsecond slew rate of the standard 741, but it is well within the capabilities of the MC1741SC.

Another op amp characteristic generally considered in op amp integrator design is the bias current. In general, the lower the frequency of operation, the more problems caused by bias currents. If very low frequencies of operation are needed, it is wise to select an op amp that has particularly low bias currents. For purposes of the present design, however, let us opt to use the MC1741SC device.

Compute R_1. It is important that the input current to the circuit be much greater than the op amp bias current. Let us choose the input current to be at least 1000 times the worst-case bias current. The manufacturer's data sheet lists the maximum bias current as 800 nanoamperes. Thus, we will establish our input current at 1000 × 800 nanoamperes, or 800 microamperes.

We can now compute the value of R_1 using Ohm's Law.

$$R_1 = \frac{2\ V}{800\ \mu A} = 2.5\ k\Omega$$

As long as this value exceeds the minimum input impedance requirement, then it may be used as calculated. Otherwise, it should be increased to satisfy the impedance requirements. If a substantial increase is needed in order to establish the correct input impedance, an op amp with a lower bias current should be selected and R_1 recalculated. For our design, let us use a standard 2.4-kilohm resistor for R_1.

Compute C_1. The basic electronics equations for charge ($Q = CV$ and $Q = It$) can be set equal to each other and manipulated to give us our equation, Equation (7.16), for C_1.

$$C_1 = \frac{i_I}{2V_{SAT}f_L} \tag{7.16}$$

where f_L is the lowest input frequency and i_I is the *maximum* input current. The maximum input current is computed with Ohm's Law as

$$i_I(\text{max}) = \frac{v_I(\text{max})}{R_1} = \frac{6.5\ V}{2.4\ k\Omega} = 2.7\ mA$$

For our current design, we compute C_1 as

$$C_1 = \frac{2.7\ mA}{2 \times 13\ V \times 300\ Hz} = 0.346\ \mu F$$

We will use a standard 0.33-microfarad capacitor for C_1. A low-leakage type of capacitor should be chosen.

Compute R_2. Resistor R_2 is chosen to have a resistance of at *least* 10 times the capacitive reactance of C_1 at the lowest input frequency. We simply apply the basic capacitive reactance equation to compute R_2.

$$R_2 = \frac{10}{2\pi f C_1} = \frac{10}{6.28 \times 300\ Hz \times 0.33\ \mu F} = 16\ k\Omega$$

Compute R_3. Resistor R_3 is computed as the parallel combination of R_1 and R_2. That is,

$$R_3 = R_1 \| R_2 = \frac{1}{\frac{1}{2.4\ k\Omega} + \frac{1}{16\ k\Omega}} \approx 2\ k\Omega$$

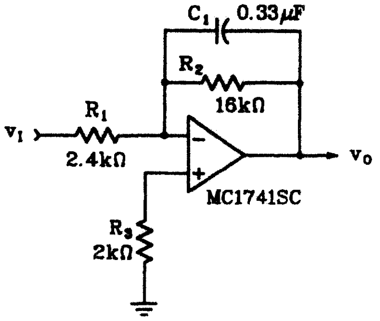
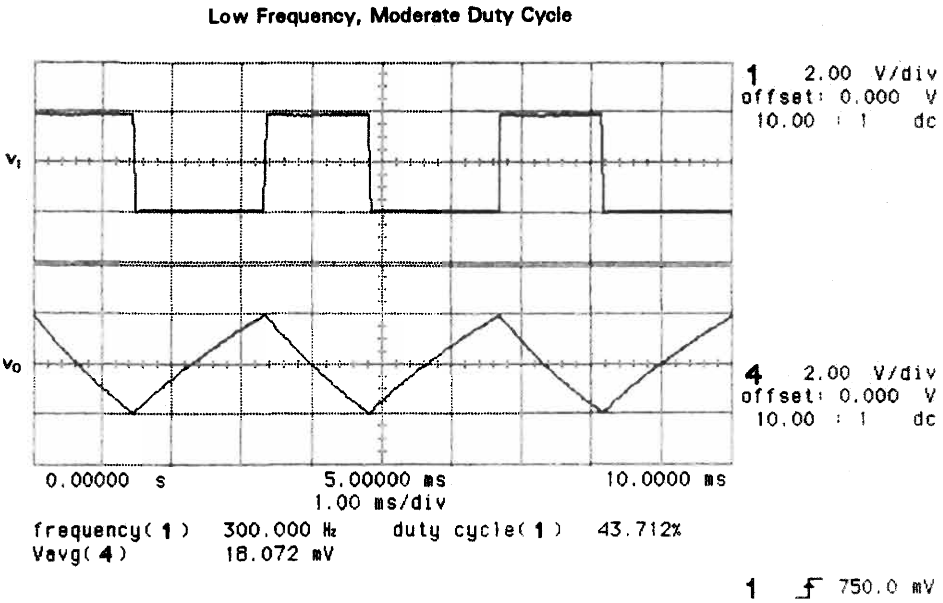
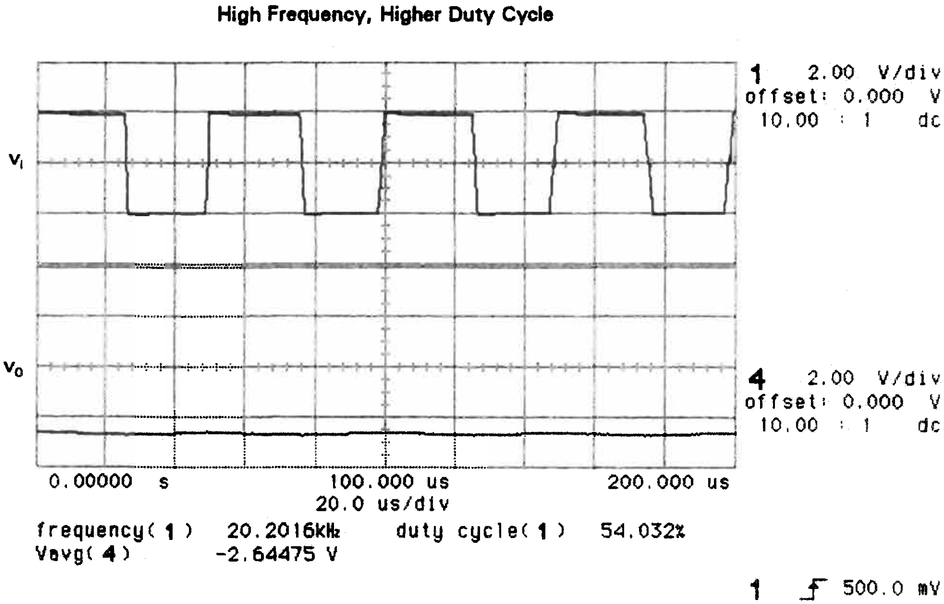


FIGURE 7.22 Final schematic of an integrator circuit design.



```
1   2.00  V/div
offset: 0.000  V
 10.00  : 1    dc

4   2.00  V/div
offset: 0.000  V
 10.00  : 1    dc

frequency( 1 )   300.000 Hz    duty cycle( 1 )   43.712%
Vavg( 4 )        18.072 mV

1   ⌐ 750.0 mV
```

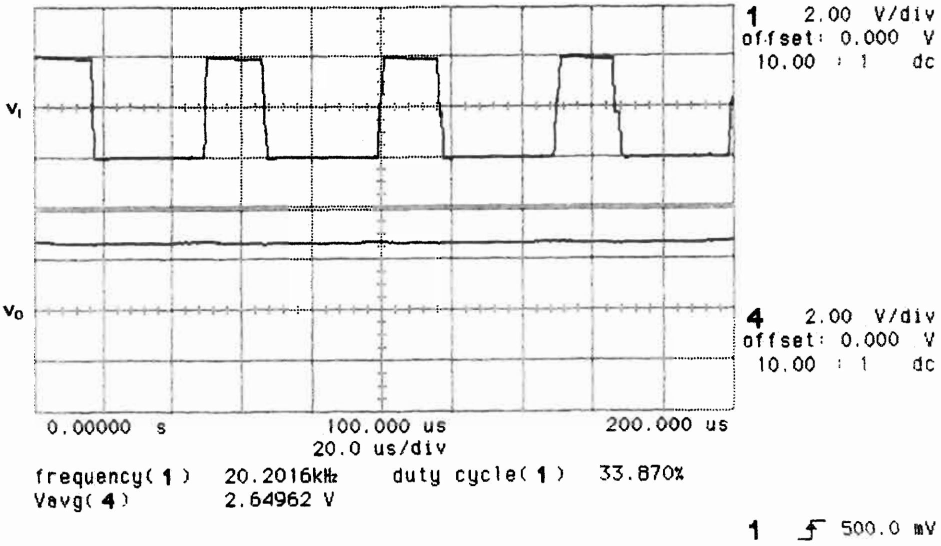
(a)



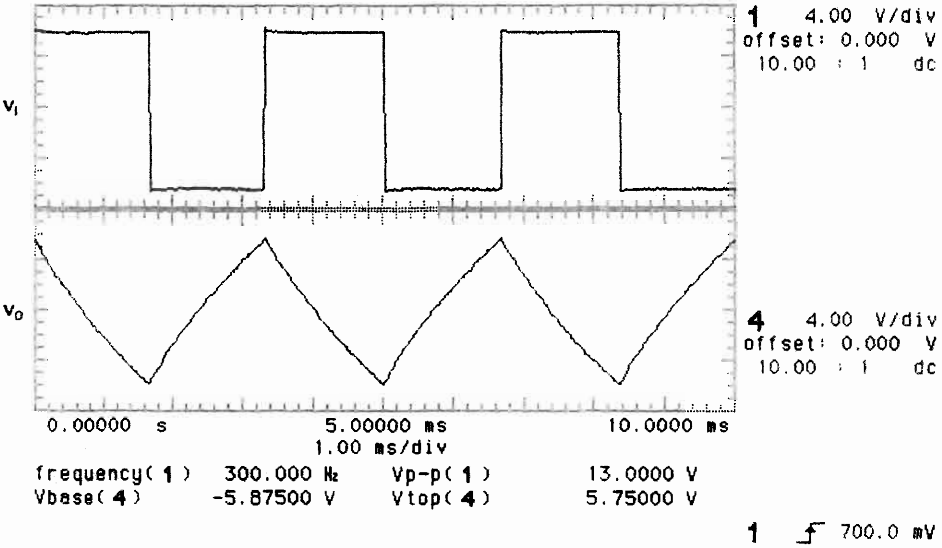
```
1   2.00  V/div
offset: 0.000  V
 10.00  : 1    dc

4   2.00  V/div
offset: 0.000  V
 10.00  : 1    dc

frequency( 1 )  20.2016kHz    duty cycle( 1 )  54.032%
Vavg( 4 )       -2.64475 V

1   ⌐ 500.0 mV
```

(b)

FIGURE 7.23 Oscilloscope displays showing the performance of the integrator circuit shown in Figure 7.22. (Test equipment courtesy of Hewlett-Packard Company.)


High Frequency, Lower Duty Cycle

(c)


High Input Voltage, Low Frequency

(d)

FIGURE 7.23 *Continued*

The completed integrator design is shown in Figure 7.22, and the circuit waveforms are presented in Figure 7.23. Figure 7.23(a) shows the response of the circuit at 300 hertz; notice the linearity of the ramp waveform. Figures 7.23(b) and 7.23(c) show the circuit response to 20-kilohertz signals. The integrator action has essentially eliminated the observable waveform, but comparison of Figures 7.23(a) to 7.23(c) will clearly show the circuit's response to changes in duty cycle. Figure 7.23(d) illustrates the circuit's response to a 6.5-volt peak input signal.

7.7 DIFFERENTIATOR

The differentiator is another fundamental electronic circuit and is the inverse of the integrator circuit. In terms of mathematics, it produces an output signal that is the first derivative of the input signal. In more intuitive terms, the instantaneous output voltage is proportional to the instantaneous rate of change of input voltage. If, for example, we apply a linear ramp voltage to the input of a differentiator, we will expect the output to be a DC level since the rate of change of input voltage is a constant value. Similarly, if we apply a sine wave to the differentiator, the output will also be sinusoidal in shape but will be shifted in phase by approximately 90 degrees since the maximum rate of change of a sine wave occurs as it passes through the 0° and 180° points.

7.7.1 Operation

Figure 7.24 shows the schematic diagram of an op amp differentiator circuit. From basic electronics, we know that the current through a capacitor is directly proportional to the rate of change of applied voltage. This is evident from the equation for capacitive current.

$$i_C = C\frac{\Delta v}{\Delta t} = C\frac{dv}{dt}$$

It is also evident from the capacitive reactance equation—

$$X_C = \frac{1}{2\pi fC}$$

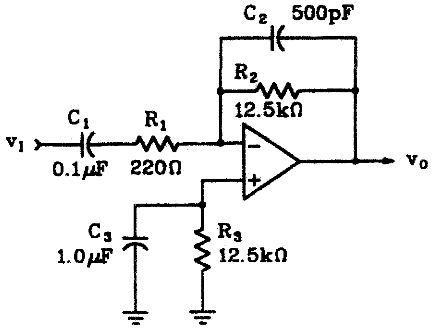


FIGURE 7.24 A differentiator produces an output voltage that is proportional to the rate of change of input voltage (i.e., $v_{o(t)} = k(dv/dt)$).

which shows that the opposition to current flow decreases as the frequency (rate of change of voltage) increases. In the case of the circuit shown in Figure 7.24, we can expect capacitor C_1 to have greater currents for input voltages that *change* levels more quickly. Any current that flows through the capacitor must also flow through R_1 because of the series connection. Since no significant current flows in or out of the (–) input, we can conclude that the current through R_2 will also be the same as the input current and will be proportional to the rate of change of input voltage. The left end of R_2 is connected to a virtual ground point; therefore, the voltage across it is the output voltage of the op amp and is determined by the rate of change of input voltage.

The differentiator circuit is inherently unstable and prone to oscillation because the input impedance decreases with increasing frequency. Recall that the gain for an inverting op amp is determined by the ratio of the impedance in the feedback path to the input impedance. Since the input impedance decreases with frequency, it will cause the gain to increase at high frequencies. Even though the actual input signal frequency may be relatively low, there are always high-frequency noise signals present. If the gain were allowed to increase excessively at high frequencies, these noise signals would interfere with the desired output and could cause oscillation in the circuit. To prevent this gain, we include capacitor C_2 in the feedback path. This capacitor tends to bypass resistor R_2 at noise frequencies, thus reducing the circuit gain and improving the circuit stability. Additionally, resistor R_1 works to increase the stability by ensuring that the input impedance has a practical minimum limit regardless of the frequency.

Resistor R_3 reduces the effects of the op amp bias current. As with previous circuits, we make R_3 equal to R_2 so that the DC resistance in both op amp terminals is the same. Capacitor C_3 simply bypasses R_3 at high frequencies, which further minimizes the circuit's response to noise frequencies.

7.7.2 Numerical Analysis

Since the output voltage of a differentiator circuit is determined by the rate of change of input voltage, we want to know the maximum rate of change of input voltage that can be applied to the circuit without driving the circuit into saturation. We can estimate this rate by applying Equation (7.17).

$$\frac{\Delta v_I}{\Delta t} = \frac{V_{SAT}}{R_2 C_1} \tag{7.17}$$

For the circuit shown in Figure 7.24, we estimate the maximum rate of change of input voltage as

$$\frac{\Delta v_I}{\Delta t} = \frac{13\ V}{12.5\ k\Omega \times 0.1\ \mu F} = 10.4\ V/ms$$

The input impedance is a rather complex issue because it varies with frequency and is affected by several components. Nevertheless, the absolute minimum impedance is established by R_1. In practice, the actual minimum impedance may never go as low as that but it is a good approximation for worst-case analysis.

The output impedance increases with frequency, but can still be estimated as described in Chapter 2 for inverting amplifiers.

7.7.3 Practical Design Techniques

We will now design a differentiator circuit that will satisfy the following design goals:

1. Input waveform	Triangle (dual ramp)
2. Input voltage	±2 volts
3. Input frequency	2 kilohertz
4. Output voltage	±10 volts for the given input signal
5. Op amp	741

Compute R_2. Resistor R_2 is selected to establish the basic range of operation. A good rule of thumb for the initial selection of R_2 is given by Equation (7.18).

$$R_2 = \frac{25v_O^+(\text{max})}{I_{SC}} \tag{7.18}$$

where $v_o^+(\text{max})$ is the highest expected output voltage and I_{SC} is the short-circuit current rating of the op amp. For our present design, we compute R_2 as

$$R_2 = \frac{25 \times 10\ V}{20\ mA} = 12.5\ k\Omega$$

We will select the nearest standard value of 12 kilohms.

Compute C_1. The time constant for R_2C_1 is determined by the expected rate of change of input voltage as compared to the resulting output voltage. In equation form, we can compute the value of C_1 as

$$C_1 = \frac{v_O^+(\text{max})\Delta t}{R_2 \Delta v_I} \tag{7.19}$$

Utilization of this equation requires us to know the rate of change of input voltage. The design specifications tell us that we will have a ramp voltage that goes from −2 volts to +2 volts and back at a frequency of 2 kilohertz. Thus, the Δv_I is 4 volts (i.e., −2V to +2V), and the Δt is one half of the period (t) of one input cycle. That is,

$$\Delta t = \frac{t}{2} = \frac{1}{2f} = \frac{1}{2\ kHz} = 250\ \mu s$$

We can now compute C_1 with Equation (7.19) as

$$C_1 = \frac{10\ V \times 250\ \mu s}{12\ k\Omega \times 4\ V} = 0.052\ \mu F$$

Let us plan to use a standard 0.05-microfarad capacitor for C_1.

Compute R_1. Resistor R_1 should equal the reactance of C_1 at a frequency higher than the normal operating frequency. In this way, R_1 has minimal effect for the normal input signal but becomes effective for higher frequencies (noise). We can compute a reasonable value for R_1 with Equation (7.20).

$$R_1 = \sqrt{\frac{R_2}{\pi C_1 f_{UG}}} \tag{7.20}$$

where f_{UG} is the unity gain frequency of the op amp. For the present application, we can compute the value of R_1 as follows.

$$R_1 = \sqrt{\frac{12\ k\Omega}{3.14 \times 0.05\ \mu F \times 1\ MHz}} = 276.5\ \Omega$$

We will use the nearest standard value of 270 ohms.

Compute R_3. Resistor R_3 is always equal to R_2 in order to maintain equal DC resistances in both of the op amp input terminals. Therefore, R_3 will also be a 12-kilohm resistor.

Compute C_3. The reactance of capacitor C_3 should be less than one-tenth the resistance of R_3 at a frequency that causes the reactance of C_1 to be equal to the resistance of R_2. This ensures that resistor R_3 will be effectively bypassed for all usable circuit frequencies. Since $R_2 = R_3$, we can express this in equation form as

$$C_3 = 10C_1 \tag{7.21}$$

In our present circuit, we require a value of

$$C_3 = 10 \times 0.05\ \mu F = 0.5\ \mu F$$

We will use a standard value of 0.47 microfarad for C_3.

Compute C_2. In order to reduce the gain at high-noise frequencies and yet minimize the effect on normal circuit frequencies, we want to select capacitor C_2 such that its reactance is equal to R_2 at a frequency well above the highest normal operating level but well below the unity gain frequency of the op amp. The following equation will provide a reasonable value for C_2.

$$C_2 = \sqrt{\frac{C_1}{8\pi R_2 f_{UG}}} \tag{7.22}$$

Substituting values for our present circuit gives us

$$C_2 = \sqrt{\frac{0.05\ \mu F}{8 \times 3.14 \times 12\ k\Omega \times 1\ MHz}} = 407\ pF$$

We will use the nearest standard value of 390 picofarads for C_2.

This completes the design of our differentiator circuit. The final schematic is shown in Figure 7.25. The oscilloscope display in Figure 7.26(a) shows the actual performance of the circuit under the conditions described in the original design goal, and Figure 7.26(b) shows the circuit performance for a square-wave input signal. Since the rise and fall times are significantly faster than the ramp specified in the design goal, the input amplitude has to be much lower to avoid saturating the output. Notice that during periods when the input signal is steady (i.e., *not changing states*) the output is 0. Finally, Table 7.5 compares the original design goal with the measured performance.

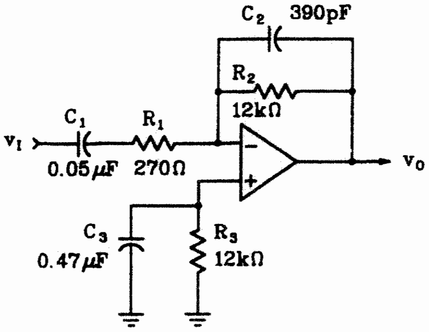
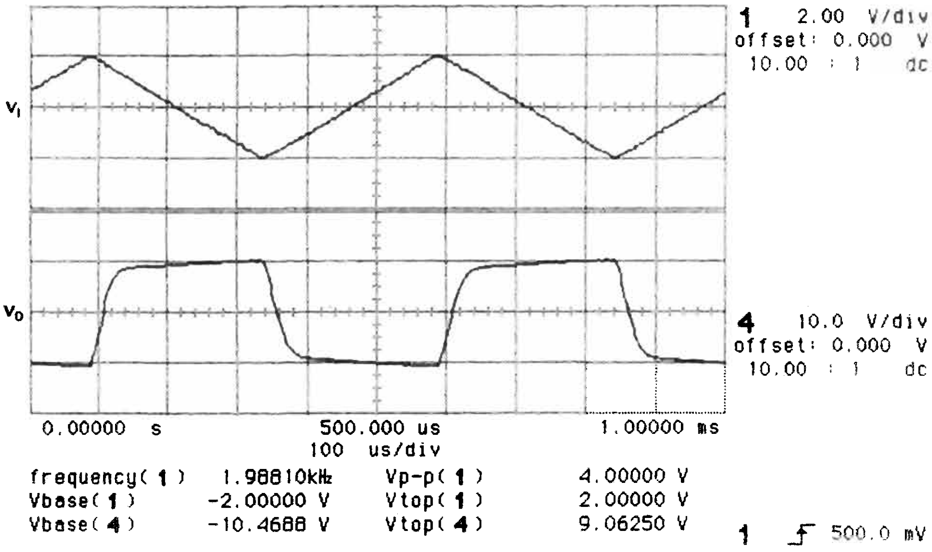


FIGURE 7.25 A differentiator circuit designed to produce a ±10-volt output for a 16-volt-per-millisecond input.

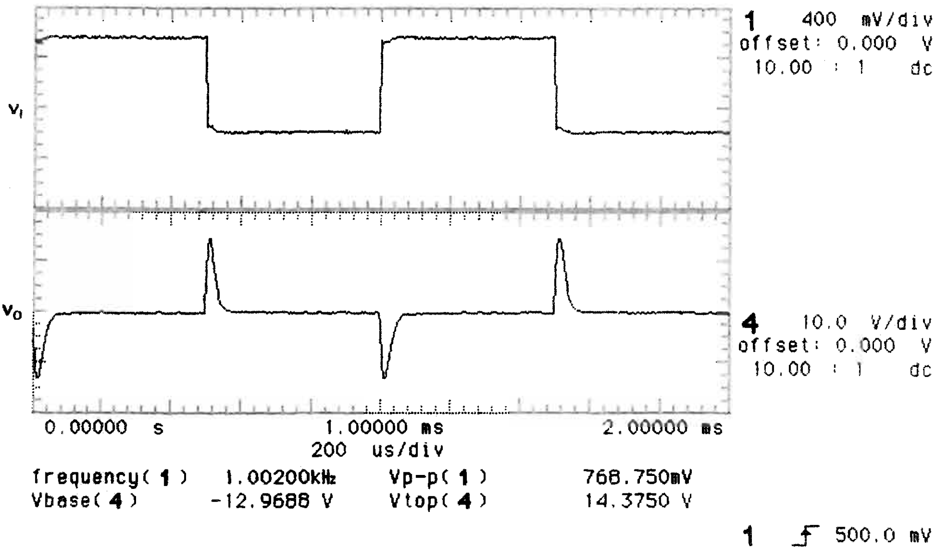
TABLE 7.5

	Design Goal	*Measured Value*
Input frequency	2.0 kilohertz	2.0 kilohertz
Input voltage	±2 volts	±2 volts
Output voltage	±10 volts	–10.5 volts, +9.1 volts


Design Conditions

```
1     2.00  V/div
offset: 0.000  V
 10.00  : 1    dc

4     10.0  V/div
offset: 0.000  V
 10.00  : 1    dc

0.00000  s            500.000 us          1.00000 ms
                      100  us/div
frequency( 1 )  1.98810kHz   Vp-p( 1 )    4.00000 V
Vbase( 1 )      -2.00000 V   Vtop( 1 )    2.00000 V
Vbase( 4 )      -10.4688 V   Vtop( 4 )    9.06250 V       1  _f¯ 500.0 mV
```

(a)


Squarewave Response

```
1     400  mV/div
offset: 0.000  V
 10.00  : 1    dc

4     10.0  V/div
offset: 0.000  V
 10.00  : 1    dc

0.00000  s            1.00000 ms          2.00000 ms
                      200  us/div
frequency( 1 )  1.00200kHz   Vp-p( 1 )    768.750mV
Vbase( 4 )      -12.9688 V   Vtop( 4 )    14.3750 V

                                                      1  _f¯ 500.0 mV
```

(b)

FIGURE 7.26 Oscilloscope displays showing the performance of the differentiator circuit shown in Figure 7.25. (Test equipment courtesy of Hewlett-Packard Company.)

7.8 TROUBLESHOOTING TIPS FOR SIGNAL PROCESSING CIRCUITS

Many of the troubleshooting procedures discussed with reference to basic amplifiers (Chapter 2) are applicable to the signal processing circuits discussed in this chapter. A few additional techniques, however, may help isolate problems more quickly.

If the input connection to any of the circuits presented in Chapter 7 is connected directly to ground, then the output should go to its *normal* DC level. The normal value, of course, depends on the circuit being considered. In any case, if the output does go to the correct DC value with no input signal, then the problem is most likely caused by a defect in one of the AC branches. An AC branch will contain a series capacitor.

If the DC level on the output is abnormal when the input is shorted to ground, then apply the basic analytical techniques described in Chapter 2. When the DC output level is incorrect, more often than not the output will be saturated. Comparison of the polarity of the differential input voltage of the op amp with the output polarity will quickly reveal a defective op amp.

If you suspect an open, 2-terminal component, you can momentarily parallel the suspected part with a known good one while monitoring the output. If the problem is corrected, you have located the defect.

REVIEW QUESTIONS

1. What is the name of the signal processing circuit that is used to shift the DC level of the input signal without altering its waveshape?
2. Refer to Figure 7.2. In your own words, explain why the output waveform for the silicon diode is a constant 0 volts.
3. Refer to Figure 7.3. What is the effect on circuit operation if diode D_1 opens?
4. Refer to Figure 7.3. What is the effect on circuit operation if resistor R_1 decreases in value?
5. Refer to Figure 7.5. While monitoring the output waveform on an AC-coupled oscilloscope, you momentarily short resistor R_4. Describe the effects, if any, that are noted on the oscilloscope display.
6. Refer to Figure 7.5. Describe the effect on output waveshape if resistor R_3 is increased to 45 kilohms.
7. Refer to Figure 7.8. What is the effect on output waveshape if resistor R_2 is increased in value?
8. Refer to Figure 7.8. What is the effect on circuit operation if capacitor C_1 develops a short circuit?
9. Refer to Figure 7.16. Describe the effect on output waveshape if resistor R_3 is increased in value.
10. Refer to Figure 7.19. Describe the effect on circuit operation if resistor R_3 is changed to 4.7 kilohms.

CHAPTER EIGHT

Digital-to-Analog and Analog-to-Digital Conversion

The world of electronics can be neatly divided into two general classes based on the nature of the signal or circuit: digital and analog. Digital signals, devices, and circuits operate in one of two states at all times. These states may be high/low, on/off, up/down, 0 volts/5 volts, –5 milliamps/+5 milliamps, or any other set of two-valued terms.

Analog signals, devices, and circuits, on the other hand, operate on a continuous range with an infinite number of values represented within a given range. An analog voltage, for example, may be 1.5 volts or 1.6 volts, but it can also be an infinite number of values between these two numbers, such as 1.55 volts or 1.590754 volts.

A technician or engineer generally must be capable of working with both analog and digital devices and systems. This text will avoid revealing a prejudice toward one type or another, and the reader is encouraged to avoid developing such a prejudice. It is true that digital devices and techniques are steadily taking over operations and functions previously implemented by analog systems. But equally true is the fact that the world in which we live is inherently analog. Temperature, pressure, weight, speed, light intensity and color, volume, and all other similar quantities are analog in that they vary continuously and have an infinite number of possible values.

This chapter will focus on the circuits that interface analog with digital systems. Analog-to-digital (A/D) converters accept an analog signal at their input and produce a corresponding digital signal at the output. This output can then be processed and interpreted by a digital circuit (typically a microprocessor system). A digital-to-analog (D/A) converter, on the other hand, is used to convert the digital output from a microprocessor or other digital device into an equivalent analog signal. The analog signal is frequently used to control a real-world quantity (e.g., temperature or pressure).

The intent of this chapter, then, is to provide the reader with the concepts and terminology associated with A/D and D/A conversion. Additionally, several representative circuits will be presented that utilize operational amplifiers. An understanding of the operation of these fundamental circuits is important because they convey essential underlying principles. The actual implementation of the converter circuits, however, is another matter. Except for unique or very demanding applications (neither of which is targeted by this text), most A/D and D/A converter applications are resolved by an integrated circuit version of the A/D or D/A converter. The price and performance of these circuits makes them very difficult to beat by designing your own.

8.1 D/A AND A/D CONVERSION FUNDAMENTALS

The concepts and terminology presented in this chapter are important to the reader whether designing a custom converter circuit or selecting an integrated version. In either case, the technician or engineer must be able to effectively evaluate the application and contrast it with the specifications of the converter circuit.

8.1.1 Analog-to-Digital Converters

Figure 8.1 illustrates the fundamental function of A/D conversion. The block labeled "A/D Converter" may be an integrated circuit or an array of op amps and other devices. In any case, it accepts the analog signal as its input and produces a corresponding digital output. The digital output is shown to consist of several lines, the number of which varies with the *resolution* of the converter. Resolution describes the percentage of input voltage change required to cause a step change in the output. Table 8.1 shows the basic relationship between number of bits (lines) and equivalent resolution.

Suppose, for example, an 8-bit A/D converter was designed to accept 0-volt to 10-volt input signals. The 10-volt range would be divided into 256 discrete steps of 10/256, or about 39 millivolts per step. By contrast, a 4-bit A/D converter would have less resolution, with each of the 16 output steps being equivalent to 6.25 percent of the full-scale input, or 625 millivolts. Thus, the higher the resolution (i.e., the number of bits in the converted output), the smaller the input change required to move to the next output step. Typical applications require resolutions of 8, 12, or 20 bits.

Since the analog input may take on any one of an infinite number of values but the output must be resolved into a fixed number of discrete levels or steps, each output step inherently represents a range of input voltages. The process of forming discrete groups from the continuous input is called *quantization*, so the output does not **exactly** represent a given input value; rather, it represents an

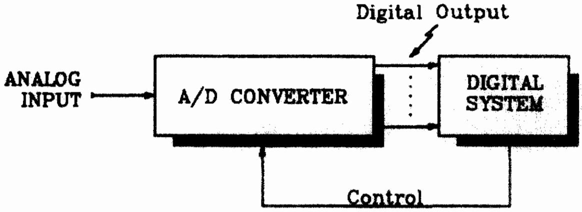


FIGURE 8.1 Analog-to-digital conversion makes an analog signal compatible with a digital system.

TABLE 8.1

Resolution in Bits	*Number of Steps*	*Resolution as Percent of Full Scale (%)*
1	2	50
2	4	25
3	8	12.5
4	16	6.25
5	32	3.125
6	64	1.5625
7	128	0.78125
8	256	0.390625

approximation. The resulting error is called *quantization uncertainty* and is equal to ±½ the value of the least significant bit of the converted output. In the example of the 8-bit converter described, this equates to an uncertainty of ±½ × 39 millivolts, or about ±19.5 millivolts. The magnitude of the quantization uncertainty is less with greater resolution. Therefore, if we need less quantization error, we must increase the number of bits in the output.

When the input signal is converted to a digital output, we normally expect that steadily increasing values of input will produce equally spaced digital values in the output. Sometimes, however, the output may skip one or more steps or digital numbers. Similarly, the output may remain on a given step throughout a range that ideally includes two or more steps. This type of performance is generally caused by *linearity errors*. If the converter has no linearity problems, then the amount of input change to produce a change in the output will be consistent throughout the entire range of operation. When the amount of input change needed to reach the next step in the output varies, we call this variation nonlinearity.

Another characteristic of A/D converters describes the polarity of output changes when a steadily increasing input is applied. With an increasing input signal, we expect (and want) a series of digital numbers in the output that are progressively larger. It is possible, however, for a particular output step to be smaller than the preceding step. That is, the magnitude of the digital output decreases rather than increases on a particular step. This type of output response is called *nonmonotonic*. That is, a converter whose output is progressively higher for progressively higher inputs has the property of *monotonicity*.

Sometimes the intended range of input signals does not match the actual range. For example, the converter may be designed to accept a 0-volt to 10-volt input, but the actual device may be found to produce a maximum digital output for a 9.7-volt input. This discrepancy in full-scale operation is called *gain error* or *scaling error*.

The entire operational range of the A/D converter can be shifted up or down. For example, it may be designed to produce a minimum digital output with 0 volts on the input; however, actual measurement may reveal that a DC offset voltage must be applied at the input in order to produce the minimum digital output. This is called the *offset error* and is often expressed as a percentage of full-scale input voltage.

Accuracy is a term used to describe the overall performance of an A/D converter. It includes the combined effects of all errors and measures the worst-case deviation from a given input signal and the equivalent value of its converted digital output.

The amount of time required to generate a particular digital number to represent a given analog input signal is called *conversion time.* Alternately, the number of these conversions that can be accomplished in one second is called *conversion rate.*

8.1.2 Preamplifiers

Many A/D converter applications involve the conversion of transducer signals into corresponding digital numbers for subsequent processing by a microprocessor or programmable logic controller (PLC). Transducer signals are frequently very low level (current or voltage) and require amplification before they can be effectively applied to an A/D converter. Operational amplifiers are often used for this purpose, as are special differential amplifiers called *instrumentation amplifiers.* Instrumentation amplifiers offer a very high rejection to common-mode signals (e.g., 60 Hz hum picked up on long cables), but offer high amplification to differential-mode signals (e.g., the actual transducer signal). These devices are discussed in greater detail in Chapter 11. Figure 8.2 shows the position of the preamplifier with respect to the A/D converter.

8.1.3 Sample-and-Hold Circuits

As mentioned previously, the conversion of an analog signal into an equivalent digital number requires a certain amount of time (conversion time). Since the analog signal may be changing values **during** the conversion process, substantial errors may be introduced. To eliminate this problem, we introduce a sample-and-hold (S/H) circuit between the preamplifier and the A/D converter. Figure 8.3 shows a block diagram for this case.

An S/H circuit is similar to the peak detector circuit presented in Chapter 7, but it is gated on and off. When the S/H circuit receives the *track* command, it follows (i.e., samples) the input voltage. When a *hold* command is received, the S/H circuit opens its link to the input signal and holds the most recently sampled value at its output. This output is held constant throughout the conversion time of the

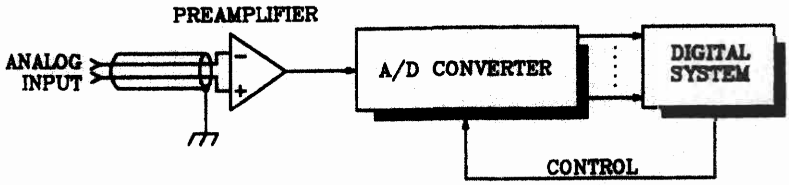


FIGURE 8.2 A preamplifier is used to boost low-level transducer signals to a level that is usable by the A/D converter. These amplifiers are frequently operated as differential amplifiers to reject common-mode noise.

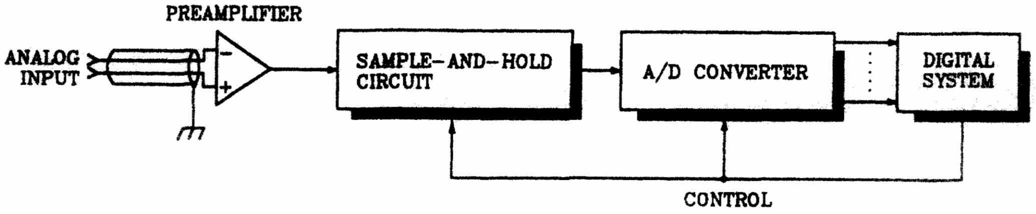


FIGURE 8.3 A sample-and-hold circuit is used to provide a steady input for the A/D conversion circuit.

A/D converter. Once the conversion has been completed, the track command is issued and the cycle repeats.

Once the track command has been received by the S/H circuit, it takes a certain amount of time for the output to match the present level of analog input. This delay is called the *acquisition time*. Similarly, there is a delay between the issuance of a hold command and the actual disconnecting of the S/H circuit from the input signal. This delay is called the *aperture time*.

The sampled input voltage is held constant by utilizing the charge on a capacitor. Although the capacitor has a very low discharge current, it does eventually leak off, causing the S/H output to slowly decay or decrease. The rate at which this occurs is called the *droop rate*.

The more often a signal is sampled, the better the digital representation of the analog signal. If the input signal changes rapidly relative to the speed of the conversion process, then substantial portions of the input signal will be missed (i.e., will go undetected). As an **absolute** minimum, the input signal must be sampled twice during each cycle. That is, the sampling rate must be at *least* twice the highest frequency component present in the input signal. While this may sound like a serious limitation, the use of a sample-and-hold circuit actually extends the highest usable frequency of an A/D converter by several thousand times.

Sample-and-hold circuits are available in integrated form. The AD386 is a sample-and-hold amplifier manufactured by Analog Devices, Inc., that offers a 3.6-microsecond acquisition time, a 12-nanosecond aperture time, and a 20-millivolt-per-second droop rate.

8.1.4 Multiplexers

Many systems have several analog inputs that are monitored by a single computer or digital system. Each of these signals must be converted before the computer can process the signal. Since the A/D conversion circuitry can be quite expensive (relative to other subsystems), many designers opt to multiplex several analog inputs through a single A/D converter circuit. This technique is illustrated in Figure 8.4.

The multiplexer acts like a rotary switch that connects each of the analog inputs to the S/H circuit on a one-at-a-time basis. The position and timing of the "switch" are controlled by the computer or digital system. There should be total isolation between the channels of a multiplexer circuit, but sometimes signal voltages from one channel will couple into another channel (generally via stray or internal capacitance). The resulting interference is called *crosstalk*.

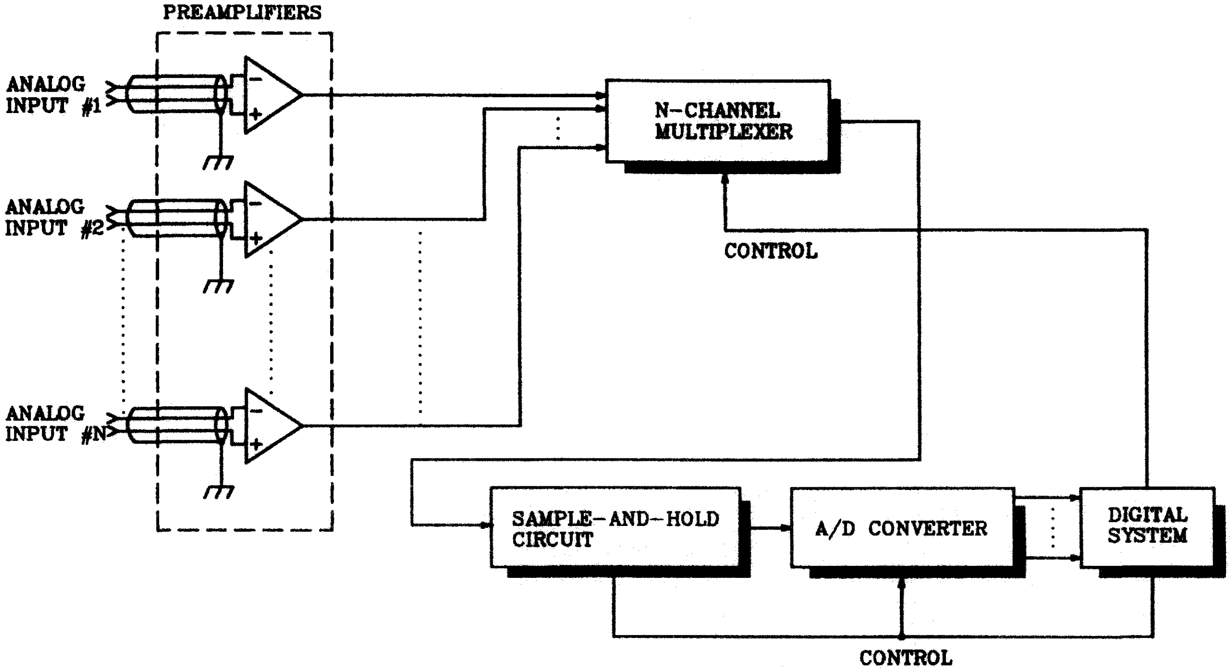

PREAMPLIFIERS
ANALOG INPUT #1
ANALOG INPUT #2
ANALOG INPUT #N
N-CHANNEL MULTIPLEXER
CONTROL
SAMPLE-AND-HOLD CIRCUIT
A/D CONVERTER
DIGITAL SYSTEM
CONTROL

FIGURE 8.4 A multiplexer is used to route several analog inputs through a single A/D conversion circuit.

This approach to system design can make it possible to use higher-performance (i.e., more expensive) sample-and-hold and A/D converter circuits by requiring only one such circuit for multiple inputs.

Multiplexers are available as integrated circuits. The AD7506 manufactured by Analog Devices, Inc., is a 16-channel device designed to select 1 of 16 analog input signals and connect it through to a single analog output.

8.1.5 Digital-to-Analog Converters

Figure 8.5 shows the basic configuration for digital-to-analog (D/A) conversion. The digital system (frequently a microprocessor) computes the required value of analog signal and outputs an equivalent digital number. The D/A converter circuit then converts this digital number into an analog voltage or current for use by the external analog device.

Since the input to the D/A converter has a finite number of digital combinations, the resulting analog output also has a limited number of possible values (unlike pure analog signals, which may have an infinite number of values). The greater the number of possible values, the closer the analog output will be to the ideal value. The number of possible levels is determined by the number of lines or bits in the digital number. More specifically, the number of states is computed as 2^N where N is the number of bits in the digital number. For example, an 8-bit D/A converter could be expected to produce 2^8, or 256, discrete output steps. If the full-scale range of the converter is 0 to 10 volts, then each step will be 10/256, or about 39 millivolts. If finer resolution is required, we need more bits in the digital number. Thus, a converter with 10-bit resolution would provide 2^{10}, or 1024, steps with each step being equivalent to 10/1024, or about 9.8 millivolts.

Accuracy of a D/A converter describes the amount of error between the actual output of the converter and the theoretical output for a given input number. This rating inherently includes several other sources of error.

A certain amount of time is required for the output of a D/A converter to be correct once a particular digital number has been applied at the input. Two major factors cause this delay. First, it takes time for the changes to pass through the converter circuitry; this is called *propagation time*. Second, the output of the D/A converter has a maximum rate of change called *slew rate*, which is identical to the slew rate problems discussed with reference to op amps. The delays caused by slew rate limiting and propagation time are collectively referred to as *settling time*—the total time required for the analog output to stabilize after a new digital number has been applied to the input.

The overall operating range of a D/A converter can be shifted up or down from the optimum point. This DC offset is called *offset error*. In a somewhat similar

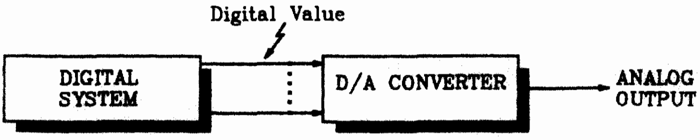


FIGURE 8.5 A digital-to-analog converter is used to make a digital signal (number) compatible with an analog system.

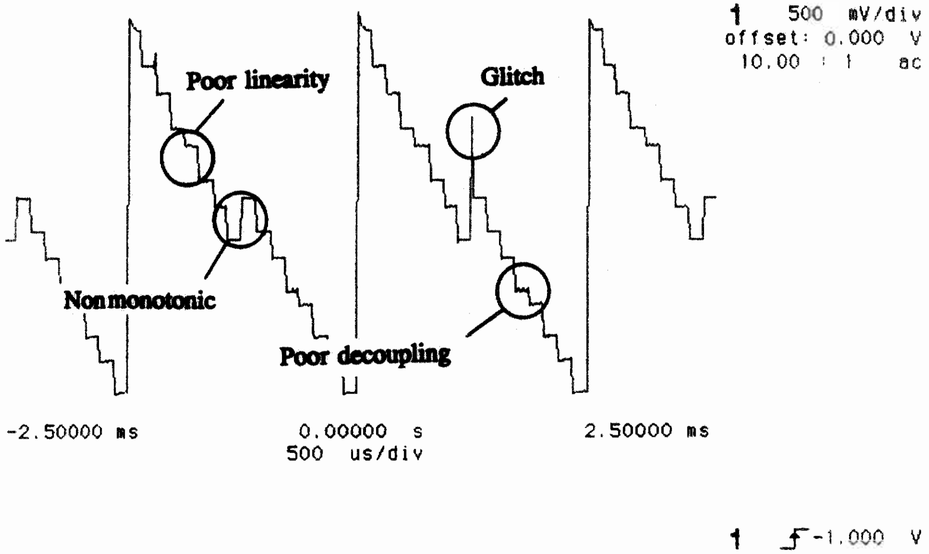


FIGURE 8.6 Oscilloscope display showing several imperfections in a low-quality D/A converter. (Test equipment courtesy of Hewlett-Packard Company.)

manner, one end of the range can be correct but the other extreme too high or too low. This is called a *gain error* or *scaling error*.

As with A/D converters, we normally want a *monotonic* output. In other words, the output should increase whenever the input number increases. However, it is possible for a D/A converter to have a reduction in analog output at a particular point in its range, even though the digital input is increasing uniformly.

Figure 8.6 shows the performance of a low-quality D/A converter. Several of the potential problems described are present in the converted waveform. The input to the converter is a 4-bit down counter (e.g., 15, 14, 13 . . . 2, 1, 0, 15), and the analog output should be 16 equally spaced, decreasing steps for each cycle, producing a reverse sawtooth waveform. If you examine the waveform carefully, you can see the 16 distinct output levels; however, the steps are not equal in amplitude (linearity problems)—the midpoint level actually increases instead of decreases (nonmonotonic), and there are several *glitches* caused by switching transients. Although the performance indicated by the waveform in Figure 8.6 is certainly not representative of a practical D/A converter, it does provide an excellent example of several terms and definitions.

Let us now examine the actual circuitry for several of the more common methods of D/A and A/D conversion.

8.2 WEIGHTED D/A CONVERTER

Figure 8.7 shows the schematic diagram of a weighted digital-to-analog converter circuit built around a 741 op amp. You should recognize the configuration as being identical to the inverting summing amplifier discussed in Chapter 2.

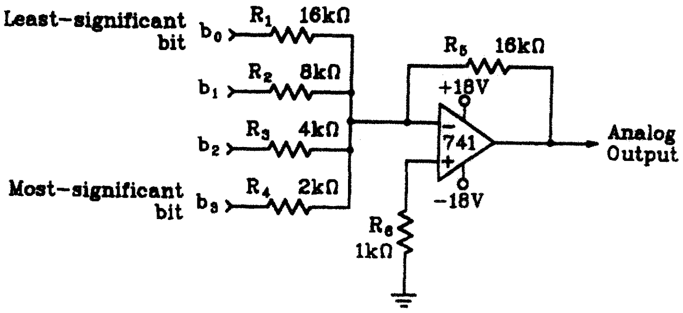

Least-significant bit
b_0
R_1 16kΩ
b_1
R_2 8kΩ
b_2
R_3 4kΩ
Most-significant bit
b_3
R_4 2kΩ
R_5 16kΩ
+18V
741
−18V
R_6 1kΩ
Analog Output

FIGURE 8.7 A weighted D/A converter with 4-bit resolution.

Recall that the gain for each input is determined by the ratio of the feedback resistor and the respective input resistor. In the circuit in Figure 8.7, the individual gains are as follows:

$$A_{V_1} = -\frac{R_F}{R_1} = -\frac{16\ k\Omega}{16\ k\Omega} = -1$$

$$A_{V_2} = -\frac{R_F}{R_2} = -\frac{16\ k\Omega}{8\ k\Omega} = -2$$

$$A_{V_3} = -\frac{R_F}{R_3} = -\frac{16\ k\Omega}{4\ k\Omega} = -4$$

$$A_{V_4} = -\frac{R_F}{R_4} = -\frac{16\ k\Omega}{2\ k\Omega} = -8$$

For purposes of analysis, let us suppose that the two levels for the digital input signals are 0 and –1 volt. Table 8.2 shows the correlation between the digital number and the state of the four inputs.

TABLE 8.2

Digital Number	*Binary Value*	b_3	b_2	b_1	b_0
0	0000	0 volt	0 volt	0 volt	0 volt
1	0001	0 volt	0 volt	0 volt	–1 volt
2	0010	0 volt	0 volt	–1 volt	0 volt
3	0011	0 volt	0 volt	–1 volt	–1 volt
4	0100	0 volt	–1 volt	0 volt	0 volt
5	0101	0 volt	–1 volt	0 volt	–1 volt
6	0110	0 volt	–1 volt	–1 volt	0 volt
7	0111	0 volt	–1 volt	–1 volt	–1 volt

Continued

TABLE 8.2 *(continued)*

Digital Number	*Binary Value*	b_3	b_2	b_1	b_0
8	1000	–1 volt	0 volt	0 volt	0 volt
9	1001	–1 volt	0 volt	0 volt	–1 volt
10	1010	–1 volt	0 volt	–1 volt	0 volt
11	1011	–1 volt	0 volt	–1 volt	–1 volt
12	1100	–1 volt	–1 volt	0 volt	0 volt
13	1101	–1 volt	–1 volt	0 volt	–1 volt
14	1110	–1 volt	–1 volt	–1 volt	0 volt
15	1111	–1 volt	–1 volt	–1 volt	–1 volt

You will likely recall from the discussion of inverting summing amplifiers that the output voltage, at any given time, can be determined simply by adding the output voltages computed for each input individually. For example, if a digital number 5 were input to the circuit, the output voltage would be computed as follows:

$$\begin{aligned}
v_{O_0} &= A_{V_1}v_{I_0} = -1(-1\ V) = +1\ V\\
v_{O_1} &= A_{V_1}v_{I_1} = -2(0) = 0\ V\\
v_{O_2} &= A_{V_2}v_{I_2} = -4(-1\ V) = +4\ V\\
v_{O_3} &= A_{V_3}v_{I_3} = -8(0) = 0\ V\\
\textit{analog output} &= v_{O_0} + v_{O_1} + v_{O_2} + v_{O_3} = +1\ V + 0 + 4\ V + 0 = +5\ V
\end{aligned}$$

The scaling factor for the converter is such that each step in the output corresponds to 1 volt, which means that the analog voltage output will be the same **numerical** value as the digital input. This is not necessarily true for all converters—the full-scale **digital** input for a 4-bit converter will always be 1111 (decimal 15). The full-scale output for the D/A converter shown in Figure 8.7 is 15 volts, but it could just as easily be 5 volts, 10 volts, or any other number depending upon the scale factor of the converter circuit.

For satisfactory performance, the input resistors must be very carefully selected (i.e., precision values) in order to maintain the correct ratios. If one or more resistors are the wrong value, the output will exhibit problems that include poor linearity and/or lack of monotonicity. Even with careful selection of resistors, the simple weighted D/A converter is only useful for small numbers of bits, since the ratio of the smallest to the largest resistor quickly becomes impractical—that is, the ratio increases as 2^{N-1}, where N is the number of bits in the input. For example, the resistor in the least significant input of a 10-bit converter would be 2^{10-1}, or 512 times larger than the resistor for the most significant input.

A variation of the basic weighted D/A converter involves dividing the bits into two or more groups and converting each group separately. The weighting resistors for each group are identical, and the outputs from each of the individual converters can then be summed into a weighted, summing amplifier to produce the final output.

8.3 R2R LADDER D/A CONVERTER

One of the most popular methods for D/A conversion is shown in Figure 8.8. It is called an *R2R ladder D/A converter*, since the input network resembles the rungs on a ladder and the resistors in the input network are either equal (R) or have a 2:1 ratio ($2R$). One advantage of the R2R converter over the weighted converter previously discussed is immediately apparent; the resistors have a 2:1 ratio *regardless* of the number of bits being converted. This makes matching resistors much easier and even makes the use of integrated resistors practical.

An easy way to analyze the operation of the circuit is to Thevenize the input circuit for one or more digital input numbers. This process was described in Chapter 1. Once the input circuit has been simplified with Thevenin's Theorem, you will be left with a simple inverting amplifier circuit whose input voltage is the Thevenin equivalent voltage and whose gain is determined by the ratio of feedback resistance to Thevenin equivalent input resistance. By performing several analyses with different input numbers, you will discover that the least significant input (b_0) produces the least effect on output voltage, and the next input (b_1) has twice as much effect on output voltage. Similarly, bit b_2 has twice the effect of b_1 but only half the effect on output voltage of b_3. These variable effects are identical to the relative weights of the digits in a binary number.

The actual performance of an inexpensive R2R ladder D/A converter circuit similar to the one shown in Figure 8.8 is revealed by the oscilloscope waveform in Figure 8.9. Although the linearity is certainly less than optimum, it clearly illus-

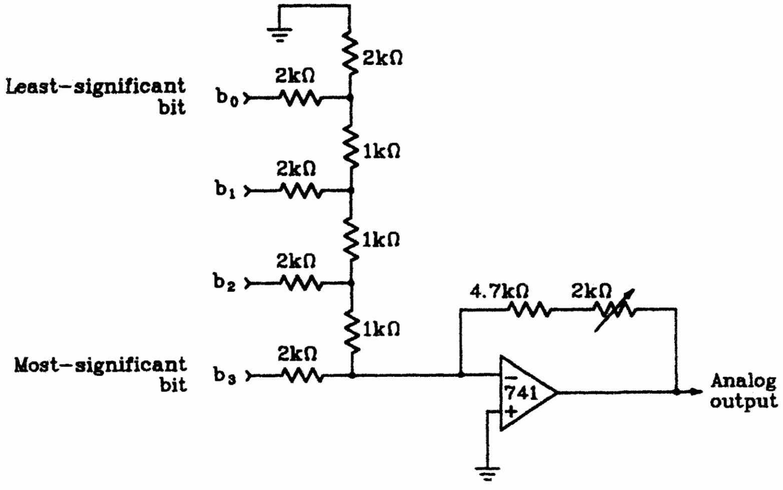
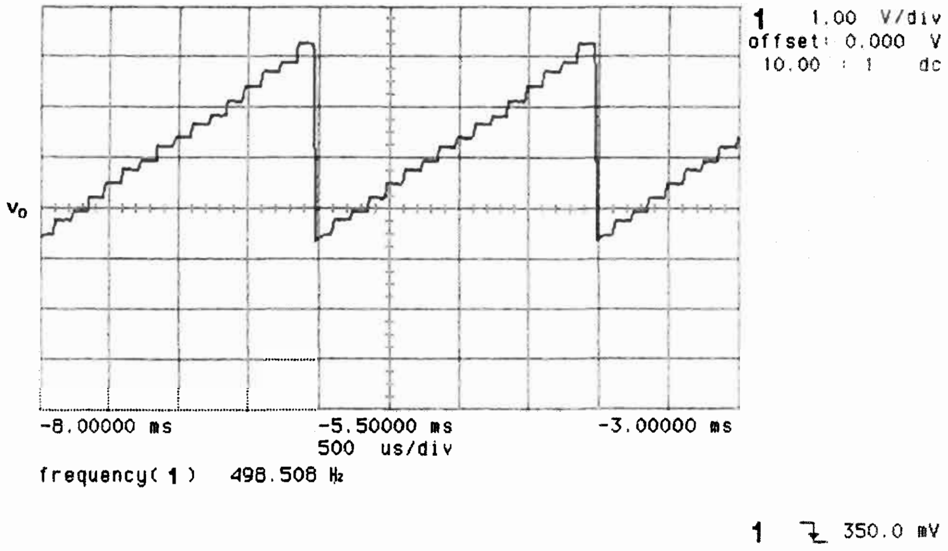
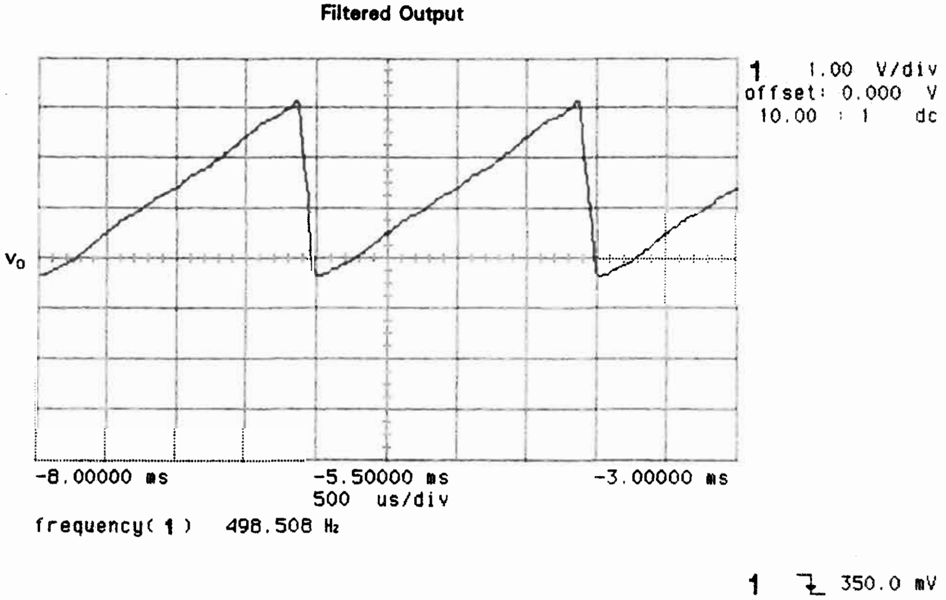


FIGURE 8.8 A 4-bit R2R ladder D/A converter utilizing a 741 op amp.



(a)



(b)

FIGURE 8.9 Oscilloscope displays showing the performance of the 4-bit D/A converter shown in Figure 8.8. (Test equipment courtesy of Hewlett-Packard Company.)

trates the principles involved and would be adequate for many D/A applications. The linearity could be **greatly** improved by using precision resistors (rather than 5 percent) and by driving the digital inputs via analog switches (rather than directly from the output of a digital counter). Figure 8.9(a) shows the actual output of the converter, with the 16 distinct output levels in the waveform easily seen. Figure 8.9(b) shows the same basic circuit after the output has gone through a simple low-pass filter. The abrupt changes in the output are now gone, leaving us with a cleaner analog signal.

For noncritical applications, construction of your own D/A converters is feasible. However, the low cost and high performance (e.g., laser-trimmed ladder resistors) available in integrated converters makes these devices the best choice for many applications. An example of such a device is the TDC1016 10-bit D/A converter manufactured by Raytheon Semiconductor.

8.4 PARALLEL A/D CONVERTER

Parallel A/D conversion (sometimes called *flash* conversion) is the fastest technique available and the simplest to understand. However, its practicality is limited to small numbers of bits, since it requires $2^N - 1$ comparator circuits in order to produce an N-bit digital output. For example, producing a 3-bit digital output (8 states) requires $2^3 - 1$, or 7, comparator circuits plus a significant amount of logic circuitry. Figure 8.10 shows the complete schematic diagram of a 3-bit parallel A/D converter circuit (including decoder logic).

The operation of the circuit is very straightforward. The voltage divider provides a stable reference for one input of each of the seven voltage comparators. Further, each voltage tap on the divider is 1.25 volts higher than the preceding one, which effectively divides the 10-volt range into 8 distinct ranges. These ranges and the corresponding comparator outputs are shown in Table 8.3, which also shows the converted digital output for each voltage range.

The converted digital output for the given converter is in standard binary format. Actual converter circuits, however, may use any one of a variety of codes, including binary, Gray Code, excess-3, and others.

It is also possible to utilize the parallel converter in a hybrid configuration that gains some of the advantage of parallel conversion and yet avoids the geometrically increasing complexity normally associated with it. This hybrid method essentially consists of applying the analog voltage to a small (4–7 bits) parallel converter. This converter generates the most significant bits in the converted number, and the digits are then reconverted to analog with a D/A converter and subtracted from the original input signal. The difference voltage is then converted with a second parallel converter to produce the least significant bits of the digital result. This multistage method of parallel A/D conversion is faster than nonparallel methods but slower than a pure parallel approach. The complexity, however, is less than that of a pure parallel converter circuit. The AD9028 high-speed 8-bit A/D converter circuit, manufactured by Analog Devices, Inc., is an example of a parallel converter. It can deliver an 8-bit output in 3.3 nanoseconds.

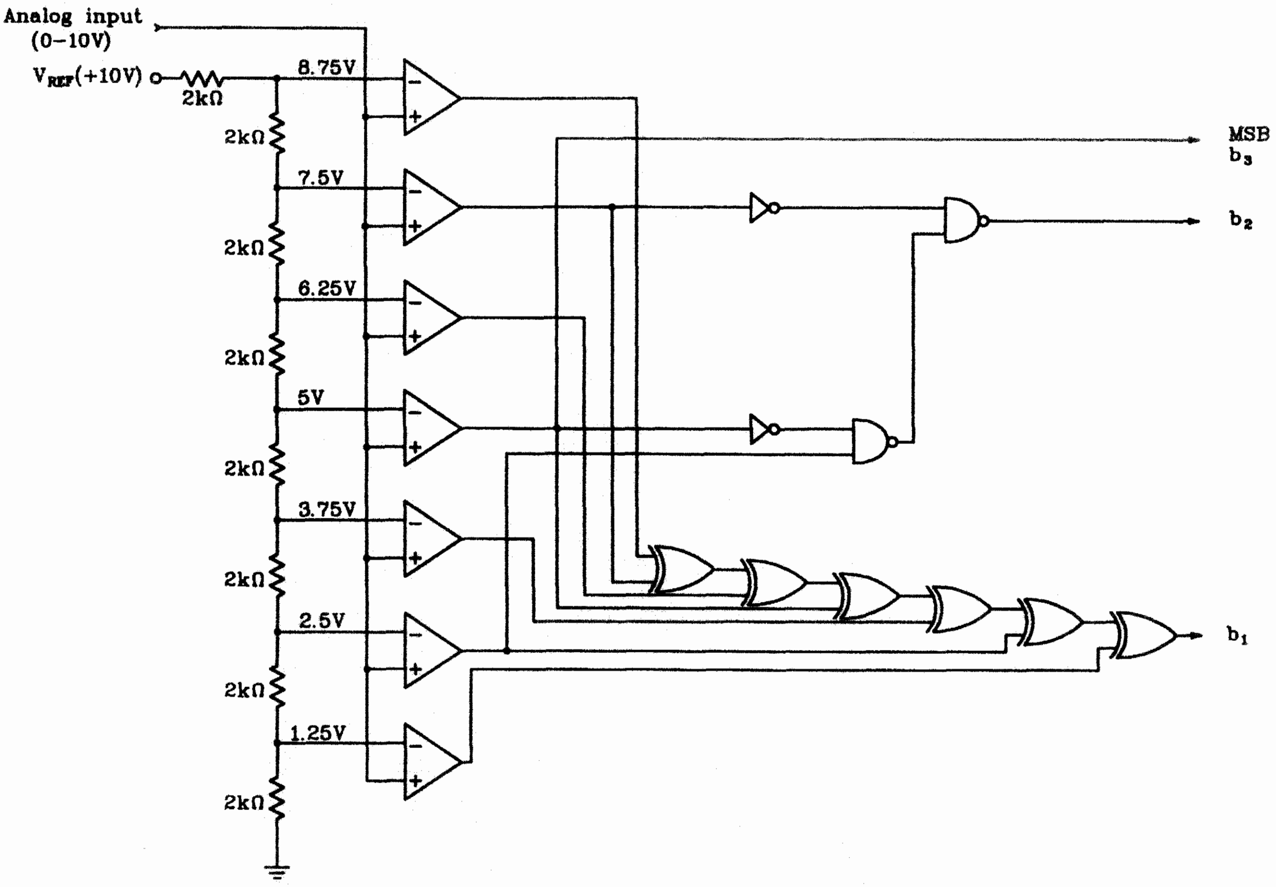

Analog input
(0–10V)
V_REF(+10V)
2kΩ
8.75V
7.5V
6.25V
5V
3.75V
2.5V
1.25V
2kΩ
2kΩ
2kΩ
2kΩ
2kΩ
2kΩ
2kΩ
2kΩ
MSB
b3
b2
b1

FIGURE 8.10 A 3-bit parallel A/D converter with a natural binary output.

TABLE 8.3

Voltage Range	*Comparator States*	*Digital Result*
$0 \leq v_{IN} < 1.25$ Volts	0000000	000
1.25 Volts $\leq v_{IN} <$2.5 Volts	0000001	001
2.5 Volts $\leq v_{IN} <$ 3.75 Volts	0000011	010
3.75 Volts $\leq v_{IN} <$ 5 Volts	0000111	011
5 Volts $\leq v_{IN} <$ 6.25 Volts	0001111	100
6.25 Volts $\leq v_{IN} <$ 7.5 Volts	0011111	101
7.5 Volts $\leq v_{IN} <$ 8.75 Volts	0111111	110
8.75 Volts $\leq v_{IN} <$ 10 Volts	1111111	111

8.5 TRACKING A/D CONVERTER

Figure 8.11 shows the schematic diagram of a tracking A/D converter. Here, the op amp plays a small but important role as a voltage comparator.

To understand the operation of the circuit, let us begin by assuming that the counter is at 0 and the analog input is at some positive voltage. The output of the counter (0 at the present time) is converted to an analog voltage by a D/A converter and applied to one input of a comparator. The other input is the amplified analog

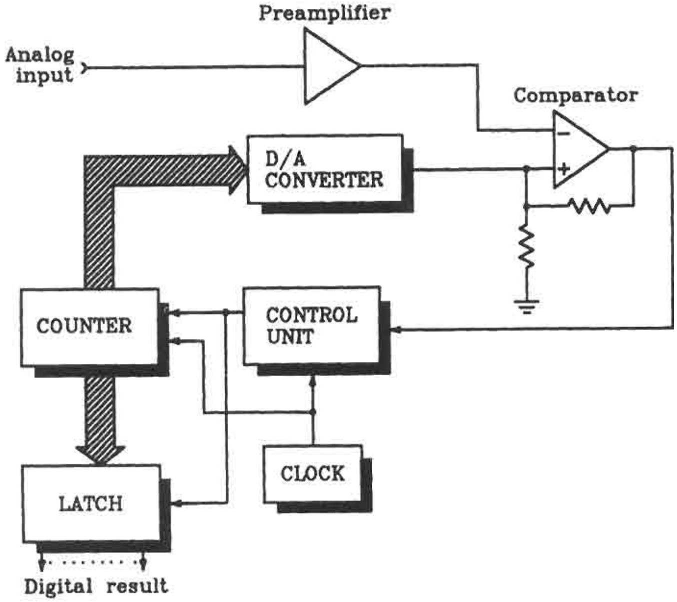


FIGURE 8.11 A tracking A/D converter will continuously follow (i.e., track) the analog input signal.

input signal. Under the given conditions, the output of the comparator will be low. The control unit interprets this comparator output to mean that the counter output is lower than the analog input, so the counter is allowed to increment.

This situation continues on each subsequent clock pulse until the counter has incremented to a value that exceeds the analog input voltage. When this point is reached, the output of the D/A will be higher than the analog input voltage, causing the comparator output to go to a high level. The control unit interprets this to mean that the counter has exceeded the input and directs the counter to begin counting down.

As the counter decrements, the output of the D/A becomes less. As soon as the D/A output falls below the analog input, the output of the comparator switches low again and causes the counter to start incrementing once more. Thus, as the input changes the counter automatically tracks it.

Every time the comparator *changes* state, the control unit transfers the counter value to a latch where it is accessible to other circuitry. This method is simple and inexpensive, but it is not particularly fast (especially for large input changes). For example, let us assume that the clock is operating at 20 megahertz and the converter is designed to provide a 16-bit output. If the input signal makes a small (equivalent of 1 bit) change, then it will take the circuit 1/20 megahertz, or 50 nanoseconds, to provide a valid output. However, if the input makes a full-range step change, it takes the converter (1/20 MHz) × 2^{16}, or 3.28 milliseconds, to provide a valid result. This converter is best suited for either slow signals or signals that make only small changes at any given time.

The oscilloscope display in Figure 8.12 shows the performance of an actual tracking A/D converter circuit. The two superimposed waveforms are taken from

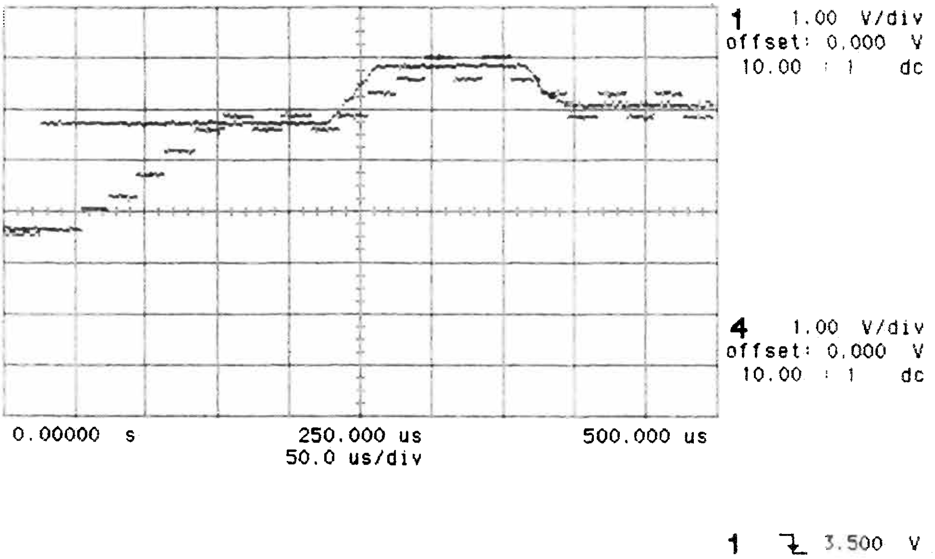


FIGURE 8.12 Oscilloscope display showing the operation of a tracking A/D converter circuit. (Test equipment courtesy of Hewlett-Packard Company.)

the two inputs of the op amp voltage comparator (refer to Figure 8.11). Near the left side of the screen, the analog input signal makes a large step change. It takes the counter and A/D circuit six clock pulses to climb to the new input level. At this point, the counter and A/D signal oscillate back and forth on either side of the analog signal. This oscillation in the least significant bit will always occur, since the counter must always count either up or down.

Near the center of the screen in Figure 8.12, the analog input makes another upward change, which the counter and D/A output can be seen to track. Similarly, when the input makes a negative transition, the counter and D/A output continue to track the input signal. The response time of the tracking A/D converter is determined solely by the frequency of the input clock.

8.6 DUAL-SLOPE A/D CONVERSION

Figure 8.13 shows the schematic diagram of a basic dual-slope A/D converter. Let us first examine each of its subcircuits and then analyze the overall operation of the circuit.

The heart of the circuit is an op amp, linear ramp generator circuit. Figure 8.14 shows the ramp generator isolated from the rest of the converter circuit. It is designed such that the charging current for capacitor C will always be constant. Basic circuit theory tells us that a constant charging current through a capacitor produces a linear ramp of voltage.

To understand the operation of the ramp generator circuit, let us assume that the capacitor is initially discharged (i.e., 0 volts). This is the purpose of transistor Q_1—as long as it is saturated, capacitor C cannot accumulate a charge. Although the actual saturation voltage of Q_1 may be a few millivolts, let us assume it is truly 0 volts for simplicity. Let us further assume (as an example) that the input voltage to the ramp generator is +5 volts. Now let us cut off transistor Q_1 and allow capac-

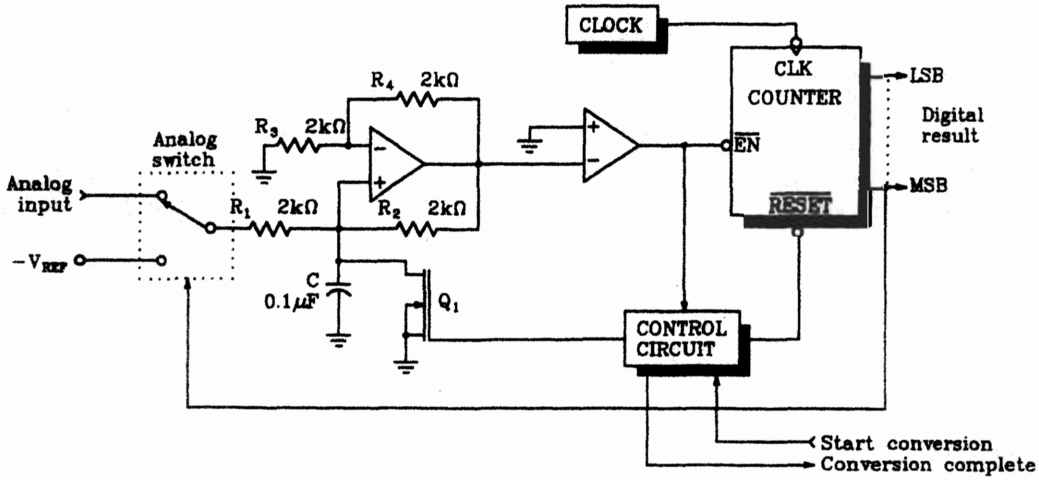


FIGURE 8.13 A basic dual-slope analog-to-digital converter circuit.

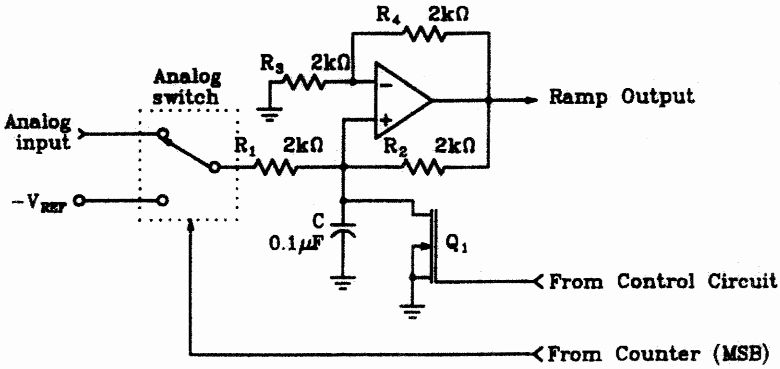


FIGURE 8.14 The linear ramp generator portion of the circuit shown in Figure 8.13.

itor C to begin charging. We will compute the current through the capacitor at several times.

At the first instant after Q_1 is cut off, the capacitor has 0 volts of charge. Ohm's Law tells us that resistor R_1 will have a current of

$$I_{R_1} = \frac{V_{R_1}}{R_1} = \frac{5\ V - 0}{2\ k\Omega} = 2.5\ mA$$

The op amp is essentially a noninverting amplifier with respect to the capacitor voltage. The voltage gain is given by our basic equation for noninverting amplifiers.

$$A_V = \frac{R_F}{R_{IN}} + 1 = \frac{2\ k\Omega}{2\ k\Omega} + 1 = 2$$

The output voltage at this instant will be 0 volts (i.e, 0 × 2). Resistor R_2 will have 0 volts on both ends, which means it has no current flow through it. We know that negligible current flows in or out of the (+) terminal of the op amp. Now, since 2.5 milliamperes of current is flowing through R_1, but no current flows to the op amp or through R_2, we can apply Kirchhoff's Current Law to conclude that the entire 2.5 milliamperes must be flowing into capacitor C as a charging current. The direction of the electron current is from ground, up through capacitor C, and through R_1 to the positive 5-volt source. This establishes the initial slope of the charge on C. If we can maintain a constant current, we will maintain a linear slope across C.

Now let us examine the circuit condition after capacitor C has accumulated 1 volt of charge (positive on top). The current through R_1 can now be computed as

$$I_{R_1} = \frac{V_{R_1}}{R_1} = \frac{5\ V - 1}{2\ k\Omega} = 2\ mA$$

With 1 volt on the capacitor and a voltage gain of 2, we can compute the output voltage of the op amp as

$$v_O = v_{IN} \times A_V = 1\ V \times 2 = 2\ V$$

The current through R_2 can be found with Ohm's Law, since it has 1 volt on the left end and 2 volts on the right end.

$$I_{R_2} = \frac{V_{R_2}}{R_2} = \frac{2\ V - 1\ V}{2\ k\Omega} = 0.5\ mA$$

Again, Kirchhoff's Current Law will let us conclude that if 2 milliamperes are flowing to the left through R_1 and 0.5 milliampere is flowing to the right through R_2, then capacitor C must still be charging with a 2.5-milliampere current. Let us examine the circuit at one more point.

Suppose we let capacitor C accumulate a charge of 4 volts. The current through R_1 will then be

$$I_{R_1} = \frac{V_{R_1}}{R_1} = \frac{5\ V - 4\ V}{2\ k\Omega} = 0.5\ mA$$

With +4 volts on the capacitor, the output voltage of the op amp must be

$$v_O = v_{IN} A_V = 4\ V \times 2 = 8\ V$$

The current through R_2 can be calculated as

$$I_{R_2} = \frac{V_{R_2}}{R_2} = \frac{8\ V - 4\ V}{2\ k\Omega} = 2\ mA$$

Finally, we apply Kirchhoff's Current Law to show that with 0.5 milliampere flowing right to left through R_1 and 2 milliamperes flowing left to right through R_2, there must surely be 2.5 milliamperes flowing upward through capacitor C. Since the current through capacitor C has remained constant at 2.5 milliamperes, we know that the voltage across it will be a linearly rising ramp. The slope of the ramp is given by the basic capacitor charge equation:

$$slope = \frac{V_C}{T} = \frac{I_C}{C}$$

For the present case, the slope of the ramp across C is computed as

$$slope = \frac{I_C}{C} = \frac{2.5\ mA}{0.1\ \mu F} = 25\ V/ms$$

The output of the op amp will have a slope that is linear but twice as great, since the amplifier has a voltage gain of 2. In either case, the slope of the ramp is determined by the charging current of C, which is determined by the value of input voltage.

Now, let us analyze the overall operation of the dual-ramp A/D converter shown in Figure 8.13. The input voltage to the ramp is switch-selected as either the analog voltage to be converted (positive) or a fixed, negative reference voltage. Recall that the input voltage to the ramp circuit determines the slope of the ramp. The position of the analog switch is controlled by the state of the most significant bit (MSB) of a counter. More specifically, if the MSB is low, then the switch will connect the analog input to the ramp generator. If the MSB of the counter is high, then the switch connects the negative reference voltage to the ramp generator input.

The counter is enabled (i.e., allowed to count) as long as the output of the ramp generator is positive. That is, as long as the ramp is above ground, the output of the comparator will be low and will enable the counter. If the ramp ever goes below ground, then the output of the comparator will switch to a high state and disable the counter.

The control circuit provides the overall timing of circuit operation. On receipt of a *start conversion* signal from the main control system (generally a microprocessor), the control unit will reset the counter to 0 and release (i.e., cut off) Q_1. With the counter reset, the MSB will be 0 and the analog switch will be connecting the analog input to the ramp generator circuit. As the counter counts up, the capacitor voltage (and the op amp output) will be linearly ramping up in a positive direction. This action is indicated in Figure 8.15 as t_1.

This action will continue until the counter reaches one-half of its maximum count. At this point, the MSB of the counter will go high and cause the analog switch to move to the reference voltage position. With a negative input voltage applied to the ramp generator, the capacitor will begin to discharge. The discharge will be linear, and the rate will be determined by the value of the negative reference voltage. Eventually, the decreasing ramp will pass through 0 volts, causing the comparator to switch states and disabling the counter. The control circuit senses this event and generates the *conversion complete* signal, which means that the digital result in the counter is now a valid representation of the analog input voltage.

We know that the initial slope (during time t_1 in Figure 8.15) is determined by the value of the analog input voltage. The length of time for t_1, however, is fixed and determined by the speed of the clock and the number of bits in the counter. Time t_2 in Figure 8.15 is the amount of time required for the capacitor to

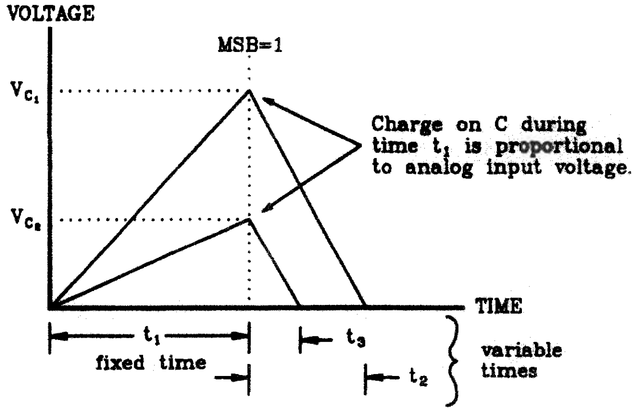


FIGURE 8.15 The positive slope of a dual-slope converter is determined by the value of analog input voltage. The slope of the negative ramp is determined by V_{REF}.

linearly discharge to 0 volts. The slope of t_2 is fixed and is determined by the negative reference, so time t_2 is variable and dependent on the value of voltage accumulated on capacitor C during time t_1. This voltage, of course, was determined by the value of analog input voltage. Since time t_2 is dependent on the value of analog input voltage, the number of counts registered in the counter will also be a function of the analog input voltage.

Figure 8.15 contrasts the results of two different analog input voltages. V_{C1} is the result of a higher input voltage. It takes a certain amount of time (t_2) to discharge the capacitor and stop the counter. A lower input voltage (V_{C2}) charges C to a lower voltage during the fixed time period t_1, so the discharge time (t_3) is shorter and the counter will have a smaller count. The final converted result appears in the counter and ignores the MSB.

The dual-slope A/D conversion method is very popular in applications that do not require high-speed operation. It has distinct advantages that include high immunity to component tolerances, component drifts, and noise. This increased immunity stems from the fact that errors introduced during the positive slope will be largely offset by similar errors during the negative slope. The circuit offers total rejection of noise signals that are even multiples of the time period t_1, since the net effect of a full cycle of noise is 0.

Complete dual-slope converter systems are available in integrated form. A common application is for digital voltmeters. The analog portion of such a system is manufactured by National Semiconductor Corporation in the form of an LF12300 integrated circuit. Analog Devices has a patented improvement on the basic dual-slope converter called Quad-Slope conversion. This is used in the AD7550 13-bit A/D converter manufactured by Analog Devices.

8.7 SUCCESSIVE APPROXIMATION A/D CONVERTER

Figure 8.16 shows the functional block diagram of a successive approximation analog-to-digital converter system. This is probably the most widely used type of A/D converter because it is fairly simple and yet offers a relatively high speed of operation.

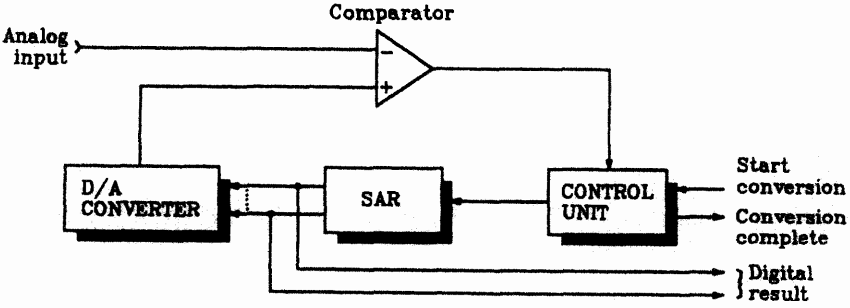


FIGURE 8.16 A functional block diagram of a successive-approximation analog-to-digital converter circuit.

The analog input signal provides one input to a voltage comparator. The second input comes from the output of a D/A converter. The input to the D/A converter is provided by an addressable latch called the successive approximation register (SAR). Each bit of this register can be selectively set or cleared by the control unit. The control unit can be an internal portion of an integrated circuit, or it may be a complete microprocessor system. In any case, the overall operation of the successive approximation converter is described.

Let us suppose that the analog input voltage is 5.7 volts. Let us further suppose that the SAR and D/A converters are 4-bit devices that provide 0.625 volts per step at the output of the D/A converter. Finally, let us assume that the SAR is initially set to 1000, thus producing a 5-volt output for the D/A converter.

Under these conditions, the output of the comparator will be low, since the analog input (inverting input) is higher than the D/A output voltage (noninverting input). The control unit interprets this to mean that the SAR value is too low, and it then leaves the MSB (b_3) alone and also sets the next bit (b_2). The SAR now holds the binary value of 1100, which converts to 7.5 volts at the output of the D/A converter. Since this exceeds the value of analog input voltage, the comparator output will go high. The control unit interprets this to mean that the SAR value is too high.

The control unit then resets bit b_2 (since that is what caused the excessive value) and sets the next most significant bit (b_1). The SAR value of 1010 is now applied to the D/A converter to produce a comparator input of 6.25 volts. This is still higher than the analog input voltage, so the comparator output remains high. The control unit again interprets this to mean that the SAR value is too large.

The control unit then resets bit b_1 and sets the next lower bit (b_0), thus yielding an SAR value of 1001. This converts to 5.625 volts at the output of the comparator. Since this is still lower than the analog input, b_0 will remain set. The *conversion complete* signal is now generated, indicating a completed conversion. The result (1001) is available in the SAR.

In general, the control unit starts by setting the most significant bit and monitoring the output of the comparator. This bit will then be left set or will be reset as a function of the state of the comparator. In either case, the same process is applied to the next lower bit and so forth until the least significant bit is left either set or reset. With each progressive step, the approximation gets closer. Regardless of the magnitude of the analog input voltage (within the limits of the converter), it will always take as many clock periods to convert the voltage as there are bits in the converted number. In this example, the successively better approximations were as listed in Table 8.4.

There is a striking similarity between the logic used during the successive approximation process and the logic applied during a split-half troubleshooting exercise. In both cases, each successive step reduces the number of options by one-half.

There are many integrated forms of A/D converters that utilize the successive approximation technique. One such device is the ADC-910, which is a 10-bit converter manufactured by Analog Devices, Inc. It provides a 10-bit result in 6 microseconds and is compatible with microprocessors. It should also be pointed out that all functions represented in Figure 8.16, except for the comparator and

TABLE 8.4

Analog Input (Volts)	*SAR Status*	*D/A Output (Volts)*	*Comparator Output (Volts)*
5.7	1000	5.0	Low
5.7	1100	7.5	High
5.7	1010	6.25	High
5.7	1001	5.625	Low

D/A converter, can be implemented with software internal to a microprocessor. However, the speed is generally much slower than a dedicated converter.

REVIEW QUESTIONS

1. A certain A/D converter has a 12-bit resolution specification for the analog input range of 0 to 10 volts. What is the smallest voltage change that can be represented in the output?
2. If the binary output of an A/D converter does not numerically increase with every increase in input voltage, we say the converter is ____.
3. The total time required for an A/D converter to obtain a valid digital output for a given analog input is called ____.
4. Contrast and explain the terms *acquisition time* and *aperture time* with reference to sample-and-hold circuits.
5. Would a weighted D/A converter be the best choice for a 64-bit converter circuit? Explain your answer.
6. What type of A/D conversion circuit provides the fastest conversion times? What are its disadvantages?
7. If a certain successive approximation A/D converter requires 10 microseconds to resolve a 0-volt to 2-volt step change on the input, how long will it take to resolve a 0-volt to 5-volt step change?
8. Repeat question 7 for a tracking A/D converter.
9. The use of a sample-and-hold circuit greatly reduces the highest usable frequency for an A/D converter. (True or False)
10. Discuss the relationship between droop rate in a sample-and-hold circuit and the necessary conversion time of a subsequent A/D converter circuit.

CHAPTER NINE

Arithmetic Function Circuits

This chapter presents several circuits designed to perform mathematical operations, including adding, subtracting, averaging, absolute value, and sign changing. Several other common but more complex circuits that perform mathematical functions are presented in Chapter 11.

9.1 ADDER

An adder circuit has two or more signal inputs, either AC or DC, and a single output. The magnitude and polarity of the output at any given time is the algebraic sum of the various inputs. In Chapter 2, we discussed an inverting adder circuit, called an inverting summing amplifier. If we make the feedback resistor and all input resistors the same size, the circuit provides a mathematically correct sum (i.e., no voltage gain). The following discussion will introduce the noninverting adder circuit.

9.1.1 Operation

Figure 9.1 shows the schematic diagram for a noninverting adder circuit. The input signals may be AC, DC, or some combination. The op amp, in conjunction with R_1 and R_2, is a simple noninverting amplifier whose gain is determined by the ratio of R_2 to R_1. Whatever voltage appears on the (+) input will be amplified.

The voltage that appears on the (+) input is the output of a resistive network composed of R_3 through R_N and the associated input voltages. Since all input resistors are equal in value and connect together at the (+) input, we can infer that the relative effects of the inputs are identical. The absolute effect, of course, is determined by the gain of the amplifier. If R_2 is set to the correct value, then the gain of the op amp will be such that the output voltage corresponds to the sum of the input voltages.

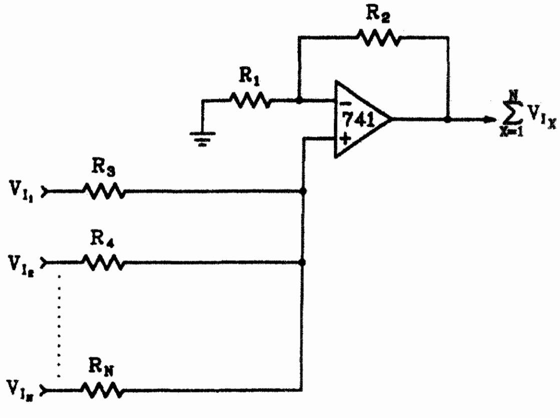


FIGURE 9.1 A noninverting adder circuit sums the instantaneous voltage at several inputs.

9.1.2 Numerical Analysis

We will now analyze the circuit shown in Figure 9.2 to numerically confirm its operation. Let us first determine the behavior of the op amp and its gain resistors (R_1 and R_2). These components form a standard noninverting amplifier whose gain can be determined with the familiar gain equation.

$$A_V = \frac{R_F}{R_I} + 1 = \frac{R_2}{R_1} + 1 = \frac{20\ k\Omega}{10\ k\Omega} + 1 = 3$$

The voltage gain of a noninverting adder will always be the same as the number of inputs.

All that remains is to determine the value of voltage on the (+) input pin. One method for calculating this voltage is to apply Thevenin's Theorem to the network, which will give us an equivalent circuit consisting of a single resistor and a single

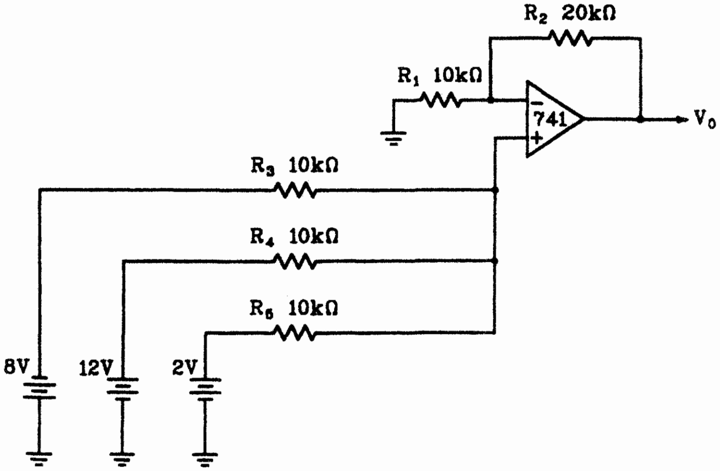


FIGURE 9.2 A 3-input noninverting adder with DC inputs.

voltage source. The application of Thevenin's Theorem is shown sequentially in Figures 9.3(a) through 9.3(c). Figure 9.3(a) shows the original input network. We will apply Thevenin's Theorem to the portion of the circuit within the dotted box.

First we see that we have two opposing voltage sources in this part of the circuit that yield a net voltage of

$$V_X = 12\ V - 2\ V = 10\ V$$

Now, with two equal resistors in the circuit, there will be 5 volts dropped across each one. The equivalent Thevenin voltage, then, can be found with Kirchhoff's Voltage Law.

$$V_{TH} = +12\ V - 5\ V = +7\ V$$

Alternately, we could apply Kirchhoff's Voltage Law as

$$V_{TH} = +2\ V + 5\ V = +7\ V$$

By replacing the two sources with their internal resistances (assumed to be 0), we can determine the Thevenin resistance, which is simply the value of R_5 and R_4 in parallel.

$$R_{TH} = R_4 \| R_5 = \frac{R_4 R_5}{R_4 + R_5} = \frac{10\ k\Omega \times 10\ k\Omega}{10\ k\Omega + 10\ k\Omega} = 5\ k\Omega$$

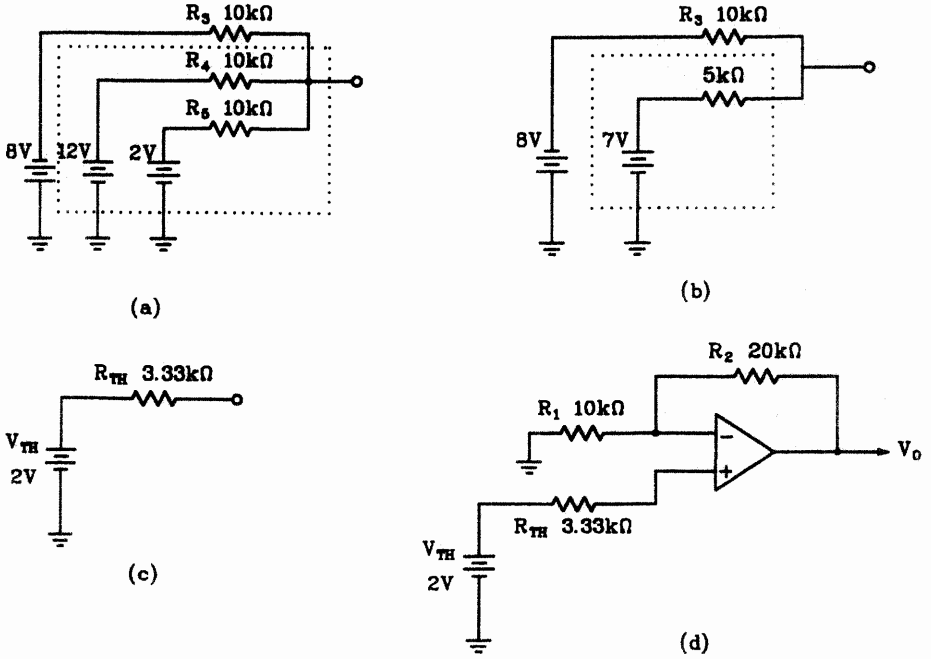


FIGURE 9.3 Application of Thevenin's Theorem to simplify the input network of the noninverting adder circuit.

The results of our first simplification are shown in Figure 9.3(b). The Thevenin equivalents computed above are shown inside the dotted box. We can reapply Thevenin's Theorem to the remaining circuit to obtain our final simplified circuit.

First we see that we have series-aiding voltage sources for an effective voltage source equal to

$$V_X = 7\ V + 8\ V = 15\ V$$

The portion of this effective voltage that drops across R_3 can be found with the voltage divider formula.

$$V_{R_3} = \left(\frac{R_3}{R_3 + R_{TH}}\right)15\ V = \left(\frac{10\ k\Omega}{10\ k\Omega + 5\ k\Omega}\right)15\ V = 10\ V$$

The resulting Thevenin voltage can now be found with Kirchhoff's Voltage Law.

$$V_{TH} = -8\ V + 10\ V = +2\ V$$

We don't really need the value of Thevenin resistance for the remainder of the problem, but, in the name of completeness, we will compute it as

$$R_{TH} = 5\ k\Omega \| 10\ k\Omega = \frac{5\ k\Omega \times 10\ k\Omega}{5\ k\Omega + 10\ k\Omega} = 3.333\ k\Omega$$

The fully simplified circuit is shown in Figure 9.3(c). Our equivalent circuit reconnected to the amplifier portion of the circuit is shown in Figure 9.3(d). The output voltage can be easily computed by applying our basic gain equation.

$$V_O = V_I A_V = 2\ V \times 3 = 6\ V$$

This value confirms the correct operation of our adder, which should provide the algebraic sum of its inputs (i.e., $+2\ V + 12\ V - 8\ V = +6\ V$).

9.1.3 Practical Design Techniques

Let us now design a noninverting adder that will satisfy the following design goals:

1. Accept four inputs	–10 volts < sum < +10 volts
2. Minimum input impedance	>6 kilohms
3. Frequency range	0 to 1 kilohertz

Select the Value for R_1 and for R_3 to R_6. The design of the noninverting adder circuit is very straightforward, since all resistor values are the same with the single exception of the feedback resistor. Selection of the common resistor value is made by considering the following guidelines:

1. High-value resistances magnify the nonideal op amp characteristics and make the circuit more susceptible to external noise.
2. Low-resistor values present more of a load on the driving circuits.

Resistor selection will determine the input impedance presented to the various signal sources as expressed by Equation (9.1).

$$R_{IN} = R\left(\frac{1}{N-1} + 1\right) \tag{9.1}$$

where R is the common resistor value and N is the number of inputs to the adder circuit. Since the design goal specifies a minimum input of 6 kilohms, let us substitute this value into Equation (9.1) and solve for the value of R.

$$6\ k\Omega = R\left(\frac{1}{3} + 1\right)$$

$$R = \frac{6\ k\Omega}{1.333} = 4.8\ k\Omega$$

This represents the smallest value that we can use for the input resistors and still meet our input impedance requirement. Let us choose to use 5.6-kilohm resistors for R_1 and for R_3 to R_6.

Calculate the Feedback Resistor. The value of the feedback resistor must be selected such that the voltage gain is equal to the number of inputs. In our case we will need a gain of 4. Since we already know the value of R_1, we can transpose our basic noninverting amplifier gain equation to determine the value of feedback resistor.

$$A_V = \frac{R_2}{R_1} + 1, \text{ or}$$

$$R_2 = R_1(A_V - 1)$$

Since voltage gain will always be equal to the number of inputs, this can also be written as

$$R_2 = R_1(A_V - 1) = R_1(N - 1) \tag{9.2}$$

In our case, we can compute the required value of R_2 as

$$R_2 = 5.6\ k\Omega(4 - 1) = 16.8\ k\Omega$$

If we expect the adder to generate the correct sum, it is essential to keep the resistor ratios correct. Therefore, since 16.8 kilohms is not a standard value, we will need to use a variable resistor for R_2 or some combination of fixed resistors (e.g., 15 $k\Omega$ in series with 1.8 $k\Omega$).

Select an Op Amp. There are several nonideal op amp parameters that may affect the proper operation of the noninverting adder. An op amp should be selected that minimizes those characteristics most important for a particular application. The various nonideal parameters to be considered are discussed in Chapter 10. In general, if DC signals are to be added, an op amp with a low offset voltage and low drift will likely be in order. For AC applications, bandwidth and slew rate are two important limitations to be considered.

Based on the modest gain/bandwidth requirements for this particular application, let us use a standard 741 op amp. Other, more precision devices can be substituted to optimize a particular characteristic (e.g., low noise). Many of these alternate devices are pin compatible with the basic 741.

The final schematic diagram of our noninverting adder design is shown in Figure 9.4. The measured performance is contrasted with the original design goals in Table 9.1. It should be noted that the noninverting adder is particularly susceptible to component tolerances and nonideal op amp parameters (e.g., bias current and offset voltage). For reliable operation, components must be carefully selected and good construction techniques used.

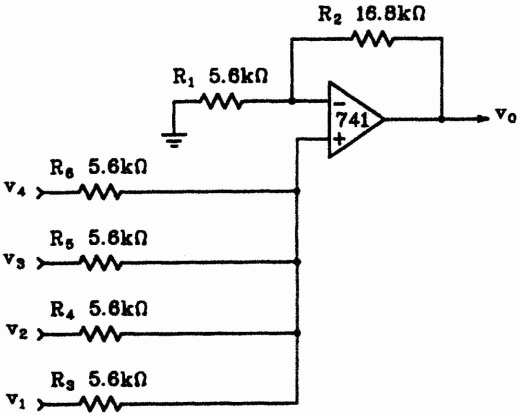


FIGURE 9.4 Final design of a 4-input noninverting adder circuit.

TABLE 9.1

Input Voltages				Output Voltage	
V_1	V_2	V_3	V_4	*Ideal*	*Actual*
-15.09 volts	4.37 volts	0 volts	0 volts	10.72 volts	10.8 volts
-8.1 volts	-2.0 volts	6.6 volts	2.7 volts	-0.8 volts	-0.74 volts
1.52 volts	0 volts	-3.1 volts	-1.49 volts	-3.07 volts	-2.98 volts

9.2 SUBTRACTOR

Another circuit that performs a fundamental arithmetic operation is the subtractor. This circuit generally has two inputs (either AC or DC) and produces an output voltage that is equal to the instantaneous difference between the two input signals. Of course, this is the very definition of a difference amplifier, which is another name for the subtractor circuit.

9.2.1 Operation

Figure 9.5 shows the schematic diagram of a basic subtractor circuit. A simple way to view the operation of the circuit is to mentally apply the Superposition Theorem (without numbers). If we assume that V_A is 0 volts (i.e., grounded), then we can readily see that the circuit functions as a basic inverting amplifier for input V_B. The voltage gain for this input will be determined by the ratio of resistors R_1 and R_2. If we assume that the voltage gain is –1, then the output voltage will be $-V_B$ volts as a result of the V_B input signal.

In a similar manner, we can assume that input V_B is grounded. In this case, we find that the circuit functions as a basic noninverting amplifier with respect to V_A. The overall voltage gain for the V_A input will be determined by the ratio of R_1 and R_2 (sets the op amp gain) and the ratio of R_3 and R_4, which form a voltage divider on the input. If we assume that the voltage divider reduces V_A by half, and we further assume that the op amp provides a voltage gain of 2 for voltages on the (+) input, then we can infer that the output voltage will be $+V_A$ volts as a result of the V_A signal.

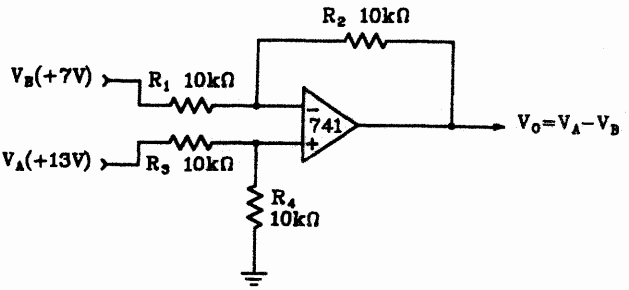


FIGURE 9.5 A subtractor circuit computes the voltage difference between two signals.

According to the Superposition Theorem, the output should be the net result of the two individual input signals. That is, the output voltage will be $+V_A - V_B$. Thus, we can see that the circuit does indeed perform the function of a subtractor circuit.

9.2.2 Numerical Analysis

The numerical analysis of the subtractor circuit is straightforward and consists of applying the Superposition Theorem. Let us first assume that the V_A input is grounded and compute the effects of the V_B input. The output will be equal to V_B times the voltage gain of the inverting amplifier circuit, which is

$$\begin{aligned} V_{O_B} &= V_B \times A_V \\ &= V_B\left(-\frac{R_2}{R_1}\right) \\ &= +7\left(-\frac{10\ k\Omega}{10\ k\Omega}\right) \\ &= -7\ V \end{aligned}$$

Now let us ground the V_B input and compute the output voltage caused by the V_A input. First, V_A is reduced by the voltage divider action of R_3 and R_4. The voltage appearing on the (+) input is computed with the basic voltage divider equation.

$$\begin{aligned} V_A' &= V_A\left(\frac{R_4}{R_3 + R_4}\right) \\ &= +13\ V\left(\frac{10\ k\Omega}{10\ k\Omega + 10\ k\Omega}\right) \\ &= 6.5\ V \end{aligned}$$

The voltage on the (+) input will now be amplified by the voltage gain of the noninverting op amp configuration, which is

$$\begin{aligned} V_{O_A} &= V_A'\left(\frac{R_2}{R_1} + 1\right) \\ &= +6.5\ V\left(\frac{10\ k\Omega}{10\ k\Omega} + 1\right) \\ &= +13\ V \end{aligned}$$

The actual output voltage will be the algebraic sum of the two partial outputs computed:

$$V_O = V_{O_A} + V_{O_B} = +13\ V + (-7\ V) = +6\ V$$

This, of course, is the result that we would expect from a circuit that is supposed to compute the difference between two input voltages.

The input impedance for the inverting input (V_B signal) can be computed with Equation (2.7). For the circuit shown in Figure 9.5, we can compute the inverting input resistance as

$$Z_I = R_1 = 10\ k\Omega$$

The input impedance presented to the noninverting input is essentially the value of R_3 and R_4 in series. That is,

$$Z_I \approx R_3 + R_4 = 10\ k\Omega + 10\ k\Omega = 20\ k\Omega$$

If resistors R_3 and R_4 are quite large, then a more accurate value can be obtained by considering that the input resistance of the op amp itself is in parallel with R_4. The small signal bandwidth of the circuit can be computed by applying Equation (2.22) to the (+) input. For our present circuit, we can estimate the bandwidth as

$$bandwidth = \frac{unity\ gain\ frequency}{closed\text{-}loop\ gain} = \frac{1\ MHz}{2} = 500\ kHz$$

The highest practical operating frequency may be substantially lower than this because of slew rate limiting of larger input signals. If we assume that the output will be required to make the full output swing from $+V_{SAT}$ (+13 V) to $-V_{SAT}$ (−13 V), then we can apply Equation (2.11) to determine the highest input frequency that can be applied without slew rate limiting.

$$f_{SRL} = \frac{slew\ rate}{\pi V_O(\max)} = \frac{0.5\ V/\mu s}{3.14 \times 26\ V} = 6.12\ kHz$$

9.2.3 Practical Design Techniques

Now let us design a subtractor circuit that will satisfy the following design goals:

1. Input voltages	0 to +5 volts
2. Input frequency	0 to 10 kilohertz
3. Input impedance	≥2.5 kilohms

Compute R_1 to R_4. The value of R_1 is determined by the minimum input impedance of the circuit. Its value is found by applying Equation (2.7).

$$R_1 = Z_I = 2.5\ k\Omega$$

Resistors R_2 through R_4 are set equal to R_1 in order to provide the correct subtractor performance. We will use standard values of 2.7 kilohms for these resistors.

Select the Op Amp. The primary considerations for op amp selection are slew rate and bandwidth. Unless the input signals are very small, the slew rate establishes the upper frequency limit. The required slew rate to meet the design specifications can be found by applying Equation (2.11). The maximum output voltage change will be 10 volts and the frequency may be as high as 10 kilohertz.

$$\text{slew rate} = \pi f v_O(\text{max}) = 3.14 \times 10\ kHz \times 10\ V = 0.314\ V/\mu s$$

This is within the range of the standard 741 op amp. The unity gain frequency required to meet the bandwidth requirements can be estimated with Equation (2.22). In the present case, the minimum unity gain frequency is computed as

$$f_{UG} = bw \times A_V = 10\ kHz \times 2 = 20\ kHz$$

which is well below the 1.0-megahertz unity gain frequency of the standard 741. Let us use this device in our design.

There are several other nonideal op amp parameters that could play a significant role in op amp selection. These factors are discussed in Chapter 10.

The schematic of our subtractor design is shown in Figure 9.6. Its performance with two in-phase AC inputs is shown in Figure 9.7, where channels 1 and

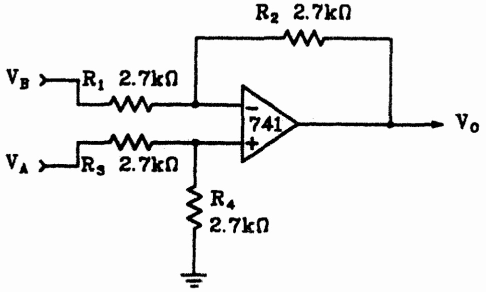
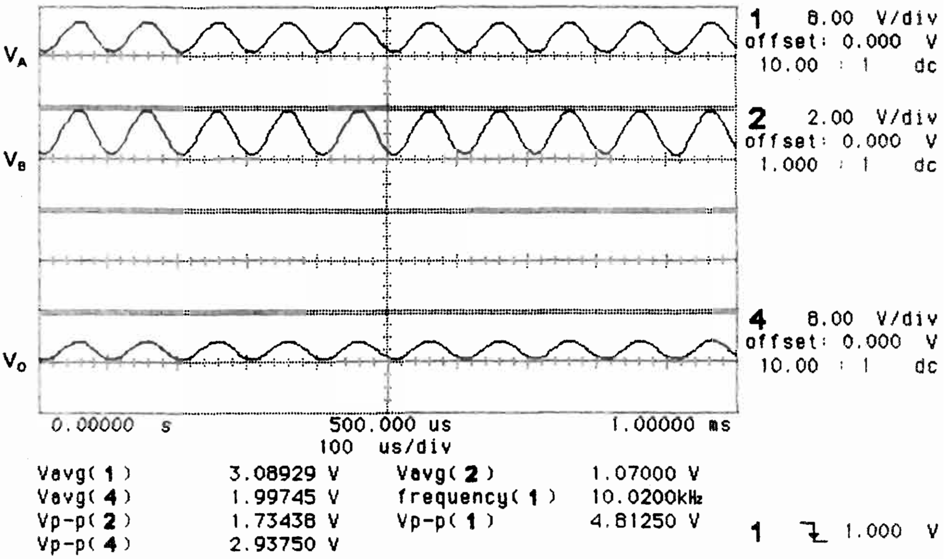


FIGURE 9.6 A subtractor circuit designed for 10-kilohertz operation with 0-volt to 5-volt input signals.



```
1      8.00  V/div
offset: 0.000   V
 10.00  : 1    dc
2      2.00  V/div
offset: 0.000   V
 1.000  : 1    dc
4      8.00  V/div
offset: 0.000   V
 10.00  : 1    dc
0.00000   s           500.000 us              1.00000 ms
                      100  us/div
Vavg( 1 )       3.08929 V    Vavg( 2 )          1.07000 V
Vavg( 4 )       1.99745 V    frequency( 1 )     10.0200kHz
Vp-p( 2 )       1.73438 V    Vp-p( 1 )          4.81250 V     1  ⮧ 1.000  V
Vp-p( 4 )       2.93750 V
```

FIGURE 9.7 Oscilloscope display showing the actual performance of the subtractor circuit shown in Figure 9.6. (Test equipment courtesy of Hewlett-Packard Company.)

TABLE 9.2

Input Voltages		Output Voltage	
V_A	V_B	Design Goal	Measured Value
+4.56 volts	+2.1 volts	+2.46 volts	+2.42 volts
0 volts	0 volts	0 volts	−0.05 volts
+1.6 volts	+3.99 volts	−2.39 volts	−2.43 volts

2 of the oscilloscope are connected to the V_A and V_B inputs, respectively, and channel 4 shows the output of the op amp, which is the desired function ($V_O = V_A - V_B$). The response of the circuit to DC signals is listed in Table 9.2.

9.3 AVERAGING AMPLIFIER

The schematic diagram of an inverting averaging amplifier is shown in Figure 9.8. Although this represents a separate mathematical operation, the configuration of the circuit is similar to that of the inverting adder or inverting summing amplifier discussed in Chapter 2.

Since its operation and design are nearly identical to that of the inverting summing amplifier, only a brief analysis will be given here.

To understand the operation of the averaging amplifier, let us apply Ohm's and Kirchhoff's Laws along with some basic equation manipulation. Since the inverting input (−) is a virtual ground point, each of the input currents can be found with Ohm's Law.

$$I_1 = \frac{V_1}{R_1}, \textit{ and}$$

$$I_2 = \frac{V_2}{R_2}, \textit{ and}$$

$$I_N = \frac{V_N}{R_N}$$

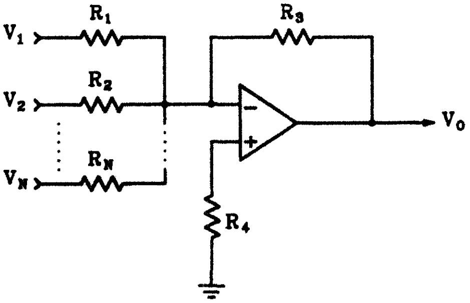


FIGURE 9.8 An N-input averaging amplifier circuit.

Negligible current flows in or out of the (–) input pin, so Kirchhoff's Current Law will show us that the sum of the input currents must be flowing through R_3. That is,

$$I_3 = I_1 + I_2 \ldots + I_N,\ or$$

$$I_3 = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots + \frac{V_N}{R_N}$$

The voltage across R_3 will be equal to the output voltage, since one end of R_3 is connected to a virtual ground point and the other end is connected directly to the output terminal. Therefore, we can conclude that

$$I_3 = -\frac{V_O}{R_3}$$

Now, for proper operation of the averaging circuit, all of the input resistors must be the same value; let us call this value R. Further, the feedback resistor (R_3) is chosen to be equal to R/N where N is the number of inputs to be averaged. Making these substitutions in our previous equations gives us the following:

$$\frac{V_1}{R} + \frac{V_2}{R} \ldots + \frac{V_N}{R} = -\frac{NV_O}{R}$$

$$V_1 + V_2 \ldots + V_N = -NV_O$$

$$-V_O = \frac{V_1 + V_2 \ldots + V_N}{N}$$

This final expression for the output voltage should be recognized as the equation for computing arithmetic averages. That is, add the numbers (input voltages) together and divide by the number of inputs. The minus sign simply shows that the signal is inverted in the process of passing through the op amp circuit.

9.4 ABSOLUTE VALUE CIRCUIT

An op amp circuit can be configured to provide the absolute value (| VALUE |) of a given number. You will recall from basic mathematics that an absolute value function produces the magnitude of a number without regard to sign. In the case of an op amp circuit designed to generate the absolute value of its input, we can expect the output voltage to be equal to the input voltage without regard to polarity. So, for example, a +6.2-volt input and a –6.2-volt input both produce the same (typically +6.2-volt) output.

9.4.1 Operation

There are several ways to obtain the absolute value of a signal. The schematic diagram in Figure 9.9 shows one possible way. The first stage of this circuit is a dual

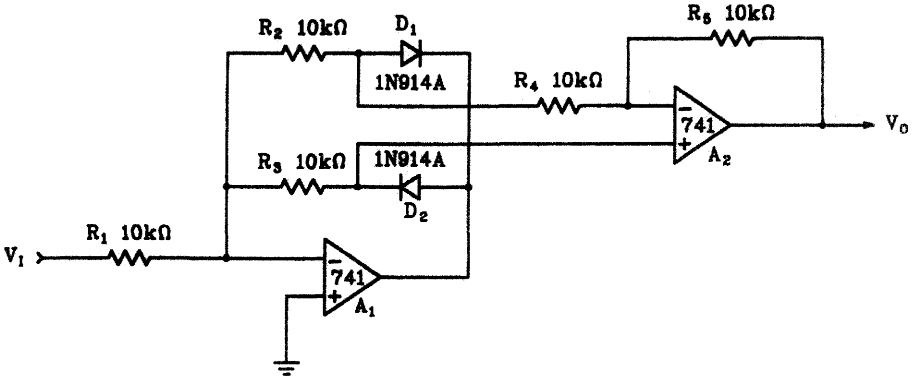


FIGURE 9.9 An absolute value circuit that computes the value of $|V_I|$.

half-wave rectifier, the same as that analyzed in Chapter 7. Recall that on positive input signals, the output goes in a negative direction and forward-biases D_1. This completes the feedback loop through R_2. Additionally, the forward voltage drop of D_1 is essentially eliminated by the gain of the op amp. That is, the voltage at the junction of R_2 and D_1 will be the same magnitude (but opposite polarity) as the input voltage.

When a negative input voltage is applied to the dual half-wave rectifier circuit, the output of the op amp goes in a positive direction. This forward-biases D_2 and completes the feedback loop through R_3. Diode D_1 is reverse-biased. In the case of the basic dual half-wave rectifier circuit, the voltage at the junction of R_3 and D_2 is equal in magnitude (but opposite in polarity) to the input voltage. In the case of the circuit in Figure 9.9, however, this voltage will be somewhat lower because of the loading effect of the current flowing through R_2, R_4, and R_5.

The outputs from the dual half-wave rectifier circuit are applied to the inputs of a difference amplifier circuit. Since the two half-wave signals are initially 180° out of phase, and since only one of them gets inverted by amplifier A_2, we can conclude that the two signals appear at the output of A_2 with the same polarity. In other words, both polarities of input signal produce the same polarity of output signal. By definition, this is an absolute value function.

9.4.2 Numerical Analysis

Now let us extend our understanding of the absolute value circuit shown in Figure 9.9 to a numerical analysis of its operation. First notice that all resistors are the same value, which greatly simplifies our algebraic manipulation. We will analyze the circuit for both polarities of input voltage.

Figure 9.10 shows an equivalent circuit that is valid whenever V_I is positive. The ground on the lower end of R_3 is provided by the virtual ground at the (–) input of A_1. It is easy to see that we now have two inverting amplifiers in cascade, so the output voltage will be equal to the input voltage times the voltage gains of the two amplifiers. That is,

$$V_O = V_I A_{V_1} A_{V_2} = V_I\left(-\frac{R_2}{R_1}\right)\left(-\frac{R_5}{R_4}\right) = V_I\left(\frac{R_2 R_5}{R_1 R_4}\right)$$

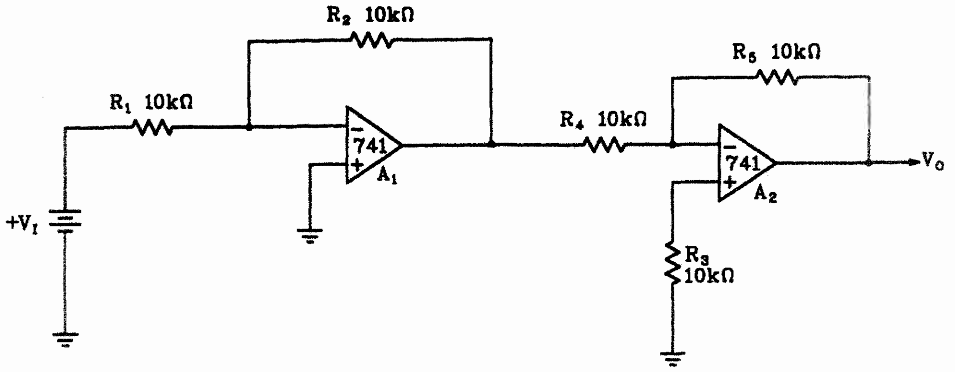

R₂ 10kΩ
R₁ 10kΩ
+V_I
741
A₁
R₄ 10kΩ
R₅ 10kΩ
741
A₂
V₀
R₃ 10kΩ

FIGURE 9.10 An equivalent circuit for the diagram shown in Figure 9.9 during times when V_I is positive.

Since all resistors are the same value (R), we can further simplify the expression for V_O.

$$V_O = V_I\left(\frac{RR}{RR}\right) = V_I$$

In the case of positive input signals, the output voltage is equal to the input voltage.

Now let us consider the effects of negative input voltages. Figure 9.11 shows an equivalent circuit that is valid whenever V_I is negative. Kirchhoff's Current Law, coupled with our understanding of basic op amp operation, allows us to establish the following relationship:

$$I_1 = I_2 + I_3$$

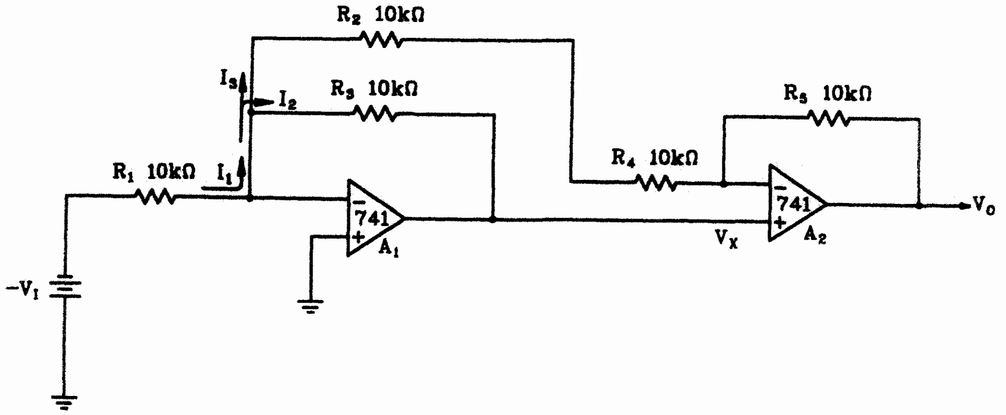

R₂ 10kΩ
I₃
I₂
R₃ 10kΩ
R₅ 10kΩ
R₁ 10kΩ
I₁
R₄ 10kΩ
741
A₁
741
A₂
V₀
V_X
−V_I

FIGURE 9.11 An equivalent circuit for the diagram shown in Figure 9.9 during times when V_I is negative.

Ohm's Law can be used to substitute resistance and voltage values.

$$-\frac{V_I}{R_1} = \frac{V_X}{R_3} + \frac{V_X}{R_2 + R_4}$$

Since all resistor values are equal (R), we can further simplify this latter expression as follows:

$$-\frac{V_I}{R} = \frac{2V_X + V_X}{2R} = \frac{3V_X}{2R}, \textit{ or}$$

$$-V_I = \frac{3V_X}{2}$$

We will come back to this equation momentarily. For now, though, let us determine the output voltage in terms of V_X. Amplifier A_2 is a basic noninverting amplifier with respect to V_X, since the left end of R_2 connects to ground (virtual ground provided by the inverting input of A_1). Therefore, the output voltage can be expressed using our basic gain equation for noninverting amplifiers.

$$V_O = V_X\left(\frac{R_5}{R_2 + R_4} + 1\right)$$

Since the resistors are all equal, we will substitute R for each resistor and solve the equation for V_X.

$$\begin{aligned} V_O &= V_X\left(\frac{R}{R + R} + 1\right) \\ &= V_X\left(\frac{R + 2R}{2R}\right) \\ &= \frac{3V_X}{2}, \textit{ or} \\ V_X &= \frac{2V_O}{3} \end{aligned}$$

If we now substitute this last expression for V_X into our earlier expression, we can determine the output voltage in terms of input voltage. That is,

$$\begin{aligned} -V_I &= \frac{3V_X}{2} \\ &= \frac{3\left(\frac{2V_O}{3}\right)}{2} \\ V_O &= -V_I \end{aligned}$$

For negative input voltages, the output is equal in amplitude but opposite in polarity. This, coupled with our previous analysis for positive input voltages, means that the output voltage is positive for either polarity of input voltage and equal in amplitude to the input voltage. Of course, this is the proper behavior for an absolute value circuit where $V_O = |V_I|$.

The input impedance, output impedance, frequency response, and so on, are computed in the same manner as are similar circuits previously discussed in detail. These calculations are not repeated here.

9.4.3 Practical Design Techniques

Since all resistor values are the same in the absolute value circuit, the calculations for design are fairly straightforward. Let us design an absolute value circuit that will perform according to the following design goals:

1. Input voltage	$-10 \text{ volts} \le V_I \le 10 \text{ volts}$
2. Input impedance	>18 kilohms
3. Frequency range	0 to 100 kilohertz

Select the Value for *R*. The minimum value for all of the resistors is determined by the required input impedance. The maximum value is limited by the nonideal characteristics of the circuit (refer to Chapter 10), but is generally below 100 kilohms. The minimum value for R can be found by applying Equation (2.7).

$$R = \textit{input impedance} = 18\ k\Omega$$

Let us choose to use 22-kilohm resistors for our design.

Select the Op Amps. As usual, slew rate and small signal bandwidth are used as the basis for op amp selection. The required unity gain frequency for A_2 can be computed with Equation (2.22).

$$\begin{aligned} f_{UG} &= bw \times A_V = bw\left(\frac{R_5}{R_2 + R_4} + 1\right) \\ &= 100\ kHz\left(\frac{10\ k\Omega}{10\ k\Omega + 10\ k\Omega} + 1\right) \\ &= 150\ kHz \end{aligned}$$

The bandwidth for A_1 will be somewhat lower because it has a voltage gain of −1. But in either case, the standard 741 will be more than adequate with regard to bandwidth.

The required slew rate for either amplifier can be computed with Equation (2.11). The voltage and frequency limits are stated in the design goals.

$$\textit{slew rate} = \pi f V_O(\text{max}) = 3.14 \times 100\ kHz \times 20\ V = 6.28\ V/\mu s$$

This slew rate exceeds the capability of the standard 741, but falls within the 10-volts-per-microsecond slew rate capability of the MC1741SC. Let us utilize this device in our design. It should be noted that in critical applications several additional nonideal op amp characteristics should be evaluated before a particular op amp is selected. These characteristics are discussed in Chapter 10.

The final schematic diagram for our absolute value circuit is shown in Figure 9.12. Its performance is evident from the oscilloscope displays in Figure 9.13. In Figure 9.13(a) the input is a sinewave. Since both polarities of input translate to a positive output, we have essentially built an ideal full-wave rectifier circuit. Figure 9.13(b) shows the circuit's response to a very slow (essentially varying DC) triangle wave.

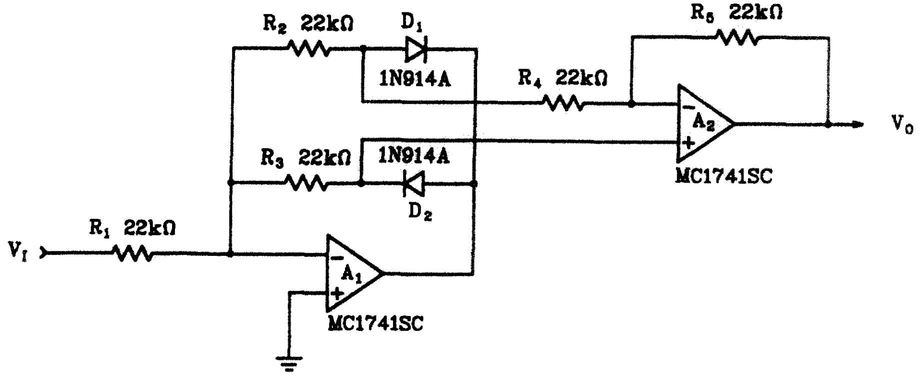
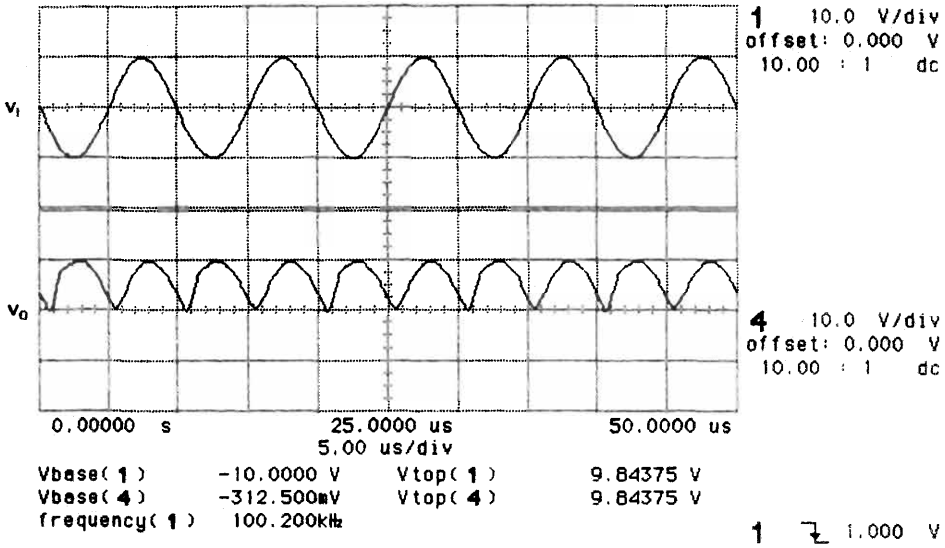


FIGURE 9.12 Final design of a 100-kilohertz absolute value circuit.

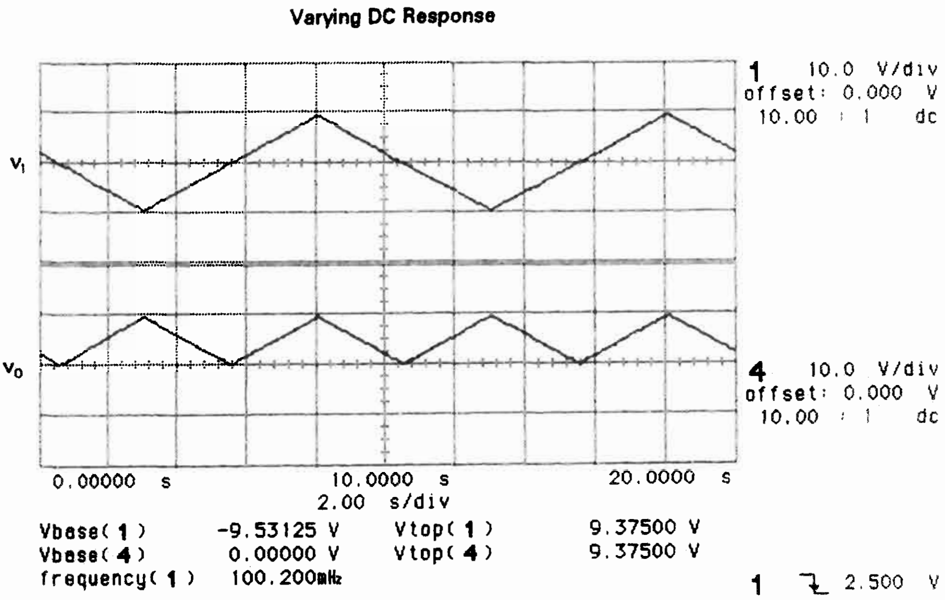
Sinewave Response



```
Vbase( 1 )       -10.0000 V     Vtop( 1 )      9.84375 V
Vbase( 4 )       -312.500mV     Vtop( 4 )      9.84375 V
frequency( 1 )   100.200kHz
```

(a)

FIGURE 9.13 Oscilloscope displays showing the performance of the absolute value circuit shown in Figure 9.12. (Test equipment courtesy of Hewlett-Packard Company.)



(b)

FIGURE 9.13 *Continued*

9.5 SIGN CHANGING CIRCUIT

A sign changing circuit is a simple, but important, member of the arithmetic circuits family. Many arithmetic operations require sign or polarity changes. A sign changing circuit, then, is one that can either invert a signal or, alternately, pass it through without inversion. A specific application that could utilize a sign changing circuit is a combination add/subtract circuit. You will recall the basic rule for algebraic subtraction, "... change the sign of the subtrahend and then proceed as in addition." We could, therefore, route one of the adder inputs through a sign changing circuit that could invert or not invert the signal to subtract or add, respectively.

9.5.1 Operation

The schematic diagram of a sign changing circuit is shown in Figure 9.14. The single-pole double-throw (SPDT) switch is generally an analog switch controlled by another circuit (e.g., a microprocessor system). When the switch is in the upper position, the amplifier is configured as a basic inverting amplifier. The gain ($A_V = -1$) is determined by the ratio of R_1 and R_2.

When the switch is moved to the lower position, the circuit is configured as a simple voltage follower ($A_V = 1$). Resistor R_3 determines the input impedance of the circuit. Its value can be selected such that the input impedance offered by the sign changer is the same in both modes, allowing the circuit to present a constant load on the driving stage. Resistor R_1 is open-circuited in the noninverting mode and has no effect on circuit operation.

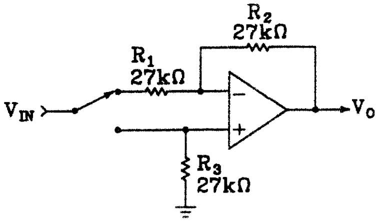


FIGURE 9.14 A sign changing circuit allows selectable inversion.

9.5.2 Numerical Analysis

The numerical analysis for this circuit must be done in two stages (one for each position of the switch). Each of these calculations is literally identical to the calculations presented in Chapter 2 for inverting and noninverting amplifiers, so they are not repeated here.

9.5.3 Practical Design Techniques

Let us now design a simple sign changer circuit that satisfies the following design requirements:

1. Input impedance	≥47 kilohms
2. Frequency range	0–8.5 kilohertz

Compute R_1 and R_2. The value of R_1 is established by the input impedance requirement. Its value is computed with Equation (2.7).

$$R_1 = Z_I \geq 47\ k\Omega$$

Let us choose a standard value of 100 kilohms. Resistor R_2 will be the same value as R_1, since we want the circuit to have a voltage gain of −1.

Compute R_3. The value of R_3 should be equal to the value of R_1 so that we can maintain a constant input impedance for both modes. Therefore,

$$R_3 = R_1 = 100\ k\Omega$$

It should be noted that this selection does not minimize the effects of input bias current. The ideal value for R_3 is different for the two modes if we want to minimize those effects.

Select the Op Amp. We will select the op amp on the basis of bandwidth and slew rate. The minimum unity gain frequency is found as

$$f_{UG} = bwA_V = 8.5\ kHz \times 1 = 8.5\ kHz$$

This value should be doubled (i.e., 17 *kHz*) for critical applications. The minimum required slew rate (based on a full output swing) is calculated with Equation (2.11).

$$\textit{slew rate} = \pi f V_O(\max) = 3.14 \times 8.5\ kHz \times 26\ V = 0.694\ V/\mu s$$

The bandwidth specification can be satisfied by most any op amp. The required slew rate, however, exceeds the 0.5-volts-per-microsecond rating for the standard 741. Let us plan to use an MC1741SC device, which satisfies both bandwidth and slew rate requirements.

The schematic of our sign changing circuit is shown in Figure 9.15. Its performance is evident from the oscilloscope displays shown in Figure 9.16. The waveforms in Figure 9.16(a) show the circuit's performance in the invert mode. Figure 9.16(b) shows the circuit operated in the noninvert mode.

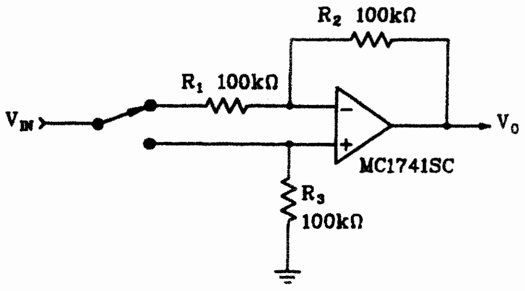


FIGURE 9.15 Final design of an 8.5-kilohertz sign changing circuit.

Invert Mode

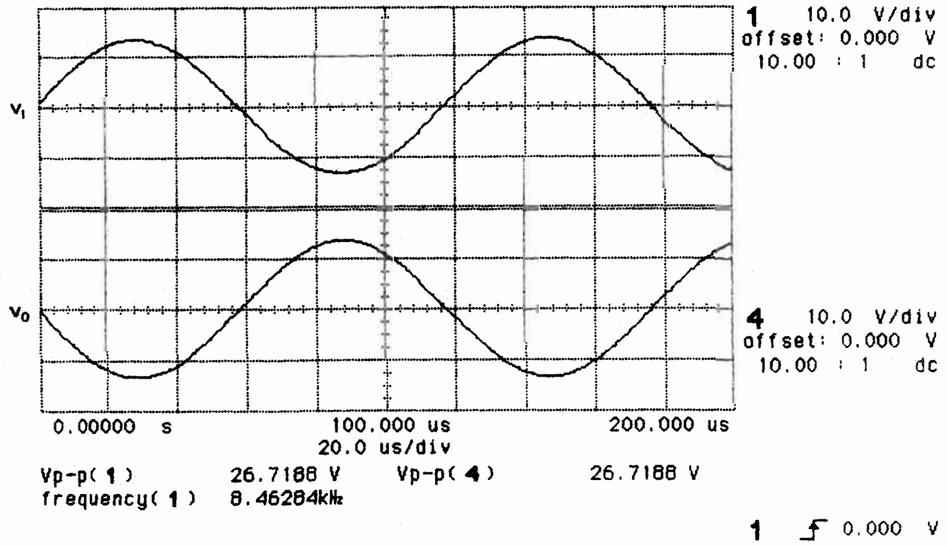
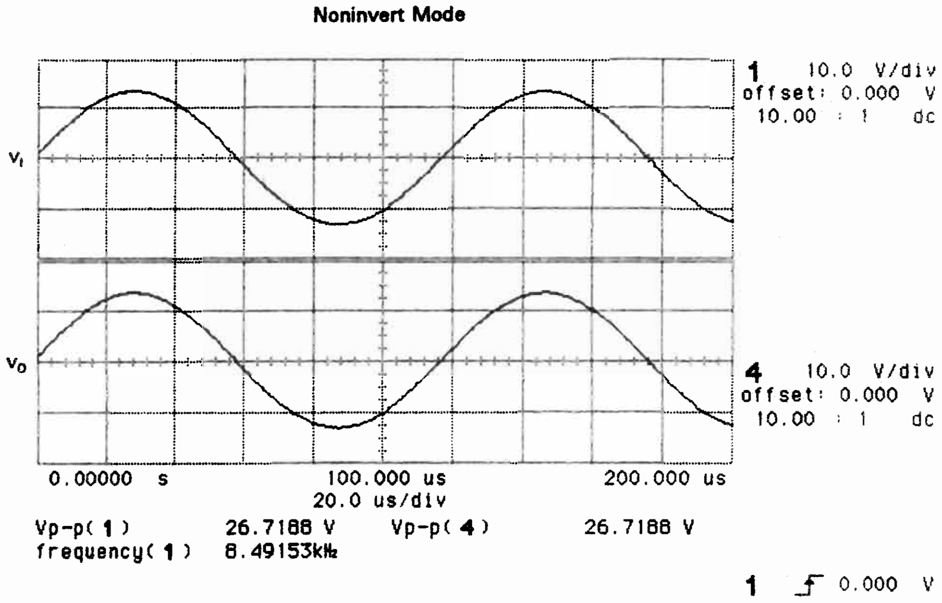


FIGURE 9.16 Oscilloscope displays showing the actual performance of the sign-changing circuit shown in Figure 9.15. (Test equipment courtesy of Hewlett-Packard Company.) *(continued)*



(b)

FIGURE 9.16 *Continued*

9.6 TROUBLESHOOTING TIPS FOR ARITHMETIC CIRCUITS

Most of the arithmetic circuits presented in this chapter are electrically similar to other amplifier circuits previously studied; it is the component values and intended application that cause them to be classified as *arithmetic.* With this in mind, all of the troubleshooting tips and procedures previously discussed for similar circuits are applicable to the companion arithmetic circuits and will not be repeated here.

Proper operation of the arithmetic circuits presented in this chapter requires accurate component values. It is common to use precision resistors to obtain the desired performance. If a component changes value, its effects may be more noticeable in the arithmetic circuits than in similar, nonarithmetic circuits previously discussed. The very nature of the arithmetic circuit generally implies a higher level of required accuracy than that for a simple amplifier. Thus, the probability of problems being caused by component variations is greater with arithmetic circuits.

To diagnose a problem caused by a component variation, it is helpful to apply your theoretical understanding of the circuit to minimize the number of suspect components. By applying various combinations of signals and monitoring the output signal, you can usually identify a particular input that has an incorrect response. If, on the other hand, all of the inputs seem to be in error (e.g., shifted slightly), then the problem is most likely a component that is common to all inputs (e.g., the feedback resistor or op amp).

If your job requires you to do frequent maintenance on arithmetic circuits, it is probably worth your while to construct a test jig to aid in diagnosing faulty circuits. The test jig could consist of a number of switch-selectable voltages applied to several output jacks, and the voltages should be accurate enough to effectively test the particular class of circuits being evaluated. The jig, coupled with a table showing the performance of a known good circuit, can be used to very quickly isolate troubles in arithmetic circuits. Of course, this entire test fixture could easily be interfaced to a computer for automatic testing and comparison.

If the circuit seems to work properly in the laboratory, but consistently goes out of tolerance when placed in service, you might suspect a thermal problem. Nearly all of the components in all of the circuits are affected by temperature changes. Short of providing a constant temperature environment, your only options for improving performance under changing temperature conditions are these:

1. Locate a defective component.
2. Substitute compatible components with tighter tolerances.
3. Redesign the circuit using a different technique.

You can artificially simulate temperature changes to a single component by spraying a freezing mist on it. Sprays of this type are available at any electronics supply store. Although every component you spray may cause a shift in operation, an abrupt or dramatic or erratic response from a particular one may indicate a failing part.

There are numerous choices for all of the components in the circuits presented in this chapter. Improved immunity to temperature variations can often be obtained simply by substituting components with more stringent tolerances. Resistors with a 5-percent rating can be replaced, for example, with 1-percent resistors. Similarly, a general-purpose op amp can be replaced with a pin-compatible op amp having lower bias currents, noise, or temperature coefficients.

Finally, if items 1 and 2 in the list above do not resolve a particular thermal problem, then redesign may be in order. Frequently, there is a trade-off between circuit simplicity and circuit stability. Achieving rock-solid stability often requires a step increase in circuit complexity.

REVIEW QUESTIONS

1. Refer to Figure 9.2. What is the effect on circuit operation if resistors R_3 to R_5 are all increased to 20 kilohms?
2. Refer to Figure 9.2. Show how the circuit can be analyzed by applying the Superposition Theorem to the input circuit.
3. Refer to Figure 9.5. What is the effect on circuit operation if resistor R_3 develops an open?
4. Refer to Figure 9.5. What is the effect on circuit operation if resistor R_2 develops an open?
5. Refer to Figure 9.9. What is the effect on circuit operation if resistor R_3 is doubled in value?
6. Refer to Figure 9.9. Describe the effect on circuit operation if resistor R_4 becomes open.
7. Will the circuit shown in Figure 9.9 still operate correctly if resistors R_4 and R_5 are both doubled in value? Explain your answer.

CHAPTER TEN

Nonideal Op Amp Characteristics

For purposes of analysis and design in the preceding chapters, we considered many of the op amp parameters to be ideal. For example, we generally assumed the input bias current to be 0, we frequently ignored output resistance, and we disregarded any effects caused by drift or offset voltage. This approach not only greatly simplifies the analysis and design techniques, but is a practical method for many situations. Nevertheless, more demanding applications require that we acknowledge the existence of certain nonideal op amp characteristics. This chapter will describe many of these additional considerations.

10.1 NONIDEAL DC CHARACTERISTICS

We will classify the nonideal characteristics of op amps into two general categories: DC and AC. Let us first consider the effects of nonideal DC characteristics.

10.1.1 Input Bias Current

As briefly noted in Chapter 1, the first stage of an op amp is a differential amplifier. Figure 10.1 shows a representative circuit that could serve as an op amp input stage. Clearly, the currents that flow into or out of the inverting (–) and noninverting (+) op amp terminals are actually base current for the internal transistors. So, for proper operation, we must always insure that both inputs have a DC path to ground. They cannot be left floating, and they cannot have series capacitors. These currents are very small (ideally 0), but may cause undesired effects in some applications.

Figure 10.2 can be used to show the effect of nonideal bias currents. It illustrates a basic op amp configured as *either* an inverting or a noninverting amplifier with the input signal removed (i.e., input shorted to ground). The direction of current flow for the bias currents and the resulting output voltage polarities are essentially arbitrary, since different op amps have different directions of current flow. However, for a given op amp, both currents will flow in the same direction

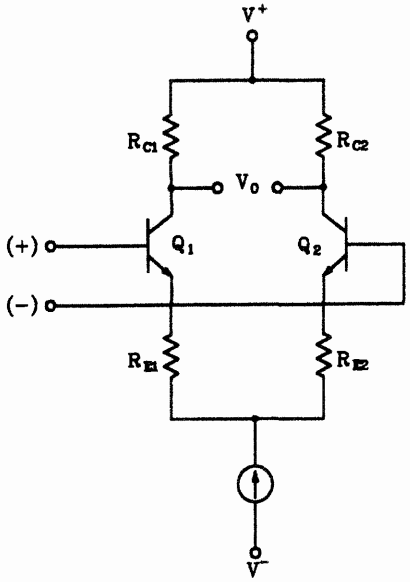


FIGURE 10.1 A representative input stage for a bipolar op amp.

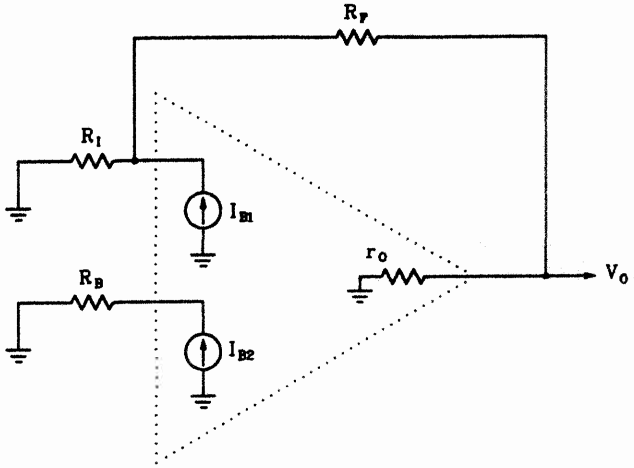


FIGURE 10.2 A model that can be used to determine the effects of bias current.

(i.e., either in or out). For our immediate purposes, let us assume that the arrows on the current sources indicate the direction of electron flow. We will now apply Ohm's Law in conjunction with the Superposition Theorem to determine the output voltage produced by the bias currents. First, the noninverting bias current (with the inverting bias current set to 0) will cause a voltage drop across R_B with a value of

$$V_{R_B} = I_{B_2} \times R_B$$

This voltage will be amplified by the noninverting gain of the amplifier and appear in the output as

$$V_{O_2} = V_{R_B}\left(\frac{R_F}{R_I} + 1\right) = I_{B_2}R_B\left(\frac{R_F}{R_I} + 1\right)$$

It should be noted that this voltage will be negative in our present example, since we assume that the electron flow was out of the input terminals.

Now let us consider the effect of the bias current for the inverting input. According to the Superposition Theorem, we must set the bias current on the noninverting input to 0. Having done this, we see that since no current is flowing through R_B there will be no voltage across it. Therefore, the voltage on the (+) input will be truly 0 or ground. Additionally, we know that the closed-loop action of the amplifier will force the inverting pin to be at a similar potential. This means that the inverting pin is also at ground potential; recall that we referred to this point as a virtual ground. In any case, with 0 volts across R_I there can be no current flow through R_I. The entire bias current for the inverting input, then, must flow through R_F (by Kirchhoff's Current Law). Since the left end of R_F is grounded and the right end is connected to the output, the voltage across R_F is equal to the output voltage. Therefore, the output voltage caused by the bias current on the inverting pin can be computed as

$$V_{O_1} = I_{B_1} \times R_F$$

Since current has been assumed to flow out of the (–) pin, we know that the resulting output voltage will be positive. Note that this is opposite the polarity of the (+) input.

Now, continuing with the application of the Superposition Theorem, we simply combine (algebraically) the individual voltages computed above to determine the net effect of the two bias currents. Since the polarities of output voltage caused by the two bias currents are opposite, the net output voltage must be

$$V_O = V_{O_1} - V_{O_2}, \text{ or}$$

$$V_O = I_{B_1}R_F - I_{B_2}R_B\left(\frac{R_F}{R_I} + 1\right)$$

The manufacturer does not generally provide the individual values of both bias currents. Rather, the bias current (I_B) listed in the specification sheet is actually an average of the two. In general, the two currents are fairly close in value, so if we assume that the two currents are equal, the preceding equation becomes

$$\boxed{V_O = I_B\left[R_F - R_B\left(\frac{R_F}{R_I} + 1\right)\right] \qquad (10.1)}$$

Thus, to estimate the output voltage caused by the bias currents in a particular amplifier circuit, we apply Equation (10.1). As an example, let us estimate the output voltage caused by the bias currents for the inverting amplifier circuit shown in Figure 10.3.

By referring to the data sheets in Appendix 1, we can determine the maximum value of bias current for a 741 under worst-case conditions to be 1500 nanoamperes. Substituting this into Equation (10.1) gives us

$$\begin{aligned}
V_O &= I_B\left[R_F - R_B\left(\frac{R_F}{R_I}+1\right)\right]\\
&= 1500\ nA\left[120\ k\Omega - 68\ k\Omega\left(\frac{120\ k\Omega}{27\ k\Omega}+1\right)\right]\\
&= -375.33\ mV
\end{aligned}$$

Now a good question to ask is how we design our circuits to minimize the effects of op amp bias currents. We prefer to have 0 volts in the output as a result of the bias currents, so let us set Equation (10.1) equal to 0 and then manipulate the equation.

$$\begin{aligned}
0 &= I_B\left[R_F - R_B\left(\frac{R_F}{R_I}+1\right)\right]\\
&= R_F - R_B\left(\frac{R_F}{R_I}+1\right)\\
R_F &= R_B\left(\frac{R_F}{R_I}+1\right)\\
R_B &= \frac{R_F}{\frac{R_F}{R_I}+1}\\
&= \frac{R_F}{\frac{R_F+R_I}{R_I}}\\
&= R_F\left(\frac{R_I}{R_I+R_F}\right)\\
&= \frac{R_F R_I}{R_F+R_I}
\end{aligned}$$

The final outcome should be recognized as an equation for two parallel resistances. You will recall that throughout the earlier chapters we always tried to set R_B equal to the parallel resistance of R_F and R_I. This is an important result.

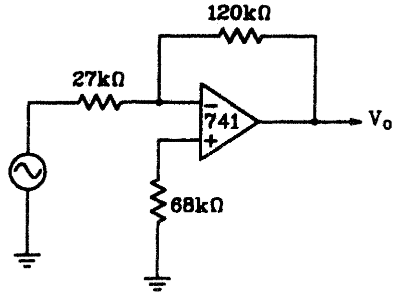


FIGURE 10.3 A basic inverting amplifier circuit.

As a final example, let us replace R_B in Figure 10.3 with the correct value and compare the results. The correct value for R_B is determined with Equation (10.2).

$$R_B = \frac{R_F R_I}{R_F + R_I} = R_F \| R_I \qquad (10.2)$$

$$R_B = \frac{R_F R_I}{R_F + R_I} = \frac{120\ k\Omega \times 27\ k\Omega}{120\ k\Omega + 27\ k\Omega} \approx 22\ k\Omega$$

We now apply Equation (10.1) to determine the resulting output voltage with the correct value of R_B.

$$\begin{aligned} V_O &= I_B\left[R_F - R_B\left(\frac{R_F}{R_I} + 1\right)\right] \\ &= 1500\ nA\left[120\ k\Omega - 22\ k\Omega\left(\frac{120\ k\Omega}{27\ k\Omega} + 1\right)\right] \\ &= -333\ \mu V \end{aligned}$$

This, as you can see, is an improvement of over 1000 times, but you should realize that these calculations were based on the assumption that the two bias currents are identical. And while they are close, they are not truly equal. The difference between them is the subject of the next section.

10.1.2 Input Offset Current

The value of bias current listed in the manufacturer's data sheet is the average of the two individual currents. The value listed in the manufacturer's data sheet as input offset current is the difference between those currents, which is always less than the individual currents. In the case of the standard 741, the worst-case input offset current is listed as 500 nanoamperes (compared to 1500 nA for bias current).

The typical values for these currents at room temperature are 20 nanoamperes and 80 nanoamperes for input offset current and input bias current, respectively.

While deriving Equation (10.1), we generated the following intermediate step:

$$V_O = I_{B_1}R_F - I_{B_2}R_B\left(\frac{R_F}{R_I} + 1\right)$$

Now, from this point let us assume that R_B is selected to be equal to the parallel combination of R_F and R_I as expressed in Equation (10.2). If we substitute this equality into this equation and then manipulate the equation, we can produce a useful expression.

$$\begin{aligned} V_O &= I_{B_1}R_F - I_{B_2}\frac{R_F R_I}{R_F + R_I}\left(\frac{R_F}{R_I} + 1\right) \\ &= I_{B_1}R_F - \left[\frac{I_{B_2}R_F^2 + I_{B_2}R_F R_I}{R_F + R_I}\right] \\ &= I_{B_1}R_F - I_{B_2}R_F \\ &= R_F\left(I_{B_1} - I_{B_2}\right) \end{aligned}$$

Since the quantity $I_{B_1} - I_{B_2}$ is the very definition of input offset current, we can make this substitution and obtain Equation (10.3).

$$V_O = R_F I_{IO} \tag{10.3}$$

As long as we select the correct value for R_B, we can use the simplified Equation (10.3) to determine the output voltage caused by op amp input currents. In the case of the standard 741 shown in Figure 10.3 (but with the correct value for R_B), the worst-case output voltage caused by offset current is

$$V_O = 120\ k\Omega \times 500\ nA = 60\ mV$$

A more likely result can be found by using the typical value of offset current at room temperature. That is,

$$V_O = 120\ k\Omega \times 20\ nA = 2.4\ mV$$

10.1.3 Input Offset Voltage

Input offset voltage is another parameter listed in the manufacturer's data sheet. Like the bias currents, it produces an error voltage in the output. That is, with 0 volts applied to the inputs of an op amp, we expect to find 0 volts at the output. In fact, we will find a small DC offset present at the output. This is called the *output* *offset voltage* and is a result of the combined effects of bias current (previously discussed above) and input offset voltage.

The error contributed by input offset voltage is a result of DC imbalances within the op amp. The transistor currents (see Figure 10.1) in the input stage may not be exactly equal because of component tolerances within the integrated circuit. In any case, an output voltage is produced just as if there were an actual voltage applied to the input of the op amp. To facilitate the analysis of the problem, we model the circuit with a small DC source at the noninverting input terminal (see Figure 10.4). This apparent source is called the input offset voltage, and it will be amplified and appear in the output as an error voltage. The output voltage caused by the input offset voltage can be computed with our basic gain equation.

$$V_O = V_{IO}\left(\frac{R_F}{R_I} + 1\right)$$

The manufacturer's data sheet for a standard 741 lists the worst-case value for input offset voltage as 6 millivolts. In the case of the circuit shown in Figure 10.4, we could compute the output error voltage caused by the input offset voltage as follows:

$$V_O = 6\ mV\left(\frac{180\ k\Omega}{56\ k\Omega} + 1\right) = 25.29\ mV$$

The polarity of the output offset may be either positive or negative. Therefore, it may add or subtract from the DC offset caused by the op amp bias currents. The worst-case output offset voltage can be estimated by assuming that the output voltages caused by the bias currents and the input offset voltage are additive. In that case, the resulting value of output offset voltage can be found as

$$\boxed{V_{OO} = R_F I_{IO} + V_{IO}\left(\frac{R_F}{R_I} + 1\right) \qquad (10.4)}$$

Most op amps, including the 741, have provisions for nulling or canceling the output offset voltage. Appendix 4 shows the recommended nulling circuit for an

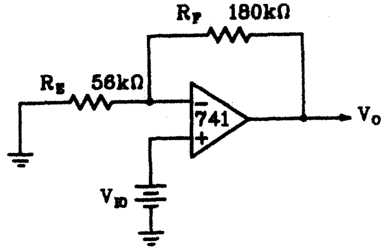


FIGURE 10.4 The input offset voltage contributes to the DC offset voltage in the output of an op amp.

MC1741SC. It consists of a 10-kilohm potentiometer connected between the offset null pins (1 and 5) of the op amp. The wiper arm of the potentiometer connects to the negative supply voltage. The amplifier is connected for normal operation (excluding any DC input signals), and the potentiometer is adjusted to produce 0 volts at the output of the op amp. You should realize, however, that this only cancels the output offset voltage at one particular operating point. With temperature changes or simply over a period of time, the circuit may drift and need to be readjusted. Nevertheless, it is an improvement over a circuit with no compensation.

10.1.4 Drift

Drift is a general term that describes the change in DC operating characteristics with time and/or temperature. The temperature drift for input offset current is expressed in terms of *nA/°C,* and the drift for input offset voltage is expressed in terms of $\mu V/°C$. The temperature coefficient of each of these quantities varies over the temperature range, and this variation may even include a change in polarity of the temperature coefficient. The maximum drift may be provided in tabular form by some manufacturers, but more meaningful data is available when the manufacturer provides a graph showing the response of input offset current and input offset voltage to changes in temperature. The data sheet in Appendix 1 is essentially a compromise between these two methods. Here the manufacturer has provided the values of input offset current and input offset voltage at room temperature and at the extremes of the temperature range.

The usual way to reduce the effects of drift is to select an op amp that has a low temperature coefficient for these parameters. Additionally, in certain critical applications some success can be achieved by including a thermistor network as part of the output offset voltage compensation network.

10.1.5 Input Resistance

An ideal op amp has an infinite input resistance. However, for practical op amps the input resistance is lower but still very high. The errors caused by nonideal input resistance in the op amp do not generally cause significant problems, and what problems may be present can generally be minimized by ensuring that the following conditions are satisfied:

1. The differential input resistance should be at *least* 10 times the value of feedback resistor for inverting applications.
2. The differential input resistance should be at *least* 10 times the values of the feedback and source resistances for noninverting applications.

In most cases, these requirements are easily met. In more demanding applications, the designer may select a FET input op amp. The MC34001 op amp made by Motorola, Inc., is an example of this type; it provides an input resistance of 10^{12} ohms and is pin-compatible with the standard 741 device.

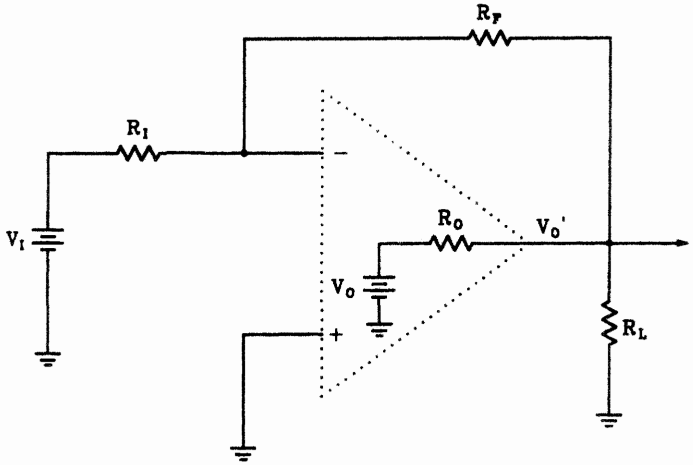


FIGURE 10.5 The effect of op amp output resistance (R_O) is to reduce the output voltage.

10.1.6 Output Resistance

Figure 10.5 shows a circuit model that can be used to understand the effects of non-0 output resistance in an op amp. Considering that the (–) input pin is a virtual ground point, we find that R_F and R_L are in parallel with each other. This combination forms a voltage divider with the series output resistance (R_O). The actual output voltage (V_O') will be somewhat less than the ideal output voltage (V_O).

The numerical effect of R_O can be determined by applying the basic voltage divider equation.

$$V_O' = V_O\left(\frac{R_F \| R_L}{R_F \| R_L + R_O}\right)$$

$$= V_O\left(\frac{\dfrac{R_F R_L}{R_F + R_L}}{\dfrac{R_F R_L}{R_F + R_L} + R_O}\right)$$

$$= \frac{V_O}{1 + R_O\left(\dfrac{R_F + R_L}{R_F R_L}\right)}$$

Now, as long as the following condition is maintained,

$$R_O\left(\frac{R_F + R_L}{R_F R_L}\right) \ll 1$$

the actual output voltage will show very little loading. In practice, this condition is generally easy to satisfy. In most cases, the maximum output current of the op amp will be exceeded before the output resistance becomes a problem.

10.2 NONIDEAL AC CHARACTERISTICS

10.2.1 Frequency Response

The effects of limited bandwidth have been discussed in several of the earlier chapters with reference to specific circuits. In general, the open-loop DC gain of an op amp is extremely high (typically well over 200,000). However, as the frequency of operation increases, the gain begins to fall off. At some point, the open-loop gain reaches 1. We call this the *unity gain frequency,* which is also referred to as the *gain bandwidth product.*

When the op amp is provided with negative feedback, the closed-loop gain is less than the open-loop gain. As long as the closed-loop gain is substantially less than the open-loop gain (at a given frequency), then the circuit is relatively unaffected by the reduced open-loop gain. However, at frequencies that cause the open-loop gain to approach the expected closed-loop gain, the actual closed-loop gain also begins to fall off.

We can estimate the highest operating frequency for a particular closed-loop gain as follows:

$$bw = \frac{unity\ gain\ frequency}{closed\text{-}loop\ gain}$$

This is adequate for many, if not most, applications, but it ignores the fact that the closed-loop gain falls off more rapidly as it approaches the open-loop curve. In fact, when the circuit is operated at the frequency computed, the response will be about 3 dB below the ideal voltage gain. If this 3-dB drop is unacceptable for a particular application, then the gain must be reduced (or an op amp with a higher gain bandwidth product used).

10.2.2 Slew Rate

In order to provide high-frequency stability, op amps have one or more capacitors connected to an internal stage. The capacitor may be internal to the op amp (internally compensated), or it may be added externally by the designer (externally compensated) (Section 10.2.4 discusses compensation in greater detail). In either case, this compensating capacitance limits the maximum rate of change that can occur at the output of the op amp. That is, the output voltage can only change as fast as this capacitance can be charged and discharged. The charging rate is determined by two factors:

1. Charging current
2. Size of the capacitor

The charging current is determined by the design of the op amp and is not controllable by the user. In the case of internally compensated op amps, the value of capacitance is also fixed. The user does have control over the capacitance values for externally compensated op amps. The smaller the compensating capacitor, the wider the bandwidth and the faster the slew rate. Unfortunately, the price paid for this increased performance is a greater amplification of noise voltages and a greater tendency for oscillations.

Since slew rate is, by definition, a measure of volts per second, the severity of problems caused by limited slew rates is affected by both signal amplitude and signal frequency. We can determine the largest output voltage swing for a given slew rate and operating frequency by applying Equation (2.11).

$$v_O(\mathrm{max}) = \frac{slew\ rate}{\pi f}$$

Of course, we can also transpose this equation to determine the highest operating frequency for a given output amplitude.

10.2.3 Noise

The term *noise*, as used here, refers to undesired voltage (or current) fluctuations created within the internal stages of the op amp. Although there are many internal sources of noise, and several types, it is convenient to view the noise sources collectively as a single source connected to the noninverting input terminal. This approach to noise analysis is shown in Figure 10.6.

The value of the equivalent noise source shown in Figure 10.6 is labeled by some manufacturers as *equivalent input noise*. The gain given to this noise voltage is computed with our basic noninverting amplifier gain equation, which is

$$v_O = V_N\left(\frac{R_F}{R_I} + 1\right)$$

It is important to note, however, that R_I for the purposes of calculating noise gain is the total resistance from the inverting pin to ground. This has particular significance in the case of a multiple-input summing amplifier, where the R_I value is actually the parallel combination of all input resistors. Thus, the noise gain of the circuit is higher than any of the individual gains.

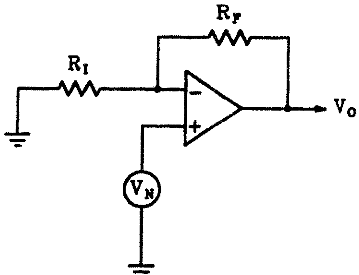


FIGURE 10.6 All of the internal noise sources in an op amp can be viewed as a single source (V_N) applied to the noninverting input.

Another important aspect of noise gain is apparent when capacitance is used in the input circuit (e.g., the differentiator circuit). By having a capacitance in series with the input terminal (–), we cause the effective R_I to decrease at higher frequencies, thus increasing the noise gain of the circuit.

The data sheet for the standard 741 provided in Appendix 1 shows one manufacturer's method of providing noise specifications for an op amp. The graph labeled "Output Noise versus Source Resistance" is particularly useful. Here the manufacturer is indicating the total RMS output noise for various gains and various source resistances. The source resistor always generates thermal noise that increases with resistance and temperature. For low values of source resistance (below 1.0 kΩ), the op amp noise is the primary contributor to overall output noise. Thus, the curves remain fairly flat for various source resistance values. As the source resistance is increased beyond 10 kilohms, its noise begins to swamp out the internal op amp noise and we begin to see a steady rise in overall noise with source resistance increases.

The graph labeled "Spectral Noise Density" also provides us with greater insight into the noise characteristics of the 741. This graph indicates the relative magnitudes of noise signals at various frequencies. In particular, notice that at frequencies above 1.0 kilohertz, the distribution of noise voltage is fairly constant. This flat region is largely caused by the noise generated in the source resistance. Much of the internal op amp noise decreases with increasing frequency. By the time we reach 1.0 kilohertz, this internal noise contributes little to the overall noise signal, but below 1.0 kilohertz the overall noise amplitude increases sharply as frequency is decreased. This increase is largely caused by increased internal op amp noise and can present problems in DC amplifiers.

There are several things we can do to minimize the effects caused by noise voltages. First, we can take steps to minimize the noise gain of the circuit. This means avoiding the use of large values of feedback resistance (R_F) and small values of input resistance (R_I). Unfortunately, the gain of the circuit for normal signals determines the ratio of these two components, but if we bypass R_F with a small capacitor, we can cause the noise gain to decrease at frequencies beyond the normal operating range of the circuit. In other words, the normal input signals will see the bypass capacitor as an open and will be unaffected, but the noise signals will see the bypass capacitor as a low impedance and reduce the overall noise gain of the circuit.

A second way to minimize the effects of noise in an op amp circuit is to ensure that the resistance between the inverting input and ground, and between the noninverting input and ground, are equal. You will recall that this same procedure helped us minimize the effects of input offset current.

Third, since the noise generated by resistors increases with resistance (actually $\sqrt{R}$), we should avoid large values of resistance when noise is potentially a problem.

Finally, we can reduce the op amp's contribution to overall output noise by selecting an op amp that is optimized for low-noise operation. The OP-27 op amp manufactured by Motorola, Inc., for example, is called an "ultra-low" noise device. It generates only 3.0 nanovolts of RMS noise at 1.0 kilohertz.

10.2.4 Frequency Compensation

We know from the study of oscillators that the two primary criteria for oscillation are in-phase (or 360°) feedback and a gain of at least unity at the feedback frequency.

The op amp has a varying gain depending upon the operating frequency, but the gain requirement for oscillation is certainly a possibility.

Additionally, the op amp inherently has a 180° phase shift between its inverting input and the output by virtue of its operation. Now if we provide an additional 180° phase shift **and** provide a loop gain of at least unity, we will have built an oscillator.

In an earlier chapter, we provided this extra phase shift externally at a specific frequency to construct an op amp oscillator. All of the internal stages of an op amp also have certain frequency and phase characteristics. As frequency increases, the cumulative phase shift of these internal stages also increases. If, at some frequency, the total phase shift reaches 360° (or 0°) and **at the same time** we have a loop gain of at least unity, the circuit will oscillate even though that may not be the intended behavior.

Principles of Frequency Compensation. So far in the text we have primarily focused on the frequency characteristics of the op amp with only occasional reference to the phase characteristics. Figure 10.7 shows a simple RC circuit and graphs showing its frequency and phase performance. Table 10.1 shows this same data in tabular form.

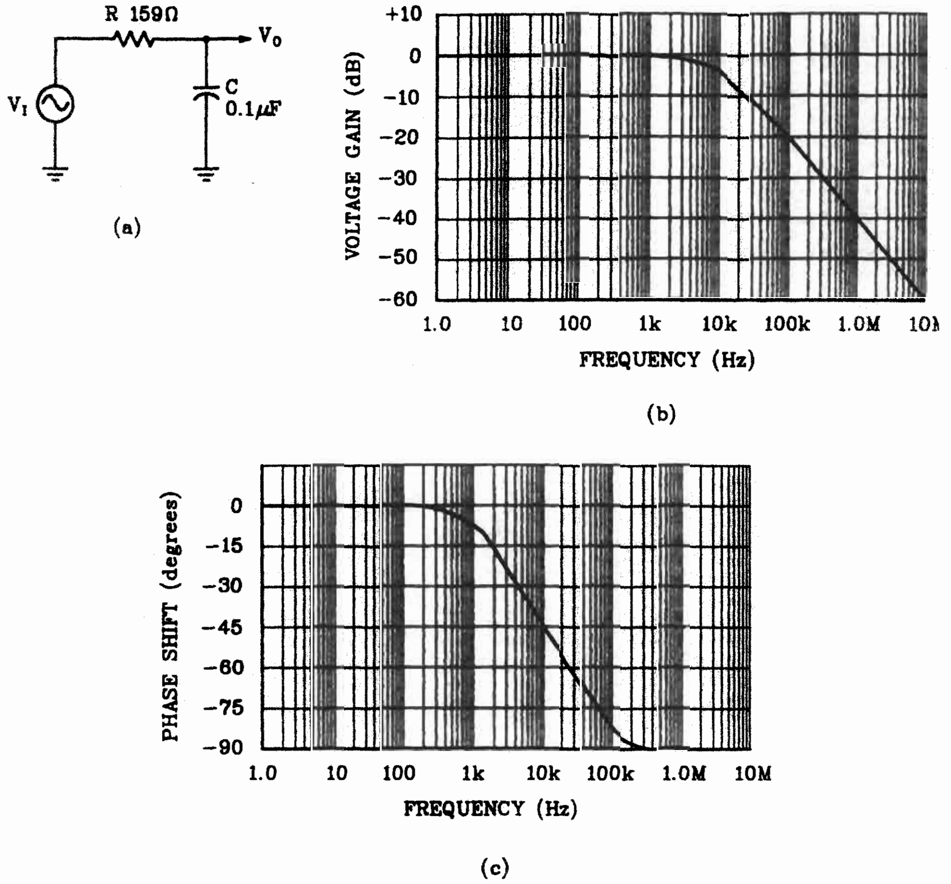


FIGURE 10.7 The frequency/phase response of a simple RC circuit.

There are several things to be observed from these data. First note that the break (or cutoff) frequency occurs at 10 kilohertz. At this frequency, $X_C = R$, the voltage gain is 0.707, and the phase shift is about 45°. Now notice that if we are at least a decade lower than the break frequency, the following occurs:

1. Voltage gain remains fairly constant (near unity).
2. The dB-per-decade drop in output voltage is very slight.
3. The phase shift is near 0° (<6°).

As the cutoff frequency is passed things change. By the time we are one decade above the cutoff frequency and continuing beyond, the following occurs:

1. Voltage gain decreases by a factor of 10 for each decade increase in frequency.
2. The dB-per-decade drop continues at about –20 dB per decade.
3. The phase shift is near 90° (>84°).

If we add a second RC section to the circuit shown in Figure 10.7, these effects are magnified. That is, for frequencies well below **both** break frequencies, the circuit behaves as described for low frequencies. For frequencies greater than the break frequency of one RC section, but less than the second, the circuit response is as described for high frequencies. Finally, when the operating frequency is higher than **both** break frequencies, the following effects occur:

1. Voltage gain decreases by a factor of 100 for each decade increase in frequency.
2. The dB-per-decade drop continues at –40 dB per decade.
3. The phase shift is near 180°.

This two-stage response is shown graphically in Figure 10.8 as a solid line. The dotted curves represent the responses of the individual RC sections. A similar cumulative effect occurs for each subsequent RC section added.

TABLE 10.1

Frequency (Hz)	*Voltage Gain*	*dB per Decade*	*Phase Shift*
1	1	—	–0.0057°
10	0.99999	–0.00000478	–0.0541°
100	0.99995	–0.000429	–0.5701°
1000	0.99505	–0.0427	–5.7°
10,000	0.70763	–2.964	–44.96°
100,000	0.09965	–17.046	–84.29°
1,000,000	0.01001	–19.979	–89.43°
10,000,000	0.001001	–20.022	–89.95°

As briefly mentioned earlier in this section, each of the internal stages of an op amp have frequency and phase characteristics similar to the RC sections presented. Figure 10.9 shows the open-loop frequency response of a hypothetical amplifier **with no frequency compensation.** This response presents us with "good news" and "bad news." The good news is that we have a substantial increase in bandwidth relative to a compensated op amp (e.g., the standard 741 shown as a dotted curve). The bad news is that the multiple break frequencies will certainly cause greater than 180° of phase shift. This internal shift coupled with the inherent 180° shift from the inverting input terminal will make this particular op amp very prone to oscillation. Now, let us determine how prone.

If we superimpose the closed-loop gain response on the open-loop response originally shown in Figure 10.9, we get Figure 10.10, where the closed-loop responses for several gains are shown. Now, the important characteristic for stability (i.e., no oscillations) is summarized in the following statement:

To ensure against oscillations, the intersection of the closed-loop gain and the open-loop gain curves must occur with a *net* slope of less than 40 dB per decade.

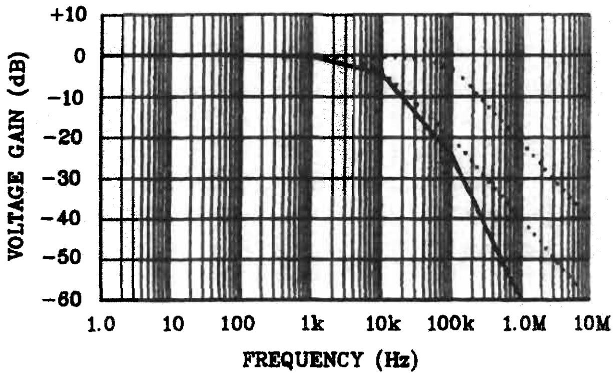


FIGURE 10.8 A two-stage RC filter has a cumulative effect.

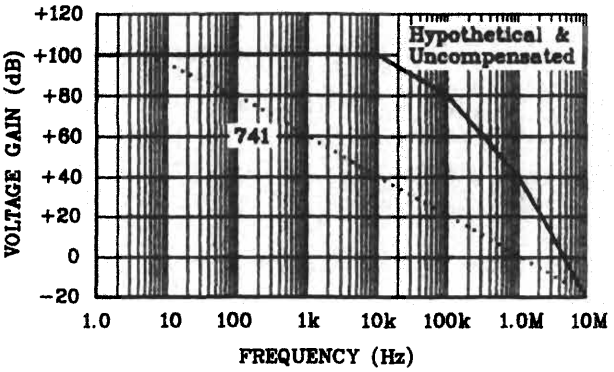


FIGURE 10.9 An uncompensated frequency response provides both "good" and "bad" news.

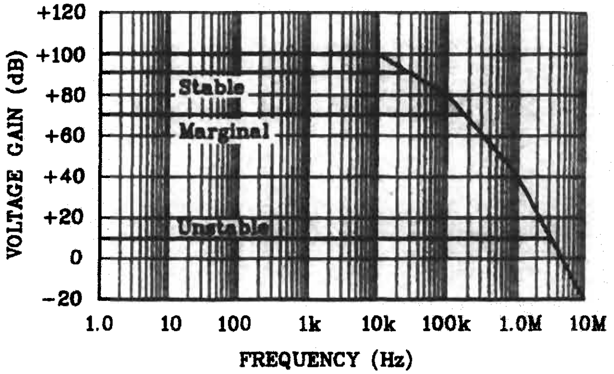


FIGURE 10.10 To ensure against oscillations, the intersection of the closed-loop gain and the open-loop gain curves must occur with a net slope of less than 40 dB per decade.

If this rule is violated, unstable operation is assured. On the other hand, if this rule is faithfully followed, it is still possible to construct an unstable amplifier circuit. Nevertheless, it provides us with an excellent starting point. We will consider exceptions at a later point in the discussion.

One method for verifying amplifier stability using this method relies on the use of simple sketches plotted on semilog graph paper. The logarithmic scale is used to plot frequency, and the linear scale is used to plot voltage gain expressed in dB. In this way, it is a simple matter to determine the net slope at the point of intersection between the closed- and open-loop gain curves. Although valid in concept, this method is often difficult to implement because the manufacturer may not provide adequate data regarding the uncompensated open-loop response. More often the manufacturer provides a set of curves that indicate the overall open loop response with frequency compensation (either internal or external). The designer must interpret these graphs to ascertain safe operating regions.

In any case, Figure 10.10 clearly indicates that the tendency for oscillation becomes greater as the closed-loop gain of the circuit is reduced. The worst-case gain, with regard to stability, occurs for 100-percent feedback or unity voltage gain. If the circuit is stable for unity gains, then we can be assured of stability at all other higher gains.

Internal Frequency Compensation. Many general-purpose op amps (e.g., the 741 or the MC1741SC) are internally compensated to provide stability for all gains down to and including unity. This is generally accomplished by adding a capacitor to one of the internal stages, which causes the overall response to have an additional roll-off characteristic (like adding another series RC section). The break frequency of this added circuit is chosen to be lower than all other break frequencies present in the output response, defining it as the dominant network. Figure 10.11 illustrates how the response curve of an uncompensated op amp is shifted downward by the introduction of a compensation capacitor. Notice that the effects of each of the break frequencies are still present in the response but that the amplifier gain falls below unity *before* the slope exceeds 40 dB per decade. While this does ensure maximum stability, it is clearly detrimental to the bandwidth of the amplifier.

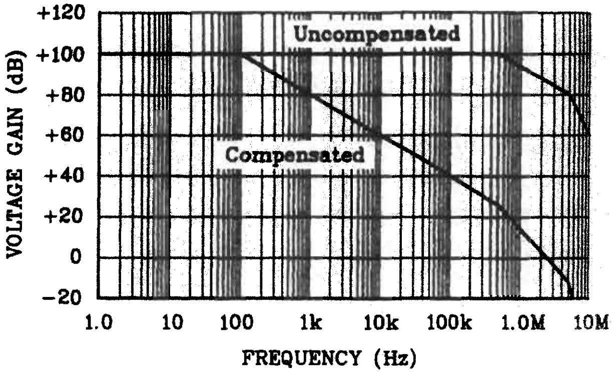


FIGURE 10.11 Adding a compensation capacitor increases stability but reduces the bandwidth of an amplifier.

The internal capacitance, called a *lag capacitor,* can be connected to any one of several points within the op amp. Since larger values of capacitance are required for lower impedance points, it is common to connect the lag capacitor at a high-impedance point in the device. Additionally, by inserting the capacitor in one of the earlier stages rather than in the output stage, it has less of a slowing effect on the slew rate. Probably the most common value of internal compensating capacitance is 30 picofarad. It can be readily identified on the simplified schematic of the standard 741 included in Appendix 1.

External Frequency Compensation. Although the inclusion of an internal compensating capacitor greatly simplifies the use of an op amp and makes it less sensitive to sloppy designs, it does cause an unnecessarily severe reduction in the bandwidth of the circuit. Alternatively, the manufacturer may elect to bring out one or more pins for the connection of an external compensating capacitor. The value of the capacitor can be tailored by the designer for a specific application.

The extreme case, of course, is to put heavy compensation on the device to make it stable all the way down to unity gain. This makes the externally compensated op amp equivalent to the internally compensated one. However, many applications do not require unity gain. In these cases, we can use a smaller compensating capacitor, which directly increases the bandwidth. So long as the closed-loop gain curve intersects the open-loop gain curve with a net slope of less than 40 dB, we will generally have a stable circuit.

The LM301A op amp is an externally compensated, general-purpose op amp. Its data sheet includes a graph that illustrates the effect on open-loop frequency response for compensating capacitors of 3 and 30 picofarads. A second graph shows the dramatic increase in large-signal frequency response obtained by using a 3-picofarad capacitor instead of a 30-picofarad. With a 30-picofarad capacitor, the full-power bandwidth is limited to about 7.5 kilohertz (nearly the same as a standard 741). By using 3-picofarad, however, the full-power bandwidth goes up to about 100 kilohertz. This can be attributed to an increased slew rate. It should be noted that 3 picofarads is a **very** small capacitance. This value can easily be obtained or even exceeded by stray wiring capacitance.

The negative side, however, is evident in the open-loop frequency response. The curve for 3 picofarads does not extend to unity gain (0 dB). That is, we must design the circuit to have substantial (e.g., 40-dB) gain to insure stability.

Feed-Forward Frequency Compensation. The lowest, and therefore most dominant, break frequency in an uncompensated op amp is generally caused by the frequency response of the PNP transistors in the input stage. Although this stage does not provide a voltage gain, the attenuation to the signal increases with frequency. By connecting a capacitor between the inverting input and the input of the next internal stage, we can effectively bypass the first stage for high frequencies, thus boosting the overall frequency response of the op amp. This technique is called *feedforward compensation.*

The manufacturer must provide access to the input terminal of the second stage in order to employ feedforward compensation. In the case of the LM301, feedforward compensation is achieved by connecting a capacitor between the inverting input and pin 1 (balance). Examination of the internal schematic will reveal that this effectively bypasses the NPN differential amplifier on the input and the associated level-shifting PNP transistors.

When feedforward compensation is used, a small capacitor must be employed to bypass the feedback resistor to ensure overall stability. The manufacturer provides details for each op amp that demonstrate the selection of component values.

The use of feedforward compensation produces all of the following effects:

1. Increased small-signal bandwidth
2. Increased full-power bandwidth
3. Improved slew rate

10.2.5 Input Resistance

Calculation of input resistance, or, more correctly, input impedance, was presented in Chapter 2. In the case of a noninverting configuration, we found that the open-loop input resistance of the op amp is magnified when the feedback loop is closed. Equation (2.29) is used to determine the effective input impedance once the loop is closed.

$$Z_I = R_{OP}A_V\left(\frac{R_I}{R_F + R_I}\right)$$

This calculation, of course, produces a very high value, which for most applications can be viewed as the ideal value of infinity.

In the case of an inverting configuration, the input impedance is generally considered to be equal to the value of the input resistor. That is, the impedance directly at the inverting input is generally considered to be 0 (virtual ground). This approximation is satisfactory for most applications. If a greater level of accuracy is needed, we can estimate the actual input impedance directly at the inverting input with Equation (10.5).

$$R_I(-) \approx \frac{R_F}{A_{OL}} \tag{10.5}$$

The total input impedance for the amplifier circuit is simply the sum of the input resistor and the value computed with Equation (10.5).

10.2.6 Output Resistance

The calculation and effects of output resistance, or impedance, were presented in Chapter 2. There it was found that the closed-loop output resistance was substantially reduced from the open-loop value. Equation (2.15) was used to estimate the closed-loop output impedance for either inverting or noninverting configurations:

$$R_O = \frac{\textit{output impedance (open-loop)} \times (R_I + R_F)}{A_{OL} R_I}$$

This is an adequate approximation for most applications. In the case of very low open-loop gains (e.g., at higher frequencies), Equation (10.6) provides a more accurate estimate of the closed-loop output impedance.

$$R_O = \frac{\textit{output impedance (open-loop)} \times (R_I + R_F)}{R_I + R_F + A_{OL} R_I} \tag{10.6}$$

In most cases, the finite output resistance has little effect on circuit operation. The maximum output current capability will generally limit the size of load resistor to a value that is still substantially larger than the output resistance of the op amp. Therefore, the voltage divider action of output resistance is minimal.

10.3 SUMMARY AND RECOMMENDATIONS

For some applications, many of the nonideal characteristics of op amps can be ignored without compromising the design. But how do you know which parameters are important under what conditions? The answer to that question is quite complex, but the following will provide you with some practical guidelines.

10.3.1 AC-Coupled Amplifiers

If a particular amplifier is AC-coupled (e.g., capacitive-, optically-, or transformer-coupled), then the nonideal DC characteristics can often be ignored. Any offsets caused by bias currents, drift, and so on, will be noncumulative; that is, the effects will be limited to the particular stage being considered and will not upset the operation of subsequent stages. Therefore, as long as the DC offset is not so great as to present problems (e.g., saturation on peak signals) in the present stage, it can probably remain uncompensated.

Frequency response and slew rate, on the other hand, are important in nearly every AC-coupled application. These parameters should be fully evaluated before a particular amplifier is selected for a given application.

Noise characteristics can often be ignored, but it depends on the application and on the amplitude of the desired signal relative to the noise signal. If the noise signal has an amplitude that is comparable to the desired signal, then the designer should take steps (discussed in an earlier section) to minimize the circuit noise response. On the other hand, if the primary signal is many times greater than the noise signal, the design may not require any special considerations with regard to noise reduction.

10.3.2 DC-Coupled Amplifiers

DC-coupled amplifiers seem to present some of the more formidable design challenges. Depending on the specific application, a DC amplifier may be affected by literally all of the nonideal op amp characteristics. This is certainly the case for a DC-coupled, low-level, wideband amplifier.

If, however, the input frequency is always very low (e.g., the output of a temperature transducer), then considerations regarding slew rate and bandwidth can often be disregarded. In these cases, the emphasis needs to be on the DC parameters such as DC offsets and drifts.

10.3.3 Relative Magnitude Rule

A good rule of thumb that is applicable to all classes of amplifiers and to all of the nonideal characteristics of op amps involves the relative magnitude of the nonideal quantity compared to the desired signal. If the nonideal value is less than 10 percent of the desired signal quantity, then ignoring it will cause less than a 10 percent error. Similarly, keeping the nonideal value below 1 percent of the desired signal will generally keep errors within 1 percent even if the nonideal quantity is disregarded.

Consider, for example, the case of input bias current. If the input bias current is approximately 700 microamperes and the input signal current is expected to be 1.2 milliamperes, then to ignore bias current would be to make a significant error because the bias current is comparable in magnitude to the desired input current.

Now suppose that the cumulative effects of bias current and input offset voltage for a particular amplifier are expected to produce a 75-millivolt offset at the output of the op amp. If the normal output signal is a 1-volt sinewave riding on a 5-volt DC level, then the undesired 75 millivolts offset can probably go unaddressed without producing any serious effects on circuit operation.

10.3.4 Safety Margins on Frequency Compensation

It is common to speak of *phase margin* and *gain margin* with reference to op amp frequency compensation. The terms describe the amount of safety margin between the designed operating point of the op amp and the point where oscillations will likely occur. The absolute limits (i.e., zero safety margin) occur when the closed-loop gain reaches unity and has a phase shift of –180°. This is the dividing line between oscillation and stable operation.

Gain margin is defined as the difference between unity and the actual closed-loop voltage gain at the point where a –180° phase shift occurs. To insure stable operation and to allow for variances in component values, the loop gain should fall to about one-third or –10 dB by the time the phase shift has reached –180°. Similarly, the phase margin is the number of degrees between the actual phase shift and –180° at the time the loop gain reaches unity. A safety margin of about 45° is recommended. If these safety margins are maintained and the capacitive loading on the output of the amplifier is light, then the circuit should be stable and perform as expected.

REVIEW QUESTIONS

1. The value of the difference between the two input bias currents of an op amp is provided by the manufacturer in the data sheet and is called ____.
2. Drift is a nonideal characteristic that primarily affects (AC-coupled/DC-coupled) op amp circuits.
3. What type of op amp would you select if a very high value of input impedance was required?
4. Noise generation in op amp circuits can be reduced by selecting very large values of resistance. (True or False)
5. If the intersection of the closed-loop gain curve and the open-loop gain curve for an op amp amplifier occurs with a net slope of 60 dB per decade, will the amplifier be stable? Explain your answer.

CHAPTER ELEVEN

Specialized Devices

This chapter will provide an overview of specialized op amps and their applications. The focus will be on identifying the primary characteristics of the various devices and on illustrating their potential applications.

11.1 PROGRAMMABLE OP AMPS

One class of specialized op amp is the micropower programmable op amp. Such devices utilize an external resistor to establish the quiescent operating current for the internal stages. That is, the internal stages are biased at a particular operating current by the selection of an external resistor. Several characteristics of the amplifier are altered by changes in the programming current (I_P):

1. DC supply current
2. Open-loop voltage gain
3. Input bias current
4. Slew rate
5. Unity gain frequency
6. Input noise voltage

Typical values of DC supply current range from less than 1 microampere to as high as 1 milliampere, and they are proportional to the value of programming current. The ability to operate at very low currents makes these devices especially attractive for battery-powered applications. Additionally, the DC voltage requirements are generally quite flexible, with ±1.2 to ±18 volts being a representative range. Here again, the programmable op amp is well suited to battery-powered applications. The DC supply current remains fairly constant with changes in supply voltage, provided the programming current is held constant.

The open-loop voltage gain increases as the programming current increases. It is reasonable to expect as much as a 100:1 change as the programming current is varied over its operating range. This characteristic can be considered an advantage (e.g., programmable voltage gain) or a disadvantage (e.g., unstable voltage gain) depending on the nature of the application.

Input bias current also increases as programming current increases. In this case, variations as great as 200:1 are reasonable over the range of programming currents. The minimum input bias current is often in the fractional nanoampere range.

The slew rate of a programmable op amp increases as programming current increases. It can also be increased by using higher DC supply voltages. As the programming current is varied over its operating range, the slew rate can be expected to vary as much as 1500:1. The upper limit is typically greater than that for the standard 741 op amp (i.e., greater than 0.5 V/μS).

The unity gain frequency (or gain bandwidth product) increases as the programming current increases. Ranges as great as 500:1 are reasonable changes to expect as the programming current is varied over its operating range. The highest unity gain frequency is typically higher than the standard 741 op amp rating (i.e, higher than 1.0 MHz).

The input noise voltage of a programmable op amp decreases as the programming current increases. Ranges of as much as 200:1 are reasonable as the programming current is varied throughout its control range.

In general, the programmable amplifier can be used for most of the applications previously discussed for general-purpose op amps, provided the appropriate specifications are adequate for a given application. The data sheets are interpreted in the same manner as for other amplifiers, with the exception that the effects of programming current are included. These effects may be shown by including multiple data sheets for different values of programming current and/or by presenting graphs that show the effects of programming current. These devices are often selected for low-power applications or for applications that require a controllable parameter. Representative devices include the MC1776 and MC3476, manufactured by Motorola, Inc.

11.2 INSTRUMENTATION AMPLIFIERS

An instrumentation amplifier is essentially a high-gain differential amplifier that is internally compensated to minimize nonideal characteristics. In particular, it has a very high common-mode rejection ratio, meaning that signal voltages that appear on both input terminals are essentially ignored and the amplifier output only responds to the differential input signal. In general, the instrumentation amplifier is designed to achieve the following:

1. Offset voltages and drifts are minimized.
2. Gain is stabilized.
3. Nonlinearity is very low.

4. Input impedance is very high.
5. Output impedance is very low.
6. Common-mode rejection is very high.

In Chapter 9, the subtractor circuit was presented. If we precede a subtractor circuit with two buffer amplifiers, we have the basis for a fundamental instrumentation amplifier circuit. This configuration is shown in Figure 11.1.

For purposes of the following discussion, let us use the values shown in Figure 11.2.

Since amplifiers A_1 and A_2 are operated with a closed, negative feedback loop, we can expect the voltages on the (–) input terminals of the amplifiers to be equal to the voltages on their (+) inputs. This means that the voltage on the upper end of R_G will be equal to the voltage applied to the (–) input of the overall instrumentation amplifier. In the present example, this voltage is +2 volts. Similarly, the voltage on the lower end of R_G will be the same as the voltage applied to the (+) input of the overall instrumentation amplifier (+2.1 volts for this example). The voltage across R_G (v_G) is the difference between the two input voltages:

$$\begin{aligned} |v_G| &= |v_1 - v_2| \\ &= |2\ V - 2.1\ V| \\ &= 0.1\ V \end{aligned}$$

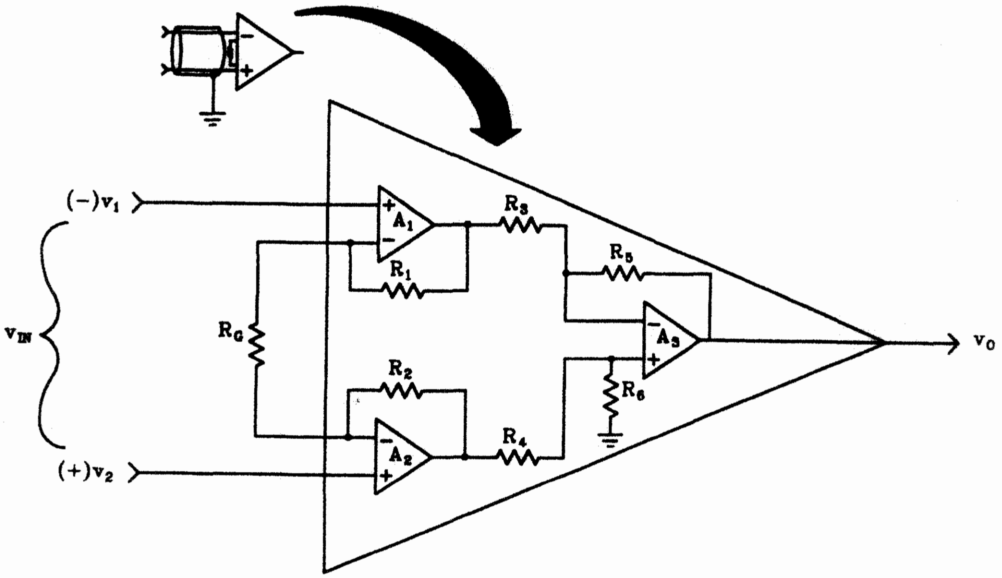


FIGURE 11.1 The basic instrumentation amplifier is essentially a subtraction circuit preceded by two buffer amplifiers.

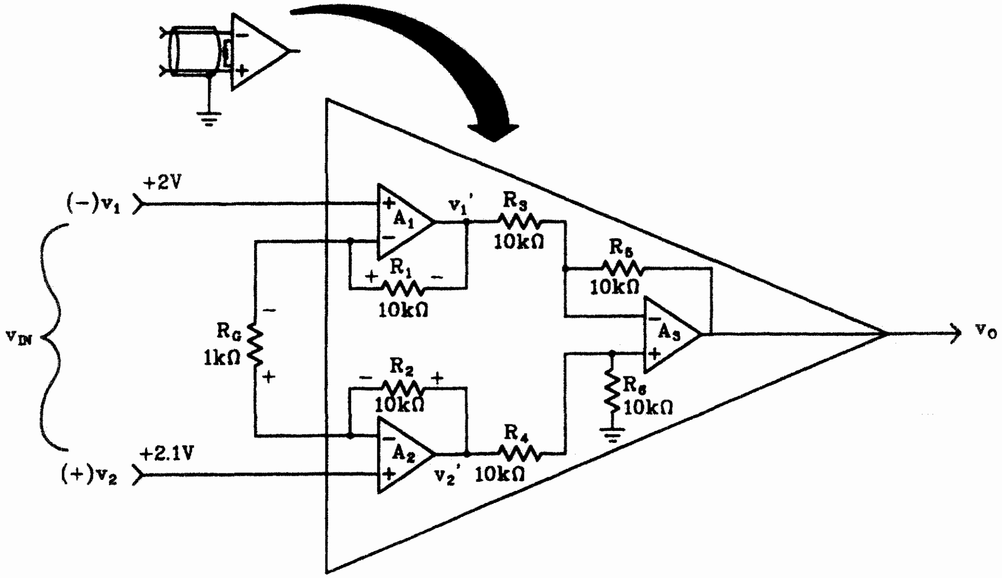


FIGURE 11.2 Basic instrumentation amplifier used for numerical analysis.

The polarity of the voltage drop depends on the relative polarities and magnitudes of the input voltages. For the present example, the lower end of R_G is the more positive, since v_2 is more positive than v_1. The current through R_G can be computed with Ohm's Law as

$$\begin{aligned} i_G &= \frac{v_G}{R_G} \\ &= \frac{0.1\ V}{1\ k\Omega} \\ &= 100\ \mu A \end{aligned}$$

Now, since none of this current can flow in or out of amplifiers A_1 and A_2 (ignoring the small bias currents), i_G must also flow through the feedback resistors of those amplifiers. Ohm's Law can be used to determine the resulting voltage drop across the feedback resistors.

$$\begin{aligned} v_{R_1} = v_{R_2} &= i_G R_1 \\ &= 100\ \mu A \times 10\ k\Omega \\ &= 1\ V \end{aligned}$$

Since electron current is flowing downward through R_G, the polarity of R_1 and R_2 will be as shown in Figure 11.2.

The voltage on the output of A_1 can be found by applying Kirchhoff's Voltage Law as follows:

$$\begin{aligned} v_1' &= v_1 - v_{R_1} \\ &= +2\ V - 1\ V \\ &= +1\ V \end{aligned}$$

Similarly, the voltage at the output of A_2 is computed as

$$\begin{aligned} v_2' &= v_2 + v_{R_2} \\ &= +2.1\ V + 1\ V \\ &= +3.1\ V \end{aligned}$$

The operation of the subtractor circuit (A_3) was discussed in Chapter 9 and will not be repeated here. The output, you will recall, is simply the difference between its inputs. In the present case, the output of A_3 will be

$$\begin{aligned} v_O &= v_2' - v_1' \\ &= 3.1\ V - 1\ V \\ &= +2.1\ V \end{aligned}$$

We can apply some basic algebraic manipulations to determine an important equation for voltage gain. We have already determined the following relationships (with polarities shown in Figure 11.2):

$$\begin{aligned} v_1' &= v_1 - v_{R_1} \\ v_2' &= v_2 + v_{R_2} \\ i_G &= \frac{v_2 - v_1}{R_G} \\ v_{R_1} &= i_G R_1 = \frac{(v_2 - v_1)R_1}{R_G} \\ v_{R_2} &= i_G R_2 = \frac{(v_2 - v_1)R_2}{R_G} \\ v_O &= v_2' - v_1' \end{aligned}$$

Substituting and simplifying gives us the following results:

$$\begin{aligned} v_O &= (v_2 + v_{R_2}) - (v_1 - v_{R_1}) \\ &= \left[v_2 + \frac{(v_2 - v_1)R_2}{R_G}\right] - \left[v_1 - \frac{(v_2 - v_1)R_1}{R_G}\right] \\ &= \left[(v_2 - v_1) + \frac{(R_1 + R_2)(v_2 - v_1)}{R_G}\right] \end{aligned}$$

Since resistors R_1 and R_2 are equal, we can replace the expression $R_1 + R_2$ with the expression $2R$. Making this substitution and simplifying gives us the following results.

$$v_O = (v_2 - v_1)\left(1 + \frac{2R}{R_G}\right)$$

Voltage gain is equal to the output voltage of an amplifier divided by its input voltage, and the input voltage to our present circuit is $v_2 - v_1$; therefore, we can now obtain our final gain equation

$$\boxed{A_V = \frac{2R}{R_G} + 1 \qquad (11.1)}$$

This shows us that the gain of the instrumentation amplifier is determined by the value of the external resistor R_G. In the case of the circuit in Figure 11.2, the voltage gain is computed as

$$\begin{aligned} A_V &= \frac{2R}{R_G} + 1 \\ &= \frac{20\ k\Omega}{1\ k\Omega} + 1 \\ &= 21 \end{aligned}$$

This, of course, correlates to our earlier discovery that an input voltage of 0.1 volts (2.1 V – 2 V) produces an output voltage of 2.1 volts.

Actual integrated instrument amplifiers may use either one or two external resistors to establish the voltage gain of the amplifier. Some devices have internal, precision resistors that can be jumpered into the circuit to obtain certain fixed gains (e.g., 10, 100, and 1000). Additionally, they will generally have other inputs for such things as trimming offset voltage and modifying the frequency response (frequency compensation).

The instrumentation amplifier is an important building block based on op amps. An understanding of its general operation coupled with the data provided by the manufacturer will allow you to use this device effectively.

11.3 LOGARITHMIC AMPLIFIERS

Although it is certainly possible to construct discrete amplifier circuits based on op amps that produce outputs that are proportional to the logarithm or antilogarithm of the input voltage, the design is very critical if stable performance is to be expected. In many cases, it is more practical to utilize integrated log and antilog amplifiers that perform these functions in a stable and predictable manner.

Whether the amplifiers are constructed from discrete components or purchased in an integrated form, the basic operation remains the same. In the case of the log amp, the output voltage is proportional to the logarithm of the input voltage. This relationship is obtained by utilizing the logarithmic relationship that exists between base-emitter voltage and emitter current in a bipolar transistor. Figure 11.3 shows a representative circuit that generates an output proportional to the logarithm of the input voltage.

The input current is computed in the same way as for a simple inverting amplifier (i.e., $i_I = v_I/R_I$). Since no substantial part of this current can flow in or out of the (–) input of the op amp, all of it continues to become the collector current of Q_1. The base-emitter voltage will be controlled by the op amp to a value that allows the collector current to equal the input current.

The relationship between collector current and base-emitter voltage is given by the following equation:

$$i_C = I_{ES}\varepsilon^{38.9v_{BE}}$$

where I_{ES} is the saturation current of the emitter-base diode, v_{BE} is the base-to-emitter voltage, and ε is the natural logarithm base (approximately 2.71828). Substituting v_I/R_I for i_C and v_O for v_{BE} gives us the following expression:

$$\frac{v_I}{R_I} = I_{ES}\varepsilon^{38.9v_O}$$

Transposing to solve for v_O gives us the expression for v_O in terms of v_I. That is,

$$\boxed{v_O \approx 0.026\ln\left(\frac{v_I}{I_{ES}R_I}\right) \qquad (11.2)}$$

Once the circuit has been designed, the only variable is input voltage (v_I). The output voltage is clearly proportional to the logarithm of the input voltage. Figure 11.4 shows the actual response of the circuit shown in Figure 11.3. The upper waveform is a linear voltage ramp that provides the input to the circuit. The logarithmic relationship is quite evident.

For more critical applications, two circuits similar to the one shown in Figure 11.3 are connected via a subtractor circuit. One of the log amps is driven by the input signal, and the input to the second log amp is connected to a reference volt-

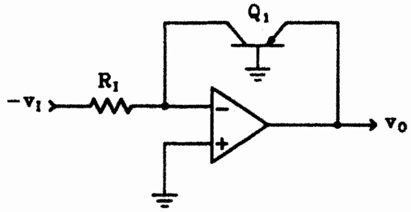


FIGURE 11.3 The basic logarithmic amplifier circuit relies on the nonlinear relationship between emitter current and base-emitter voltage in a bipolar transistor.

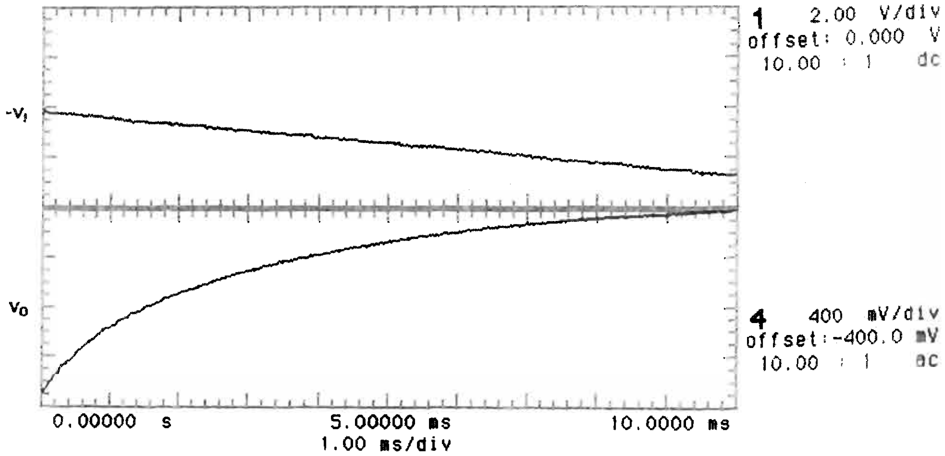


FIGURE 11.4 Oscilloscope display showing the actual behavior of the circuit shown in Figure 11.3. (Test equipment courtesy of Hewlett-Packard Company.)

age. If the transistors are similar (e.g., a matched pair integrated on the same die), then the effects of saturation current (I_{ES}) will be eliminated. This is particularly important because this parameter varies directly with temperature.

There are numerous applications for logarithmic amplifiers. One of the most common is for signal compression. By passing an analog signal through a logarithmic amplifier, a very wide range of input signals can be accommodated without saturating the output. For example, an input swing of 1.0 millivolt to 10 volts might produce a corresponding output swing of 0 to 8 volts. While this may not sound impressive at first, realize that the smaller signals will receive much greater gain than the larger signals. In this particular example, the relationship is 2 volts per decade. Thus, a 1-millivolt to 10-millivolt change on the input will cause a 0-volt–2-volt change in the output. Similarly, a 0.1-volt–1.0-volt input change will cause a 2-volt (4 V to 6 V) change in the output. Since the smaller signals are amplified more, the signal-to-noise ratio can be improved. More specifically, the smaller signals become larger relative to the noise signals. When the composite signal is subsequently translated to its original form, the noise will also be reduced.

Another application for the logarithmic amplifier is to convert a linear transducer into a logarithmic response. Optical density of microfilm, for example, is measured as the logarithm of the light that passes through the microfilm. By using a light source to shine through the microfilm and onto a photodiode whose response is linear, we have an output voltage (or current) that varies linearly with optical density. Once this waveform is passed through a logarithmic amplifier, we will have the required logarithmic relationship that represents optical density.

11.4 ANTILOGARITHMIC AMPLIFIERS

An antilogarithmic amplifier provides an output that is exponentially related to the input voltage. If, for example, a linear ramp were passed through a logarithmic amplifier (as shown in Figure 11.4), it would emerge as a logarithmic curve (similar in shape to the familiar RC time constant curve). If this logarithmic signal were then passed through an antilog amplifier, the output would again be a linear ramp. Figure 11.5 shows the basic antilog amplifier configuration.

The input current for this circuit can be estimated using the relationship between emitter-base voltage and collector current described earlier. That is,

$$i_C = I_{ES}\varepsilon^{38.9v_{BE}}$$

For proper operation of this particular circuit, the input voltage must be negative. Substituting v_I for v_{BE} gives us the following expression for input current:

$$i_I = I_{ES}\varepsilon^{38.9v_I}$$

It is important to realize that the exponent in the equation should be positive even though the actual input voltage is negative.

Since no substantial part of this current flows in or out of the (–) input of the op amp, it must all continue through R_F. The voltage drop across R_F (and therefore the output voltage) is determined with Ohm's Law.

$$\begin{aligned} v_O &= v_{R_F} = R_F i_{R_F} \\ &= R_F I_{ES}\varepsilon^{38.9v_I} \end{aligned}$$

This latter equation is repeated as Equation (11.3) and clearly shows the exponential (antilogarithmic) relationship between input voltage and output voltage.

$$\boxed{v_O = R_F I_{ES}\varepsilon^{38.9v_I} \qquad (11.3)}$$

The most obvious application for antilogarithmic amplifiers is to expand a signal that has undergone logarithmic compression. One particular application uses log/antilog circuits to reduce the number of bits needed to digitally represent an analog voltage. The signal is first compressed with a logarithmic amplifier and then converted to digital form with an analog-to-digital converter. After digital processing, the signal can be restored to proper analog form by utilizing a digital-to-analog converter followed by an antilog amplifier.

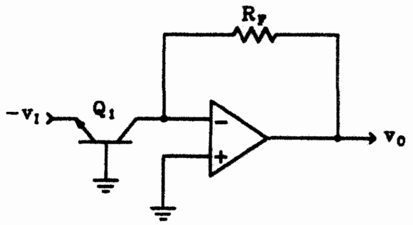


FIGURE 11.5 The basic antilogarithmic circuit configuration.

Although the average technician or engineer can easily construct one of these circuits in the laboratory and confirm logarithmic operation, the design of a reliable circuit that is minimally affected by temperature and other nonideal conditions is anything but trivial. In most cases, the designer should consider employing a logarithmic device produced commercially. Such devices contain closely matched components, track well with temperature, and are generally easy to implement. Additionally, the cost is very reasonable for many applications.

The model 755, 6-decade, high-accuracy, wideband log/antilog amplifier manufactured by Analog Devices, Inc., is an example of a commercially available logarithmic module. It requires no external components and can be configured to produce either a logarithmic or an antilogarithmic response. It comes as a module that is about 1.5 inches on a side and 0.4 inches thick.

11.5 MULTIPLIERS/DIVIDERS

Multiplier/divider circuits can be constructed from standard op amps and discrete components. However, the low cost and high performance of integrated circuit versions of these devices makes discrete designs a very unattractive alternative in most cases. In this section, we will make frequent reference to the AD532 Integrated Circuit Multiplier manufactured by Analog Devices (see Figure 11.6).

Regardless of the type of analog multiplier being considered, the device is essentially a variable gain amplifier—one of the multiplier inputs is amplified by the circuit and appears in the output, and the other is used to control the gain of the circuit. For example, if we assume that the inputs to the multiplier circuit shown in Figure 11.6 are voltages called V_X and V_Y, and we further assume that the gain of the circuit (A_V) is established by V_X, then the output of the circuit can be expressed as

$$V_O = A_V \times V_Y$$

In this form, the device appears to be a simple linear amplifier whose output is determined by the input voltage times a voltage gain. However, the voltage gain is not constant in the case of a multiplier circuit. More specifically, it is determined by the voltage applied to one of the inputs (V_X is the present example) and so can be expressed as

$$A_V = k \times V_X$$

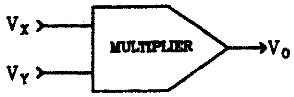


FIGURE 11.6 A basic integrated multiplier schematic representation.

where k is a constant determined by the circuit configuration. Substitution of this latter equation into the preceding equation gives us a form that reveals the multiplier action of the multiplier circuit.

$$V_O = kV_XV_Y$$

Here we can see that the output voltage is clearly a result of multiplying the input voltages together with a circuit constant. The value of the constant (k) is typically 0.1.

Since each of the input voltages may take on either of two polarities, this leads to four possible modes of operation. These four modes, or quadrants, are illustrated in Figure 11.7.

If a particular multiplier circuit is designed to accept only one polarity of input voltage on each of its inputs, then its operation will be limited to a single quadrant and it will be called a *one-quadrant multiplier.* Similarly, if a given multiplier circuit requires a single polarity on one input but accepts both polarities on the other, the device is called a *two-quadrant multiplier.* Finally, if a multiplier is designed to accept either polarity on both of its inputs, then the device is called a *four-quadrant multiplier.* The AD532 is a four-quadrant multiplier—it will accept voltages as large as ±10 volts on its inputs and produces output voltages as large as ±10 volts. The AD532 employs differential inputs and generates a single-ended output voltage described by the following expression:

$$V_{OUT} = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10}$$

Figure 11.8 shows the schematic diagram of an AD532 circuit connected as a simple multiplier. The oscilloscope display in Figure 11.9 indicates the actual behavior of the circuit.

In Figure 11.9, waveforms 1 and 2 are the input signals. Waveform 4 is the output of the multiplier circuit, and, again, its operation is easily understood by viewing it as a variable gain amplifier. One input (e.g., channel 1 in Figure 11.9) controls the gain for the second input (e.g., channel 2 in Figure 11.9).

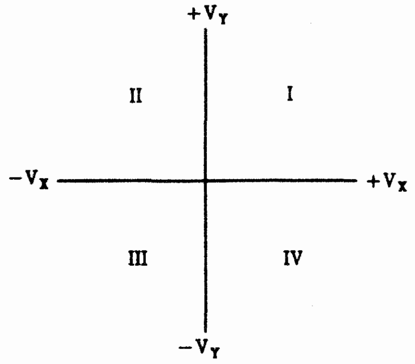


FIGURE 11.7 There are four possible modes or quadrants of operation for multiplier circuits.

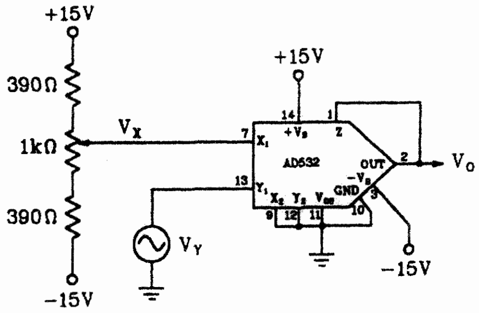
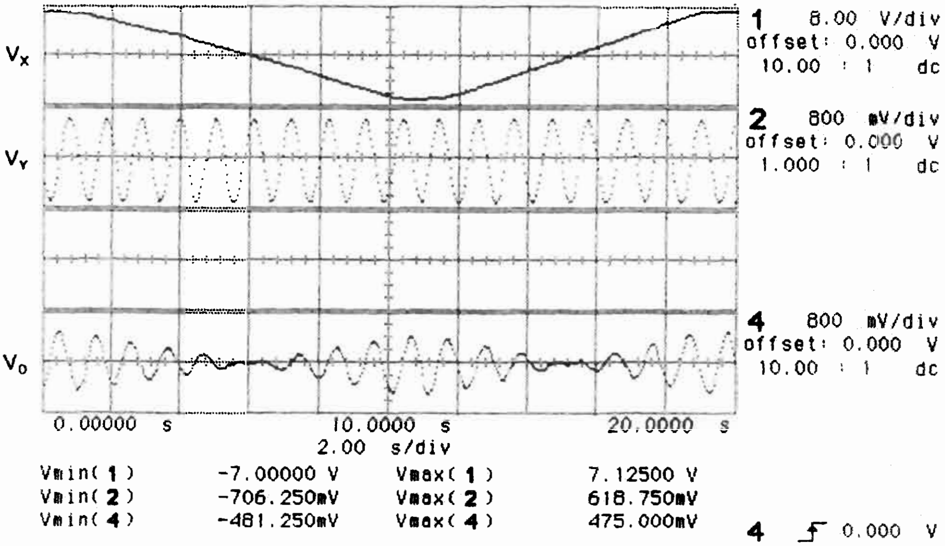


FIGURE 11.8 The AD532 connected as a simple multiplier circuit.



```
Vmin( 1 )   -7.00000 V     Vmax( 1 )   7.12500 V
Vmin( 2 )   -706.250mV     Vmax( 2 )   618.750mV
Vmin( 4 )   -481.250mV     Vmax( 4 )   475.000mV
```

FIGURE 11.9 Oscilloscope display showing the actual behavior of the circuit shown in Figure 11.8. (Test equipment courtesy of Hewlett-Packard Company.)

The multiplier circuit can also be configured to perform several other mathematical operations, including division, squaring, and square root functions. Figures 11.10, 11.11, and 11.12 show the connections required to utilize the AD532 to achieve these other functions.

Still another interesting application of the basic multiplier circuit can be demonstrated by applying the same sinusoidal waveform to both multiplier inputs, in which case the output will be a sinusoidal waveform with a frequency that is exactly double the input frequency. Thus, the multiplier circuit can be used as a frequency doubler without resorting to the use of tuned tank circuits.

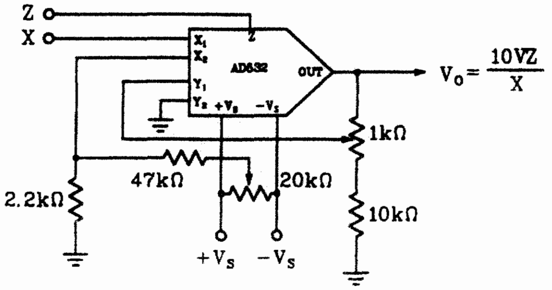

Z
X
X1
X2
Y1
Y2
AD532
OUT
+Vs
-Vs
Vo = 10VZ/X
1kΩ
47kΩ
20kΩ
2.2kΩ
10kΩ
+Vs
-Vs

FIGURE 11.10 The AD532 connected as a divider circuit.

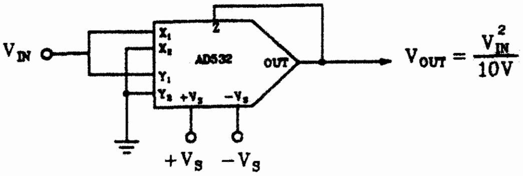

VIN
X1
X2
Y1
Y2
Z
AD532
OUT
+Vs
-Vs
VOUT = VIN²/10V
+Vs
-Vs

FIGURE 11.11 The AD532 connected to operate as a squaring circuit.

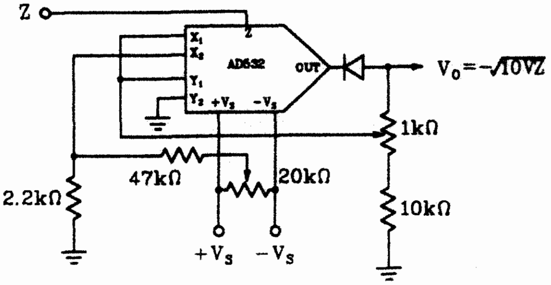

Z
X1
X2
Y1
Y2
AD532
OUT
+Vs
-Vs
Vo=-√10VZ
1kΩ
47kΩ
20kΩ
2.2kΩ
10kΩ
+Vs
-Vs

FIGURE 11.12 The AD532 connected to generate the square root function.

11.6 SINGLE-SUPPLY AMPLIFIERS

The 741, as well as other standard op amps, can be operated with a single-polarity power supply. We will examine this type of operation in this section, and we will discuss the operation of two additional op amp types that are specifically designed to be powered from a single supply.

Figure 11.13 illustrates how to operate a standard 741 (or similar dual-supply op amp) from a single-polarity power source. Here the $-V_{CC}$ terminal is returned to ground and the $+V_{CC}$ terminal is connected to +15 volts. To establish midpoint bias, a voltage divider made up of two equal resistors (R_3 and R_4) provide a DC voltage of 0.5 V_{CC} to the noninverting input terminal. Capacitor C_2 ensures that the (+) input is at AC ground potential and should have a low reactance at the lowest input frequency. Since under normal circuit conditions, the (–) input will be at the

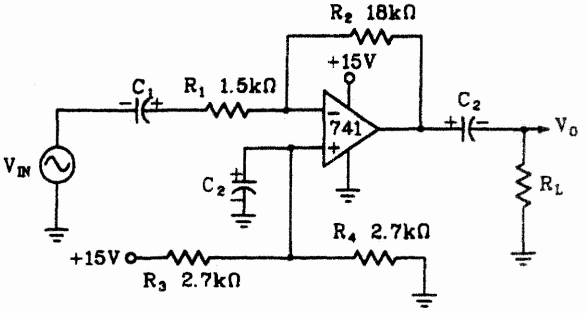
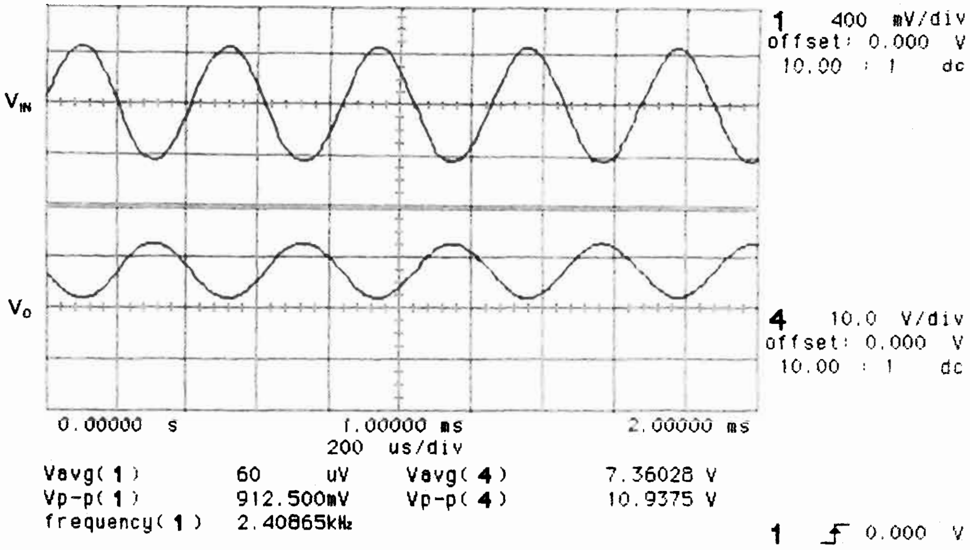


FIGURE 11.13 The standard 741 op amp can be operated from a single-polarity power source.

same DC potential as the (+) input (+7.5 volts in the present case), capacitor C_1 is included to provide DC isolation between the input source and the DC voltage on the (–) input. Resistors R_1 and R_2 serve their usual function of establishing input impedance and voltage gain.

The oscilloscope displays in Figure 11.14 further illustrate the operation of the circuit in Figure 11.13. Waveform 1 is the signal at the input of the amplifier; notice that the DC voltage is about 0 (60 μV). Waveform 4 is the signal at the output of the op amp; here we can see a DC offset of 7.36 volts or about ½ of V_{CC}. The voltage gain (12) and phase inversion are both evident from the oscilloscope display and correlate exactly with the performance of the normal dual-supply configuration. The $+V_{CC}$ pin is often connected to a higher voltage (e.g., +30 V).

Some manufacturers provide op amps specifically designed to be operated from a single-polarity power supply. We will now briefly examine the operation of two such devices (MC34071 and MC3401), both manufactured by Motorola, Inc.



```
Vavg( 1 )          60      uV      Vavg( 4 )        7.36028 V
Vp-p( 1 )          912.500mV       Vp-p( 4 )        10.9375 V
frequency( 1 )     2.40865kHz
```

FIGURE 11.14 Actual performance of the circuit shown in Figure 11.13.

Figure 11.15 shows an MC34071 connected as an AC-coupled inverting amplifier. In general, utilization of this device is similar to that of the basic 741 (e.g., $A_V = R_F/R_I$). The most conspicuous difference may be the fact that the MC34071 is specifically designed for single-supply operation, but there are a number of other features that clearly separate this device from basic op amps. Consider the following highlights:

1. The output voltage can typically swing to within 1.0 volt of the $+V_{CC}$ and to within 0.3 volt of the $-V_{CC}$ level (ground in the case of single-supply operation).
2. The supply voltage can range between 3 and 44 volts.
3. Unity gain frequency is about 4.5 megahertz.
4. Slew rates are as high as 13 volts per microsecond.
5. Full output voltage swings at frequencies over 100 kilohertz.

Figure 11.16(a) shows an inverting amplifier configuration using an MC3401 op amp. Figure 11.16(b) shows a basic noninverting amplifier connection. This single-supply device is called a *Norton operational amplifier* or *current differencing amplifier* (CDA) that has an input structure considerably different from that of the other op amps discussed in the earlier sections. Figure 11.17 shows a simplified schematic that helps clarify the behavior of the input circuitry on the Norton amplifier.

The op amp is generally biased by connecting a DC voltage (V_B) through a resistor (R_B) to the (+) input (see Figure 11.16). This causes $I_I(+)$ to flow through diode D_1 in Figure 11.17. The value of the $I_I(+)$ current can easily be estimated with Ohm's Law as

$$I_I(+) = \frac{V_B - 0.6}{R_B}$$

where V_B is the bias voltage source, R_B is the resistor in series with the (+) terminal, and 0.6 volt is the nominal voltage drop across the input diode (D_1 in Figure 11.17). The range of normal operating currents for $I_I(+)$ is between 10 and 200 microamperes.

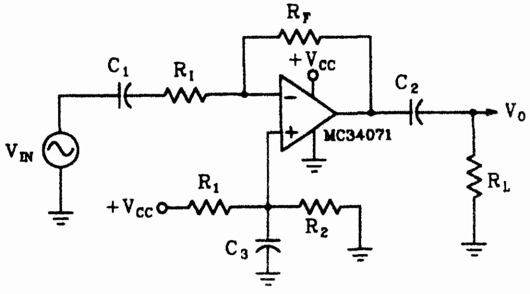
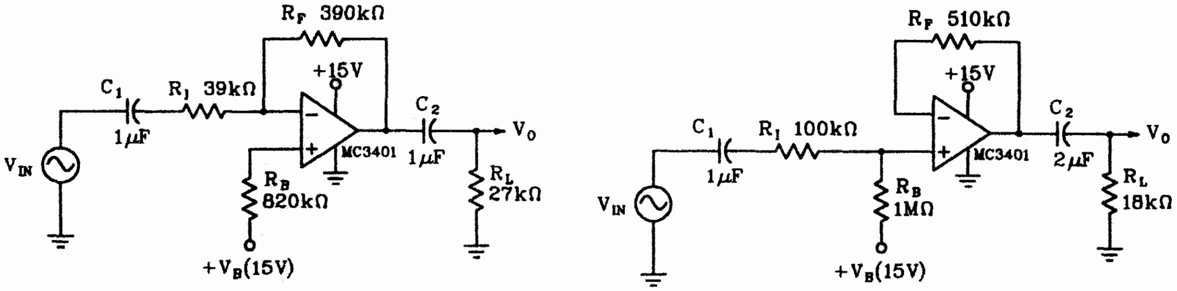


FIGURE 11.15 An AC-coupled amplifier using the MC34071 op amp.


R_F 390kΩ
+15V
C_1
R_1 39kΩ
C_2
V_O
1μF
V_IN
MC3401
1μF
R_B
820kΩ
R_L
27kΩ
+V_B(15V)
R_F 510kΩ
+15V
C_2
C_1
R_1 100kΩ
V_O
MC3401
2μF
1μF
R_B
1MΩ
R_L
18kΩ
V_IN
+V_B(15V)

(a) (b)

FIGURE 11.16 The MC3401 Norton operational amplifier is intended for single-supply operation. Circuit configurations for inverting (a) and noninverting (b) are shown.

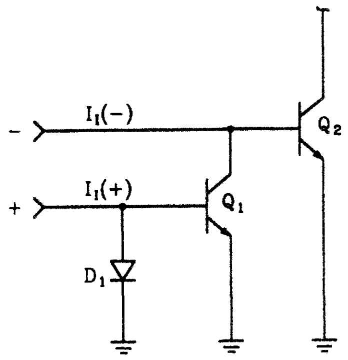


FIGURE 11.17 The simplified input circuitry for the Norton operational amplifier.

Transistor Q_1 in Figure 11.17 has matched characteristics with D_1 and will thus develop a collector current very nearly identical to the value of $I_I(+)$. This type of circuit is called a current mirror and tends to cause a mirror current in the (–) input that is equal to the current in the (+) input. The base current of Q_2 is essentially negligible for this analysis. This tendency toward keeping similar currents in the two terminals is analogous to the tendency of a standard op amp to keep the voltage on the two input terminals at the same level. The actual "signal" seen by Q_2 is the difference between $I_I(+)$ and $I_I(-)$. Just as closed-loop operation in a standard op amp tends to reduce the differential input voltage to 0, closed-loop operation in a Norton amplifier tends to reduce the differential input current to 0. The output circuitry of the MC3401 behaves similarly to a standard op amp, although the output resistance is substantially higher. Some comparative characteristics are as follows:

1. The output voltage can typically swing to within 1.0 volt or less of $+V_{CC}$ and ground.
2. The supply voltage can range between 5 and 18 volts.
3. Unity gain frequency is about 4 megahertz.
4. Slew rates are 0.5 volts per microsecond on the positive slope and 20 volts per microsecond on the negative slope.
5. Full output voltage swings up to about 8 kilohertz.

The DC output voltage (quiescent operating point) is established by the following manufacturer-provided equation:

$$V_{Odc} = \frac{(A_I)(V_B)(R_F)}{R_B} + \left(1 - \frac{R_F}{R_B} A_I\right)\Phi$$

where A_I is the gain of the current mirror, V_B is the DC voltage source used to bias the (+) input, R_B is the bias resistor in the (+) input, R_F is the feedback resistor, and Φ is base-emitter voltage drop of the input transistors. If the bias voltage is more than 5 volts, the second term of the equation may be discarded with only minimal error. Similarly, since the A_I factor is nominally equal to unity, we can simplify this expression to that given by Equation (11.4).

$$V_{Odc} = V_R\left(\frac{R_F}{R_B}\right) \tag{11.4}$$

The DC output voltage for the circuit shown in Figure 11.16(a), for example, can be estimated as follows:

$$V_{Odc} = V_B\left(\frac{R_F}{R_B}\right) = 15\ V\left(\frac{390\ k\Omega}{820\ k\Omega}\right) = 7.13\ V$$

If the more exacting equation given previously were used, the output voltage would be computed as 7.44 volts.

In a similar manner, the DC output voltage for Figure 11.16(b) can be estimated as follows:

$$V_{Odc} = V_B\left(\frac{R_F}{R_B}\right) = 15\ V\left(\frac{510\ k\Omega}{1\ M\Omega}\right) = 7.65\ V$$

The voltage gain for the inverting amplifier configuration in Figure 11.16(a) is identical to the standard op amp circuit. That is,

$$A_V = -\frac{R_F}{R_I}$$

The noninverting configuration, shown in Figure 11.16(b), is a little different. The manufacturer provides the following equation:

$$A_V = \frac{(R_F)(A_i)}{R_i + \dfrac{0.026}{I_i(+)}}$$

As long as the input resistor (R_I) is over 26 kilohms, you can get reasonable results from the simplified equation given in Equation (11.5).

$$A_V = \frac{R_F}{R_I} \tag{11.5}$$

It is very important to note that this is different from the standard noninverting amplifier circuit. If, for example, you want to build a voltage follower circuit (unity gain), the feedback resistor (R_F) and the input resistor (R_I) have to be equal. In the standard amplifier, on the other hand, unity gain is achieved in the noninverting configuration by reducing the feedback resistor to 0.

Since the input terminals, both (+) and (–), essentially have a PN junction to ground, the voltage at these points will not change substantially. Therefore, they may be considered as AC ground points for purposes of computing bandwidth and other AC values. For example, the lower cutoff frequency for the input coupling network is determined by the values of R_I and C_1. More specifically, the cutoff frequency for this portion of the circuit occurs when X_{C1} equals R_I. That is,

$$f_C = \frac{1}{2\pi C_1 R_I}$$

Although the circuit can be used as a DC, or direct-coupled, amplifier, it is frequently AC coupled as shown in Figure 11.16(a) and (b) to avoid disturbing the DC bias on the input terminal and to eliminate the DC offset in the output (typically one-half of $+V_{CC}$).

11.7 MULTIPLE OP AMP PACKAGES

Although all of the circuits presented in this text have considered the op amp to be a single integrated circuit, many op amps are available that have more than one device in a single integrated package. With the single exception of $\pm V_{CC}$, these multiple op amps are independent; that is, they can be utilized in the same way as if they were packaged separately. The 747 op amp package, for example, is essentially two 741 op amps combined in a single package. Similarly, the MC3401 device presented in the previous section actually provides four independent op amps in a single integrated package. The obvious advantages of selecting a multiple op amp package is to reduce the physical size of the circuit and to reduce cost (a package with four op amps is generally less expensive than four separate packages with similar op amps).

11.8 HYBRID OPERATIONAL AMPLIFIERS

Throughout the body of this text, we have generally confined our discussions and design examples to the basic 741 and the MC741SC. These devices are certainly not the newest, fastest, or necessarily the best in all applications, but they are very common and the principles presented directly extend to other higher-performance devices.

To provide the reader with a dramatic performance contrast, and to illustrate the performance characteristics that are available in op amps, we will briefly examine the operational characteristics of a hybrid op amp manufactured by the M.S. Kennedy Corporation (MSK). Numerous devices manufactured by MSK offer outstanding performance. We will describe the MSK 739 Wideband Amplifier as a representative device.

TABLE 11.1

Parameter	*General-Purpose Op Amp*	*MSK 739*
Input offset voltage	2 millivolts	±25 microvolts
Input bias current	80 nanoamps	±75 picoamps
Input offset current	20 nanoamps	25 picoamps
Output voltage swing	±13 volts	±12 volts
Full power bandwidth	6.12 kilohertz	30 megahertz
Unity gain frequency	1.0 megahertz	210 megahertz
Slew rate	0.5 volts/microsecond	5500 volts/microsecond
Output current	±6.5 milliamps	±120 milliamps
Power supply rejection ratio	90 decibels	115 decibels
Common mode rejection ratio	90 decibels	110 decibels

The MSK 739 is manufactured using hybrid (i.e., both thick-film and thin-film) technology. It is not appropriate for general-purpose applications any more than the standard 741 is appropriate for very-high-performance applications. Nevertheless, its performance can be quickly appreciated by contrasting some of its key parameters with those of a general-purpose amplifier. Table 11.1 provides comparative data.

The data in the table is intended for comparison purposes only to illustrate some of the outstanding performance that is available in hybrid op amps. The characteristics cited for the general-purpose device are typical and do not necessarily represent a specific device.

REVIEW QUESTIONS

1. A programmable op amp is often selected for applications requiring low-power consumption. (True or False)
2. Circle the correct word to describe the relative value of each of the following parameters with reference to instrumentation amplifiers:
   a. Input impedance (High or Low)
   b. Output impedance (High or Low)
   c. Common-mode rejection (High or Low)
3. When single-supply op amps are used in a multistage amplifier circuit, the individual stages must generally be AC coupled. Explain why.
4. A multiplier circuit that accepts either polarity of voltage on both of its inputs is called a ____-quadrant multiplier.
5. What type of amplifier circuit is used to compress a wide dynamic range of input voltage amplitudes?

APPENDIX 1

Data sheets for the Motorola MC1741 operational amplifier (pages 2-170 through 2-174). Copyright of Motorola, Inc. Used by permission.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1741
MC1741C

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

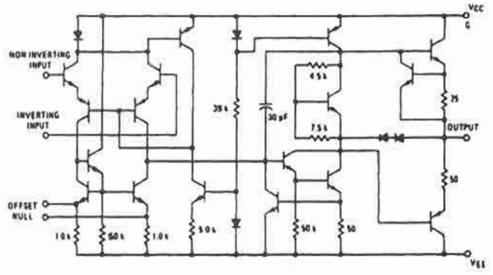
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

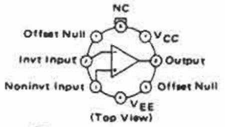
Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	+22 −22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	−55 to +125	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 −65 to +150 −55 to +125		°C

NOTES:
1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC



VCC
NON INVERTING INPUT
INVERTING INPUT
OFFSET NULL
39 k
30 pF
4.5 k
7.5 k
25
OUTPUT
50
1.0 k
50 k
1.0 k
5.0 k
50 k
50
VEE



NC
Offset Null
VCC
Invt Input
Output
Noninvt Input
Offset Null
VEE
(Top View)

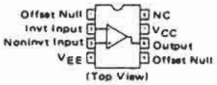
G SUFFIX
METAL PACKAGE
CASE 601

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



Offset Null
Invt Input
Noninvt Input
VEE
NC
VCC
Output
Offset Null
(Top View)

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1741CD	—	0°C to +70°C	SO-8
MC1741CG	LM741CH, μA741HC		Metal Can
MC1741CP1	LM741CN, μA741TC		Plastic DIP
MC1741CU	—		Ceramic DIP
MC1741G	—	−55°C to +125°C	Metal Can
MC1741U	—		Ceramic DIP

MC1741, MC1741C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing ($R_L \geq 10$ k) ($R_L \geq 2$ k)	V_O	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 ±14 ±13	 – –	V
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	–	50	85	mW
Transient Response (Unity Gain – Non-Inverting) (V_I = 20 mV, R_L > 2 k, C_L < 100 pF) Rise Time (V_I = 20 mV, R_L > 2 k, C_L < 100 pF) Overshoot (V_I = 10 V, R_L > 2 k, C_L < 100 pF) Slew Rate	 t_{TLH} os SR	 – – –	 0.3 15 0.5	 – – –	 – – –	 0.3 15 0.5	 – – –	 μs % V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current (T_A = 125°C) (T_A = -55°C) (T_A = 0°C to +70°C)	I_{IO}	 – – –	 7.0 85 –	 200 500 –	 – – –	 – – –	 – – 300	nA
Input Bias Current (T_A = 125°C) (T_A = -55°C) (T_A = 0°C to +70°C)	I_{IB}	 – – –	 30 300 –	 500 1500 –	 – – –	 – – –	 – – 800	nA
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing ($R_L \geq 10$ k) ($R_L \geq 2$ k)	V_O	 ±12 ±10	 ±14 ±13	 – –	 – ±10	 – ±13	 – –	V
Large Signal Voltage Gain ($R_L \geq 2$ k, V_{out} = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Supply Currents (T_A = 125°C) (T_A = -55°C)	I_D	 – –	 1.5 2.0	 2.5 3.3	 – –	 – –	 – –	mA
Power Consumption (T_A = +125°C) (T_A = -55°C)	P_C	– –	45 60	75 100	– –	– –	– –	mW

*T_{high} = 125°C for MC1741 and 70°C for MC1741C
T_{low} = -55°C for MC1741 and 0°C for MC1741C

MC1741, MC1741C

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

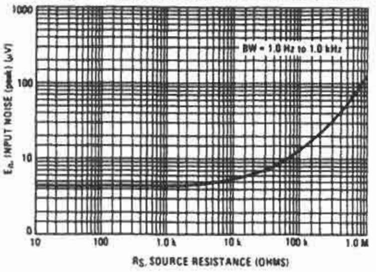


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

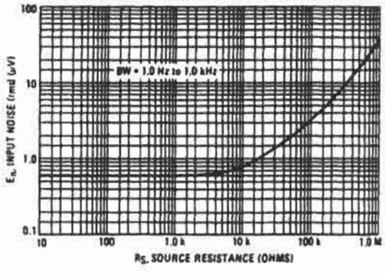


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

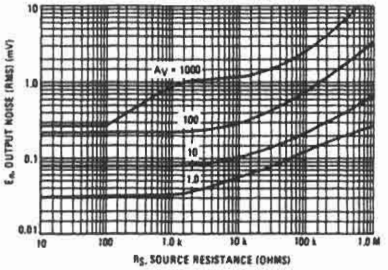


FIGURE 4 – SPECTRAL NOISE DENSITY

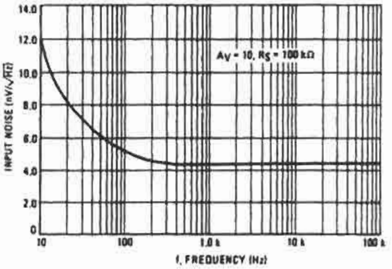
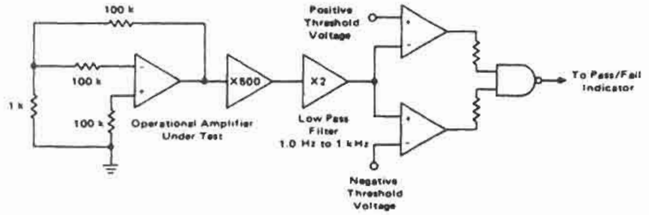


FIGURE 5 – BURST NOISE TEST CIRCUIT


100 k
100 k
1 k
100 k
Operational Amplifier
Under Test
X500
X2
Low Pass
Filter
1.0 Hz to 1 kHz
Positive
Threshold
Voltage
Negative
Threshold
Voltage
To Pass/Fail
Indicator

Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 µV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

MC1741, MC1741C

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

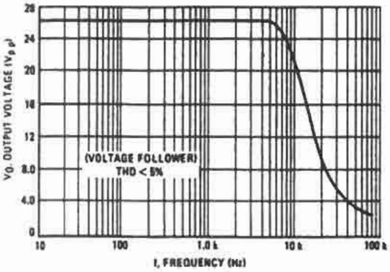


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

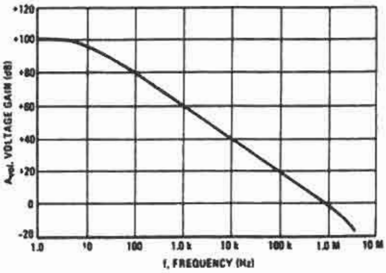


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

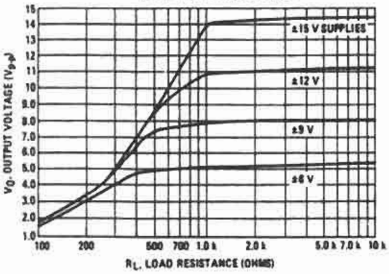


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

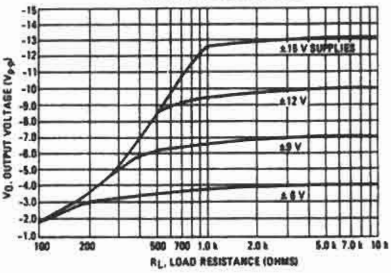


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

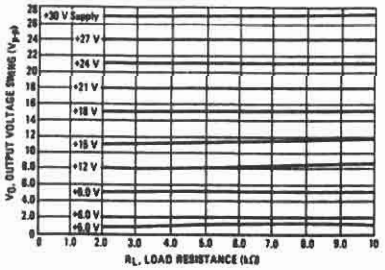
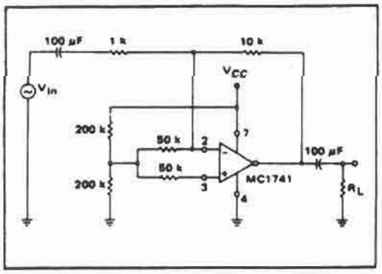


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER


100 µF
1 k
10 k
V_{in}
V_{CC}
200 k
200 k
50 k
50 k
2
3
7
4
−
+
MC1741
100 µF
R_L

MC1741, MC1741C

FIGURE 12 — NONINVERTING PULSE RESPONSE

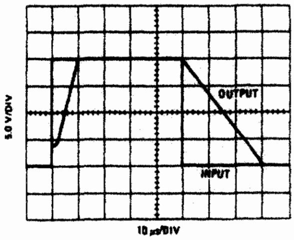


FIGURE 13 — TRANSIENT REPONSE TEST CIRCUIT

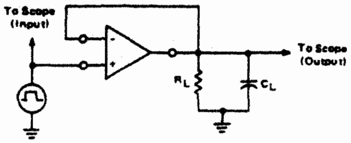
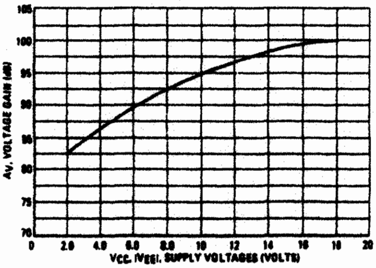

To Scope
(Input)
-
+
To Scope
(Output)
R_L
C_L

FIGURE 14 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



APPENDIX 2

Data sheets for the Motorola MJE1103 transistor (pages 3-474 through 3-475). Copyright of Motorola, Inc. Used by permission.

MJE1090 thru MJE1093 PNP (SILICON)
MJE2090 thru MJE2093
MJE1100 thru MJE1103 NPN
MJE2100 thru MJE2103

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

Designed for use in driver and output stages in complementary audio amplifier applications.

- High DC Current Gain –
  h_{FE} = 750 (Min) @ I_C = 3.0 and 4.0 Adc
- True Three Lead Monolithic Construction – Emitter-Base Resistors to Prevent Leakage Multiplication are Built in.
- Available in Two Packages – Case 90 or Case 199

5.0 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

60-80 VOLTS
70 WATTS

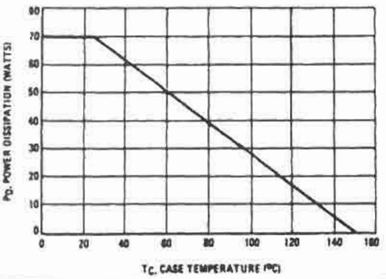
MAXIMUM RATINGS

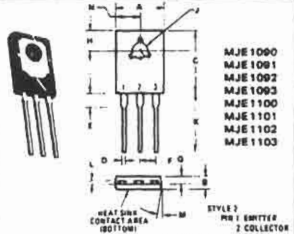
Rating	Symbol	MJE1090 MJE1091 MJE1100 MJE1101 MJE2090 MJE2091 MJE2100 MJE2101	MJE1092 MJE1093 MJE1102 MJE1103 MJE2092 MJE2093 MJE2102 MJE2103	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	5.0		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56		Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.8	°C/W

FIGURE 1 – POWER DERATING





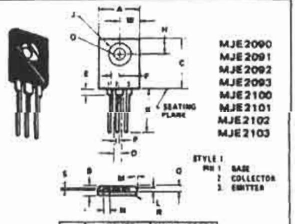
MJE1090
MJE1091
MJE1092
MJE1093
MJE1100
MJE1101
MJE1102
MJE1103

STYLE 2
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	[illegible]	[illegible]	[illegible]	[illegible]
B	[illegible]	[illegible]	[illegible]	[illegible]
C	[illegible]	[illegible]	[illegible]	[illegible]
D	[illegible]	[illegible]	[illegible]	[illegible]
E	[illegible]	[illegible]	[illegible]	[illegible]
F	[illegible]		[illegible]	
G	[illegible]	[illegible]	[illegible]	[illegible]
H	[illegible]	[illegible]	[illegible]	[illegible]
J	[illegible]	[illegible]	[illegible]	[illegible]
K	[illegible]	[illegible]	[illegible]	[illegible]
L	[illegible]	[illegible]	[illegible]	[illegible]
M	[illegible]		[illegible]	
N	[illegible]	[illegible]	[illegible]	[illegible]

NOTE
DIM "E" UNCONTROLLED

CASE 90-05



MJE2090
MJE2091
MJE2092
MJE2093
MJE2100
MJE2101
MJE2102
MJE2103

STYLE 1
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	[illegible]	[illegible]	[illegible]	[illegible]
B	[illegible]	[illegible]	[illegible]	[illegible]
C	[illegible]	[illegible]	[illegible]	[illegible]
D	[illegible]	[illegible]	[illegible]	[illegible]
E	[illegible]	[illegible]	[illegible]	[illegible]
F	[illegible]		[illegible]	
G	[illegible]	[illegible]	[illegible]	[illegible]
H	[illegible]	[illegible]	[illegible]	[illegible]
J	[illegible]	[illegible]	[illegible]	[illegible]
K	[illegible]	[illegible]	[illegible]	[illegible]
L	[illegible]	[illegible]	[illegible]	[illegible]
M	[illegible]		[illegible]	
N	[illegible]	[illegible]	[illegible]	[illegible]
P	[illegible]	[illegible]	[illegible]	[illegible]
Q	[illegible]	[illegible]	[illegible]	[illegible]
R	[illegible]		[illegible]	
S	[illegible]	[illegible]	[illegible]	[illegible]
W	[illegible]	[illegible]	[illegible]	[illegible]

NOTE
1. DIM "F" IS TO CENTERLINE OF LEADS

CASE 199-04

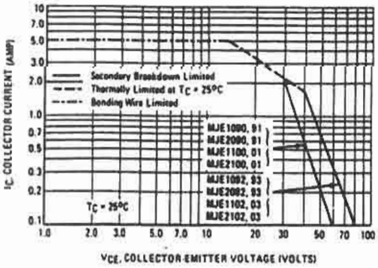
MJE1090 thru MJE1093 PNP/MJE1100 thru MJE1103 NPN (continued)
MJE2090 thru MJE2093 PNP/MJE2100 thru MJE2103 NPN

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJE1090, MJE1091, MJE1100, MJE1101 MJE2090, MJE2091, MJE2100, MJE2101	BV_{CEO}	60 60	– –	Vdc
	MJE1092, MJE1093, MJE1102, MJE1103 MJE2092, MJE2093, MJE2102, MJE2103		80 80	– –	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	MJE1090, MJE1091, MJE1100, MJE1101 MJE2090, MJE2091, MJE2100, MJE2101	I_{CEO}	– –	500 500	µAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJE1092, MJE1093, MJE1102, MJE1103 MJE2092, MJE2093, MJE2102, MJE2103		– –	500 500	
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	– –	0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	MJE1090, MJE1092, MJE1100, MJE1102 MJE2090, MJE2092, MJE2100, MJE2102	h_{FE}	750 750	– –	–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	MJE1091, MJE1093, MJE1101, MJE1103 MJE2091, MJE2093, MJE2101, MJE2103		750 750	– –	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc)	MJE1090, MJE1092, MJE1100, MJE1102 MJE2090, MJE2092, MJE2100, MJE2102	$V_{CE(sat)}$	– –	2.5 2.5	Vdc
(I_C = 4.0 Adc, I_B = 16 mAdc)	MJE1091, MJE1093, MJE1101, MJE1103 MJE2091, MJE2093, MJE2101, MJE2103		– –	2.8 2.8	
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	MJE1090, MJE1092, MJE1100, MJE1102 MJE2090, MJE2092, MJE2100, MJE2102	$V_{BE(on)}$	– –	2.5 2.5	Vdc
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	MJE1091, MJE1093, MJE1101, MJE1103 MJE2091, MJE2093, MJE2101, MJE2103		– –	2.5 2.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	–	–

(1)Pulse Test: Pulse Width $\leqslant$ 300 µs, Duty Cycle $\leqslant$ 2.0%.

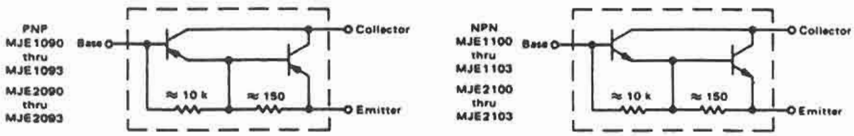
FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown. (See AN-415)

FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC



APPENDIX 3

Data sheets for the Motorola 2N2222 transistor (pages 2-255 through 2-261). Copyright of Motorola, Inc. Used by permission.

2N2218,A, 2N2219,A 2N2221,A(SILICON) 2N2222,A, 2N5581, 2N5582

NPN SILICON ANNULAR HERMETIC TRANSISTORS

. . . widely used "Industry Standard" transistors for applications as medium-speed switches and as amplifiers from audio to VHF frequencies.

- DC Current Gain Specified – 1.0 to 500 mAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ @ I_C = 500 mAdc
  = 1.6 Vdc (Max) – Non-A Suffix
  = 1.0 Vdc (Max) – A-Suffix
- High Current-Gain–Bandwidth Product –
  f_T = 250 MHz (Min) @ I_C = 20 mAdc – All Types Except
  = 300 MHz (Min) @ I_C = 20 mAdc – 2N2219A, 2N2222A, 2N5582
- Complements to PNP 2N2904,A thru 2N2907,A
- JAN/JANTX Available for all devices

NPN SILICON SWITCHING AND AMPLIFIER TRANSISTORS

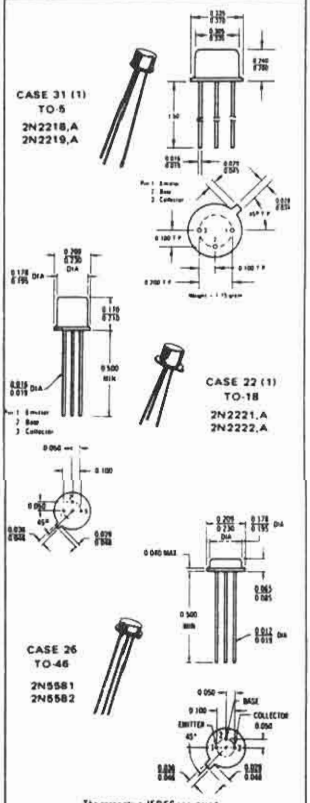
SELECTION GUIDE

Device Type	Characteristic BV_{CEO} I_C = 10 mAdc Volts	h_{FE} I_C = 150 mAdc Min/Max	h_{FE} I_C = 500 mAdc Min	Package
2N2218 2N2219	30	40/120 100/300	20 30	TO-5
2N2221 2N2222	30	40/120 100/300	20 30	TO-18
2N5581 2N5582	40	40/120 100/300	25 40	TO-46
2N2218A 2N2219A	40	40/120 100/300	25 40	TO-5
2N2221A 2N2222A	40	40/120 100/300	25 40	TO-18

*MAXIMUM RATINGS

Rating	Symbol	2N2218 2N2219 2N2221 2N2222	2N2218A 2N2219A 2N2221A 2N2222A	2N5581 2N5582	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	40	Vdc
Collector-Base Voltage	V_{CB}	60	75	75	Vdc
Emitter-Base Voltage	V_{EB}	5.0	6.0	6.0	Vdc
Collector Current – Continuous	I_C	800	800	800**	mAdc
		2N2218,A 2N2219,A	2N2221,A 2N2222,A	2N5581 2N5582	
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.8 5.33	0.5 3.33	0.5 3.33	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 20	1.8 12	2.0 11.43	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

*Indicates JEDEC Registered Data.
**Motorola Guarantees this Data in Addition to JEDEC Registered Data.


CASE 31 (1)
TO-5
2N2218,A
2N2219,A
Pin 1 Emitter
2 Base
3 Collector
45° T.P.
0.100 T.P.
0.200 T.P.
Weight = 1.15 gram
0.178 DIA
0.195
0.209
0.230
DIA
0.500 MIN
CASE 22 (1)
TO-18
2N2221,A
2N2222,A
0.050
0.100
45°
CASE 26
TO-46
2N5581
2N5582
0.040 MAX
0.065
0.085
0.012
0.019
DIA
BASE
COLLECTOR
EMITTER

The respective JEDEC registered dimensions and notes apply

2N2218,A, 2N2219,A, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 10 mAdc, I_B = 0)	Non-A Suffix		30	–	
	A-Suffix, 2N5581,2N5582		40	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 10 μAdc, I_E = 0)	Non-A Suffix		60	–	
	A-Suffix, 2N5581,2N5582		75	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 10 μAdc, I_C = 0)	Non-A Suffix		5.0	–	
	A-Suffix, 2N5581,2N5582		6.0	–	
Collector Cutoff Current		I_{CEX}			nAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	A-Suffix, 2N5581,2N5582		–	10	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 50 Vdc, I_E = 0)	Non-A Suffix		–	0.01	
(V_{CB} = 60 Vdc, I_E = 0)	A-Suffix, 2N5581,2N5582		–	0.01	
(V_{CB} = 50 Vdc, I_E = 0, T_A = 150°C)	Non-A Suffix		–	10	
(V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)	A-Suffix, 2N5581,2N5582		–	10	
Emitter Cutoff Current		I_{EBO}			nAdc
(V_{EB} = 3.0 Vdc, I_C = 0)	A-Suffix, 2N5581,2N5582		–	10	
Base Cutoff Current		I_{BL}			nAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	A-Suffix		–	20	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2N2218,A,2N2221,A,2N5581(1)		20	–	
	2N2219,A,2N2222,A,2N5582(1)		35	–	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2N2218,A,2N2221,A,2N5581		25	–	
	2N2219,A,2N2222,A,2N5582		50	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N2218,A,2N2221,A,2N5581(1)		35	–	
	2N2219,A,2N2222,A,2N5582(1)		75	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = -55°C)	2N2218A,2N2221A,2N5581		15	–	
	2N2219A,2N2222A,2N5582		35	–	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)(1)	2N2218,A,2N2221,A,2N5581		40	120	
	2N2219,A,2N2222,A,2N5582		100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)(1)	2N2218A,2N2221A,2N5581		20	–	
	2N2219A,2N2222A,2N5582		50	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)(1)	2N2218,2N2221		20	–	
	2N2219,2N2222		30	–	
	2N2218A,2N2221A,2N5581		25	–	
	2N2219A,2N2222A,2N5582		40	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	Non-A Suffix		–	0.4	
	A-Suffix, 2N5581,2N5582		–	0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)	Non-A Suffix		–	1.6	
	A-Suffix, 2N5581,2N5582		–	1.0	
Base-Emitter Saturation Voltage(1)		$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	Non-A Suffix		0.6	2.0	
	A-Suffix, 2N5581,2N5582		0.6	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)	Non-A Suffix		–	2.6	
	A-Suffix, 2N5581,2N5582		–	2.0	

2N2218,A, 2N2219,A, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

*ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Min	Max	Unit
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product(2)		f_T			MHz
(I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	All Types, Except		250	–	
	2N2219A,2N2222A,2N5582		300	–	
Output Capacitance(3) (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	8.0	pF
Input Capacitance(3)		C_{ib}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	Non-A Suffix		–	30	
	A-Suffix, 2N5581,2N5582		–	25	
Input Impedance		h_{ie}			k ohms
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		1.0	3.5	
	2N2219A,2N2222A,2N5582		2.0	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		0.2	1.0	
	2N2219A,2N2222A,2N5582		0.25	1.25	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		–	5.0	
	2N2219A,2N2222A,2N5582		–	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		–	2.5	
	2N2219A,2N2222A,2N5582		–	4.0	
Small-Signal Current Gain		h_{fe}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		30	150	
	2N2219A,2N2222A,2N5582		50	300	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		50	300	
	2N2219A,2N2222A,2N5582		75	375	
Output Admittance		h_{oe}			μmhos
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		3.0	15	
	2N2219A,2N2222A,2N5582		5.0	35	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A,2N2221A,2N5581		10	100	
	2N2219A,2N2222A,2N5582		25	200	
Collector-Base Time Constant (I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	A-Suffix, 2N5581,2N5582	$r_b'C_c$	–	150	ps
Noise Figure (I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 k ohm, f = 1.0 kHz)	2N2219A,2N2222A	NF	–	4.0	dB
SWITCHING CHARACTERISTICS (A-Suffix, 2N5581 and 2N5582)					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 14)	t_d	–	10	ns
Rise Time		t_r	–	25	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 15)	t_s	–	225	ns
Fall Time		t_f	–	60	ns
Active Region Time Constant** (I_C = 150 mAdc, V_{CE} = 30 Vdc)		T_A	–	2.5	ns

*Indicates JEDEC Registered Data.

**Motorola Guarantees this Data in Addition to JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

(3) 2N5581 and 2N5582 are Listed C_{cb} and C_{eb} for these conditions and values.

2N2218,A, 2N2219,A, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

FIGURE 1 – NORMALIZED DC CURRENT GAIN

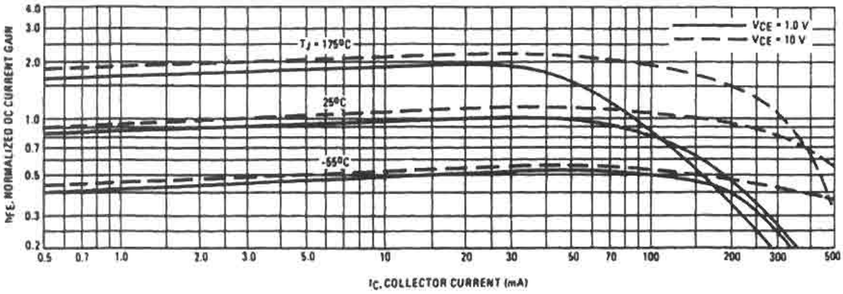
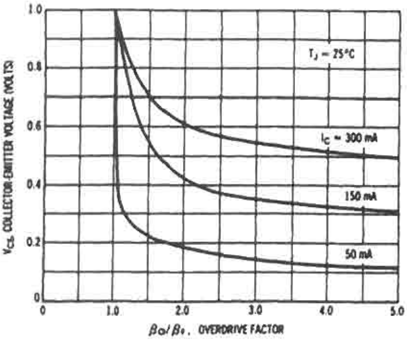


FIGURE 2 – COLLECTOR CHARACTERISTICS IN SATURATION REGION



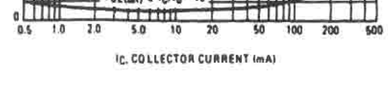
This graph shows the effect of base current on collector current. β_o (current gain at the edge of saturation) is the current gain of the transistor at 1 volt, and β_F (forced gain) is the ratio of I_C/I_{BF} in a circuit.

EXAMPLE: For type 2N2219, estimate a base current (I_{BF}) to insure saturation at a temperature of 25°C and a collector current of 150 mA.

Observe that at $I_C = 150$ mA an overdrive factor of at least 2.5 is required to drive the transistor well into the saturation region. From Figure 1, it is seen that h_{FE} @ 1 volt is approximately 0.62 of h_{FE} @ 10 volts. Using the guaranteed minimum gain of 100 @ 150 mA and 10 V, $\beta_o = 62$ and substituting values in the overdrive equation, we find:

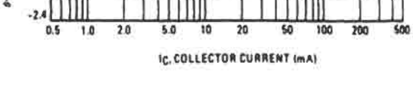
$$\frac{\beta_o}{\beta_F} = \frac{h_{FE} \text{ @ } 1.0\,V}{I_C/I_{BF}} \qquad 2.5 = \frac{62}{150/I_{BF}} \qquad I_{BF} \approx 6.0 \text{ mA}$$

FIGURE 3 – "ON" VOLTAGES



I_C, COLLECTOR CURRENT (mA)

FIGURE 4 – TEMPERATURE COEFFICIENTS



I_C, COLLECTOR CURRENT (mA)

2N2218,A, 2N2219,A, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

NOISE FIGURE

V_{CE} = 10 V, T_A = 25°C

FIGURE 5 – FREQUENCY EFFECTS

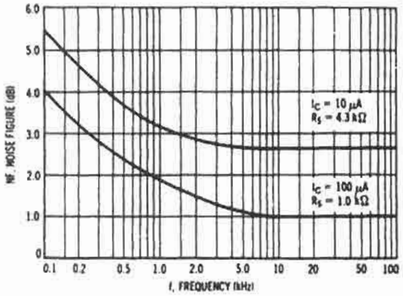
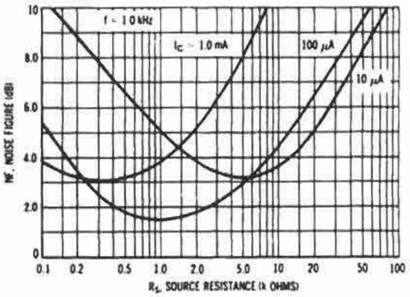


FIGURE 6 – SOURCE RESISTANCE EFFECTS



h PARAMETERS

V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C

This group of graphs illustrates the relationship between h_{fe} and other "h" parameters for this series of transistors. To obtain these curves, a high-gain and a low-gain unit were selected and the same units were used to develop the correspondingly numbered curves on each graph.

FIGURE 7 – INPUT IMPEDANCE

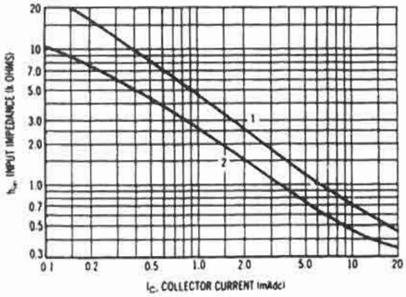


FIGURE 8 – VOLTAGE FEEDBACK RATIO

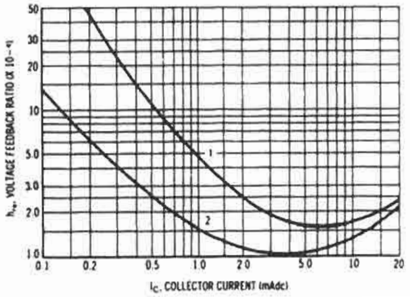


FIGURE 9 – CURRENT GAIN

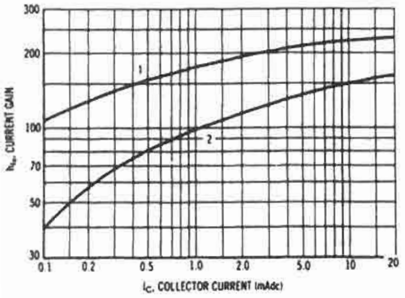
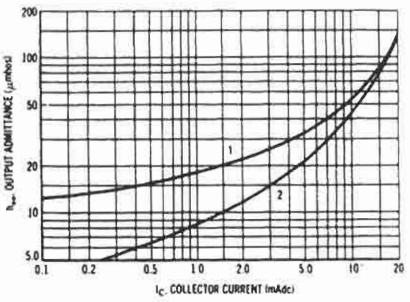


FIGURE 10 – OUTPUT ADMITTANCE



2N2218,A, 2N2219,A, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

SWITCHING TIME CHARACTERISTICS

FIGURE 11 – TURN-ON TIME

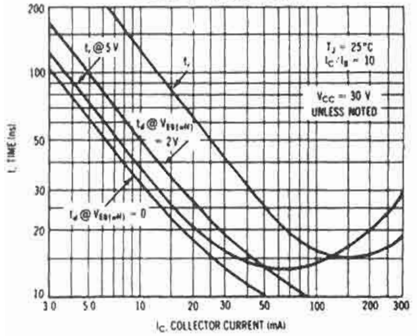


FIGURE 12 – CHARGE DATA

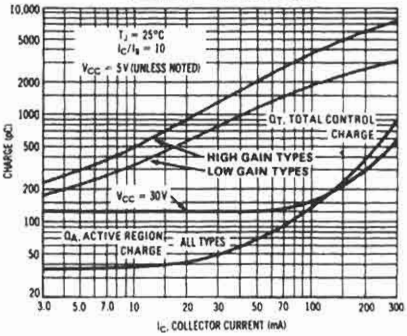


FIGURE 13 – TURN OFF BEHAVIOR

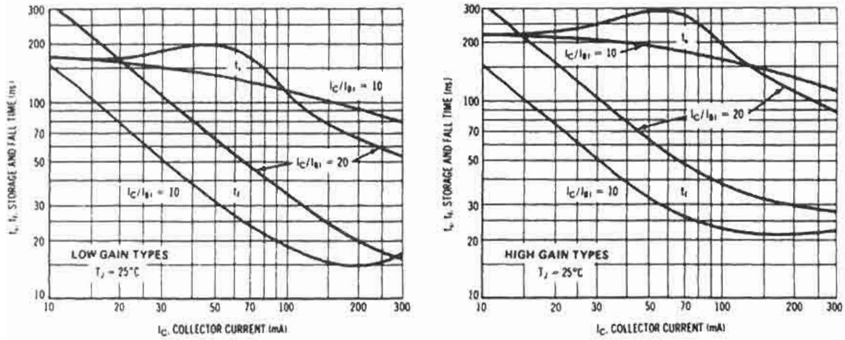
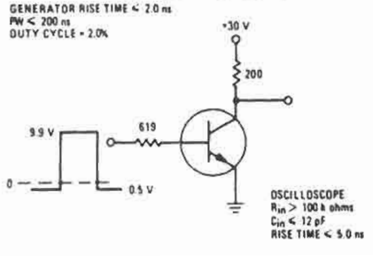


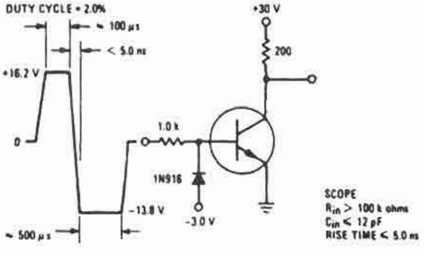
FIGURE 14 – DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT


GENERATOR RISE TIME ≤ 2.0 ns
PW < 200 ns
DUTY CYCLE = 2.0%

+30 V
200
619
9.9 V
0
0.5 V

OSCILLOSCOPE
$R_{in} > 100$ k ohms
$C_{in} \leq 12$ pF
RISE TIME < 5.0 ns

FIGURE 15 – STORAGE TIME AND FALL TIME EQUIVALENT TEST CIRCUIT


DUTY CYCLE = 2.0%

≈ 100 μs
< 5.0 ns
+16.2 V
0
−13.8 V
≈ 500 μs
+30 V
200
1.0 k
1N916
−3.0 V

SCOPE
$R_{in} > 100$ k ohms
$C_{in} \leq 12$ pF
RISE TIME < 5.0 ns

2N2218,A, 2N2219,A, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

FIGURE 16 – CURRENT-GAIN–BANDWIDTH PRODUCT AND COLLECTOR-BASE TIME CONSTANT DATA

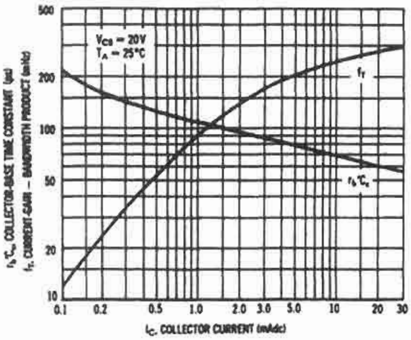


FIGURE 17 – CAPACITANCES

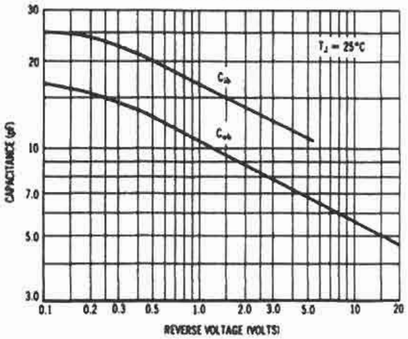
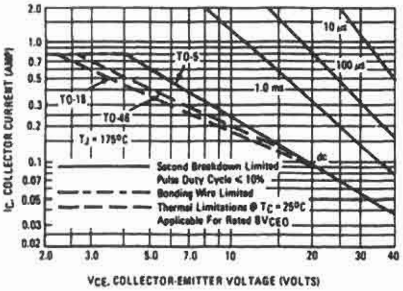


FIGURE 18 – ACTIVE-REGION SAFE OPERATING AREAS

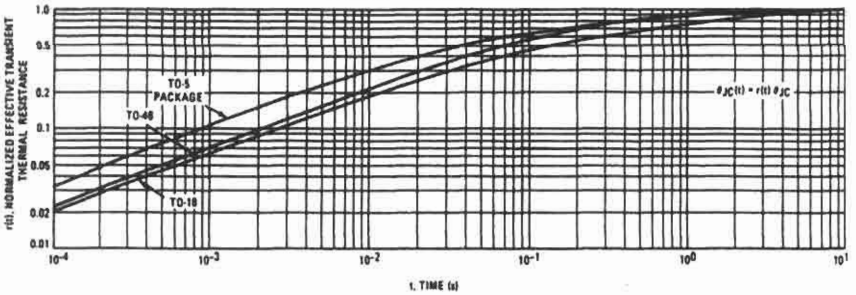


This graph shows the maximum I_C-V_{CE} limits of the device both from the standpoint of thermal dissipation (at 25°C case temperature), and secondary breakdown. For case temperatures other than 25°C, the thermal dissipation curve must be modified in accordance with the derating factor in the Maximum Ratings table.

To avoid possible device failure, the collector load line must fall below the limits indicated by the applicable curve. Thus, for certain operating conditions the device is thermally limited, and for others it is limited by secondary breakdown.

For pulse applications, the maximum I_C-V_{CE} product indicated by the dc thermal limits can be exceeded. Pulse thermal limits may be calculated by using the transient thermal resistance curve of Figure 19.

FIGURE 19 – THERMAL RESPONSE



2N2223, A

For Specifications, See 2N2060 Data.

APPENDIX 4

Data sheets for the Motorola MC1741SC op amp (pages 2-175 through 2-180). Copyright of Motorola, Inc. Used by permission.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1741S
MC1741SC

HIGH SLEW RATE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

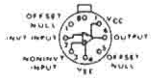
The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate – 10 V/μs Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

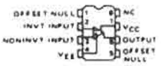
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601


OFFSET NULL
8O
1
VCC
INVT INPUT
OUTPUT
NONINVT INPUT
VEE
OFFSET NULL
2
3
4
5
6
7

(Top View)


OFFSET NULL
INVT INPUT
NONINVT INPUT
VEE
NC
VCC
OUTPUT
OFFSET NULL
1
2
3
4
5
6
7
8

(Top View)

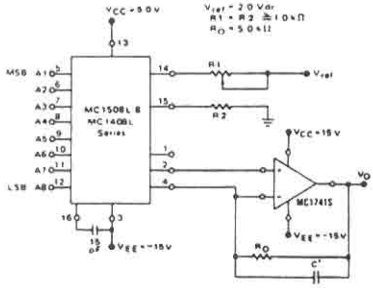
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1741SG	–55°C to +125°C	Metal Can
MC1741SCD MC1741SCG MC1741SCP1	0°C to +70°C	SO-8 Metal Can Plastic DIP

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER


VCC = 5.0 V
Vref = 2.0 Vdc
R1 = R2 ≈ 1.0 kΩ
RO = 5.0 kΩ
13
MSB A1
A2
A3
A4
A5
A6
A7
LSB A8
5
6
7
8
9
10
11
12
MC1508L 8
MC1408L
Series
14
15
1
2
4
R1
Vref
R2
VCC = 15 V
VO
MC1741S
VEE = –15V
16
3
15 pF
VEE = –15V
RO
C*

Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 150 pF).

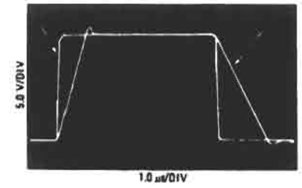
Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

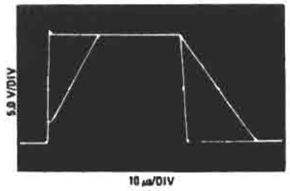
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right] = 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

MC1741S LARGE-SIGNAL TRANSIENT RESPONSE

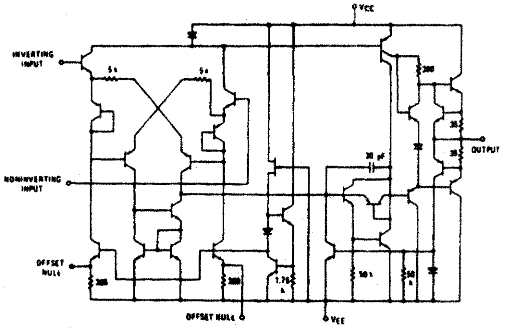


STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



MC1741S, MC1741SC

CIRCUIT SCHEMATIC


VCC
INVERTING INPUT
5 k
5 k
30 pF
OUTPUT
NONINVERTING INPUT
OFFSET NULL
1.75 k
50 k
50 k
OFFSET NULL
VEE

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MC1741SC	MC1741S	
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	+22 −22	Vdc
Differential Input Signal Voltage	V_{ID}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation)	P_D			
Metal Package		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Plastic Dual In-Line Package		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	−55 to +125	°C
Storage Temperature Range	T_{stg}			°C
Metal Package		−65 to +150		
Plastic Package		−55 to +125		

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

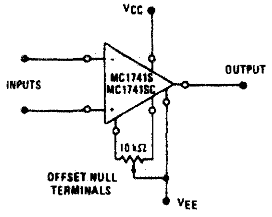
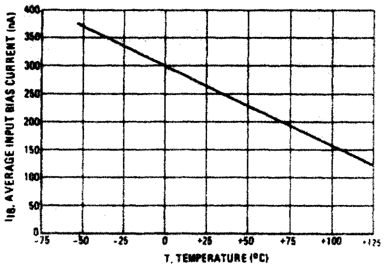

VCC
INPUTS
−
+
MC1741S
MC1741SC
OUTPUT
10 kΩ
OFFSET NULL TERMINALS
VEE

FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



MC1741S, MC1741SC

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1741S			MC1741SC			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3)	BW_p							kHz
A_v = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)		150	200	–	150	200	–	
Large-Signal Transient Response								
Slew Rate (Figures 10 and 11)	SR							
V(−) to V(+)		10	20	–	10	20	–	V/µs
V(+) to V(−)		10	12	–	10	12	–	
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	µs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8)								
Rise Time	t_{TLH}	–	0.25	–	–	0.25	–	µs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	µs
Propagation Delay Time	t_{PLH}, t_{PHL}	–	0.25	–	–	0.25	–	µs
Overshoot	OS	–	20	–	–	20	–	%
Short-Circuit Output Currents	I_{OS}	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4)	A_{vol}							–
V_O = ±10 V, T_A = +25°C		50,000	200,000	–	20,000	100,000	–	
V_O = ±10 V, T_A = T_{low}* to T_{high}*		25,000	–	–	15,000	–	–	
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing	V_O							V_{pk}
R_L = 10 kΩ, T_A = T_{low} to T_{high} (MC1741S only)		±12	±14	–	±12	±14	–	
R_L = 2.0 kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
R_L = 2.0 kΩ, T_A = T_{low} to T_{high}		±10	–	–	±10	–	–	
Input Common-Mode Voltage Range T_A = T_{low} to T_{high} (MC1741S)	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz) T_A = T_{low} to T_{high} (MC1741S)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}							nA
T_A = +25°C and T_{high}		–	200	500	–	200	500	
T_A = T_{low}		–	600	1500	–	–	800	
Input Offset Current	$\lvert I_{IO} \rvert$							nA
T_A = +25°C and T_{high}		–	30	200	–	30	200	
T_A = T_{low}		–	–	500	–	–	300	
Input Offset Voltage (R_S = ≤ 10 kΩ)	$\lvert V_{IO} \rvert$							mV
T_A = +25°C		–	1.0	5.0	–	2.0	6.0	
T_A = T_{low} to T_{high}		–	–	6.0	–	–	7.5	
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0) T_A = T_{low} to T_{high}	P_C	–	50	85	–	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant) T_A = T_{low} to T_{high} on MC1741S	PSS+	–	2.0	100	–	2.0	150	µV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS−	–	10	150	–	10	150	µV/V

*T_{low} = 0 for MC1741SC
= −55 °C for MC1741S

T_{high} = +70°C for MC1741SC
= +125 °C for MC1741S

MC1741S, MC1741SC

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

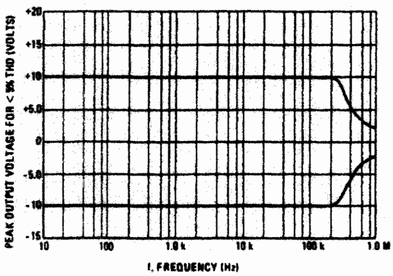


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

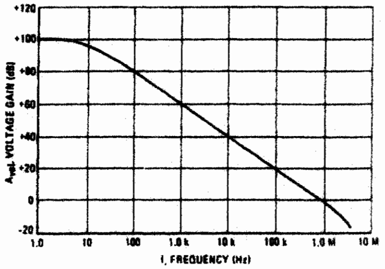


FIGURE 5 – NOISE versus FREQUENCY

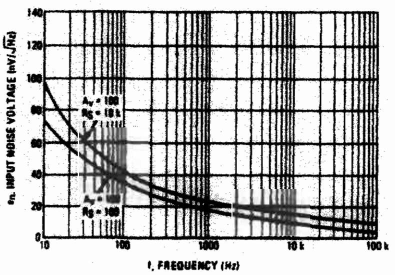


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

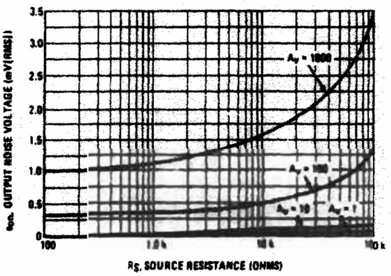


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

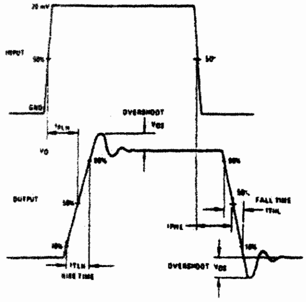
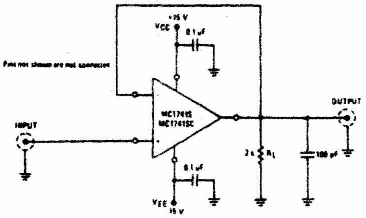

20 mV
INPUT
50%
50%
GND
OVERSHOOT
VOS
tPLH
VO
90%
90%
OUTPUT
50%
50%
FALL TIME
tTHL
tPHL
10%
10%
tTLH
RISE TIME
OVERSHOOT VOS

FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT


+15 V
VCC
0.1 µF
Pins not shown are not connected
MC1741S
MC1741SC
INPUT
OUTPUT
2 k
RL
100 pF
0.1 µF
VEE
-15 V

MC1741S, MC1741SC

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

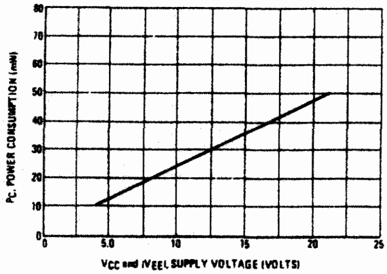


FIGURE 10 – LARGE-SIGNAL TRANSIENT WAVEFORMS

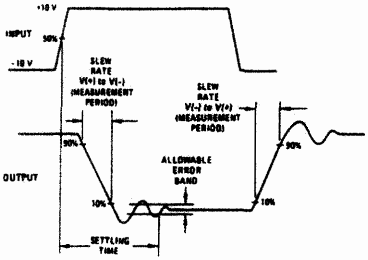
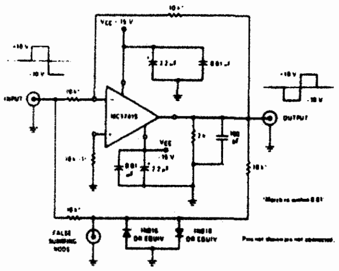

+10 V
INPUT
90%
-10 V
SLEW RATE V(+) to V(-) (MEASUREMENT PERIOD)
SLEW RATE V(-) to V(+) (MEASUREMENT PERIOD)
90%
90%
OUTPUT
ALLOWABLE ERROR BAND
10%
10%
SETTLING TIME

FIGURE 11 – SETTLING TIME AND SLEW RATE TEST CIRCUIT


10 k
VCC +15 V
+10 V
-10 V
2.2 µF
0.01 µF
+10 V
-10 V
INPUT
10 k
MC1741S
OUTPUT
VEE
-15 V
1 k
100 pF
0.01 µF
2.2 µF
10 k
10 k
FALSE SUMMING NODE
1N916 OR EQUIV
1N916 OR EQUIV
Pins not shown are not connected.

SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

MC1741S, MC1741SC

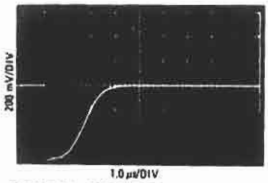


FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

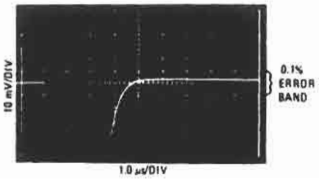


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE

TYPICAL APPLICATION

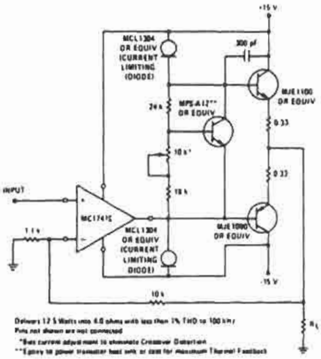


FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER

+15 V
MCL1304 OR EQUIV (CURRENT LIMITING DIODE)
300 pF
MJE1100 OR EQUIV
24 k
MPS-A12** OR EQUIV
0.33
10 k*
0.33
INPUT
15 k
MC1741S
1.1 k
MCL1304 OR EQUIV (CURRENT LIMITING DIODE)
MJE1090 OR EQUIV
-15 V
10 k
R_L

Delivers 12.5 Watts into 4.0 ohms with less than 1% THD to 100 kHz
Pins not shown are not connected
*Bias current adjustment to eliminate Crossover Distortion
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback

APPENDIX 5

Data sheets for the Motorola 1N5221 through 1N5281 (pages 1-21 through 1-26). Copyright of Motorola, Inc. Used by permission.

1N5221 (SILICON)
thru
1N5281
series

500 MILLIWATT SURMETIC▲ 20 SILICON ZENER DIODES (SILICON OXIDE PASSIVATED)

. . .in answer to the Circuit Design and Component Engineers' many requests – A complete new series of Zener Diodes in the popular DO-204AA case with higher ratings, tighter limits, better operating characteristics and a full set of designers' curves that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- Proven Capability to MIL-S-19500 Specifications
- 10 Watt Surge Rating
- Weldable Leads
- Maximum Limits Guaranteed on Six Electrical Parameters

{ .5M2.4Z610 thru .5M200Z610
1N5221A thru 1N5281A }

{ .5M2.4Z5 thru .5M200Z5 }

500 MILLIWATT
ZENER REGULATOR
DIODES

2.4 – 200 VOLTS

MAXIMUM RATINGS

Junction and Storage Temperature: –65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 500 mW @ T_L = 75°C, Lead Length = ⅜"
(Derate 4.0 mW/°C above 75°C)

Surge Power: 10 Watts (Non-recurrent square wave @ PW = 8.3 ms, T_A = 55°C, Figure 16)

MECHANICAL CHARACTERISTICS

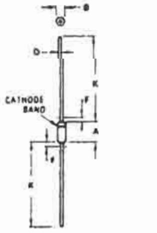
CASE: Void free, transfer molded, thermosetting plastic.

FINISH: All external surfaces are corrosion resistant. Leads are readily solderable and weldable.

POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any.

WEIGHT: 0.18 gram (approximately).

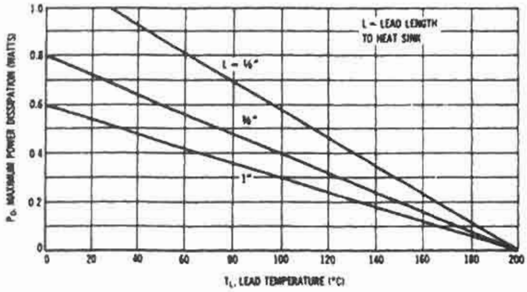


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F		1.27		0.050
K	25.40		1.000	

All JEDEC dimensions and notes apply

CASE 51-02
DO-204AA

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



▲Trademark of Motorola Inc

1N5221 thru 1N5281 series (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted). Based on dc measurements at thermal equilibrium; lead length = 3/8"; thermal resistance of heat sink = 30°C/W) $V_F = 1.1$ Max @ $I_F = 200$ mA for all types.

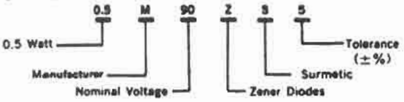
JEDEC Type No. (Note 1)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 2)	Test Current I_{ZT} mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current				Max Zener Voltage Temp. Coeff. (A & B Suffix Only) θ_{VZ} (% °C) (Note 3)
					A & B Suffix Only			Non-Suffix	
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ $I_{ZK} = 0.25$ mA Ohms	I_R µA	@ V_R Volts		I_R @ V_R Used For Suffix A µA	
						A	B		
1N5221	2.4	20	30	1200	100	0.95	1.0	200	-0.085
1N5222	2.5	20	30	1250	100	0.95	1.0	200	-0.085
1N5223	2.7	20	30	1300	75	0.95	1.0	150	-0.080
1N5224	2.8	20	30	1400	75	0.95	1.0	150	-0.080
1N5225	3.0	20	29	1600	50	0.95	1.0	100	-0.075
1N5226	3.3	20	28	1600	25	0.95	1.0	100	-0.070
1N5227	3.6	20	24	1700	15	0.95	1.0	100	-0.065
1N5228	3.9	20	23	1900	10	0.95	1.0	75	-0.060
1N5229	4.3	20	22	2000	5.0	0.95	1.0	50	+0.055
1N5230	4.7	20	19	1900	5.0	1.9	2.0	50	+0.030
1N5231	5.1	20	17	1600	5.0	1.9	2.0	50	+0.030
1N5232	5.6	20	11	1600	5.0	2.9	3.0	50	+0.038
1N5233	6.0	20	7.0	1600	5.0	3.3	3.5	50	+0.038
1N5234	6.2	20	7.0	1000	5.0	3.8	4.0	50	+0.045
1N5235	6.8	20	5.0	750	3.0	4.8	5.0	30	+0.050
1N5236	7.5	20	6.0	500	3.0	5.7	6.0	30	+0.058
1N5237	8.2	20	8.0	500	3.0	6.2	6.5	30	+0.062
1N5238	8.7	20	8.0	600	3.0	6.2	6.5	30	+0.065
1N5239	9.1	20	10	600	3.0	6.7	7.0	30	+0.068
1N5240	10	20	17	600	3.0	7.6	8.0	30	+0.075
1N5241	11	20	22	600	2.0	8.0	8.4	30	+0.076
1N5242	12	20	30	600	1.0	8.7	9.1	10	+0.077
1N5243	13	9.5	13	600	0.5	9.4	9.9	10	+0.079
1N5244	14	9.0	15	600	0.1	9.5	10	10	+0.082
1N5245	15	8.5	16	600	0.1	10.5	11	10	+0.082
1N5246	16	7.8	17	600	0.1	11.4	12	10	+0.083
1N5247	17	7.4	19	600	0.1	12.4	13	10	+0.084
1N5248	18	7.0	21	600	0.1	13.3	14	10	+0.085
1N5249	19	6.6	23	600	0.1	13.3	14	10	+0.086
1N5250	20	6.2	25	600	0.1	14.3	15	10	+0.086
1N5251	22	5.6	29	600	0.1	16.2	17	10	+0.087
1N5252	24	5.2	33	600	0.1	17.1	18	10	+0.088
1N5253	25	5.0	35	600	0.1	18.1	19	10	+0.089
1N5254	27	4.6	41	600	0.1	20	21	10	+0.090
1N5255	28	4.5	44	600	0.1	20	21	10	+0.091
1N5256	30	4.2	49	600	0.1	22	23	10	+0.091
1N5257	33	3.8	58	700	0.1	24	25	10	+0.092
1N5258	36	3.4	70	700	0.1	26	27	10	+0.093
1N5259	39	3.2	80	800	0.1	29	30	10	+0.094
1N5260	43	3.0	93	900	0.1	31	33	10	+0.095
1N5261	47	2.7	105	1000	0.1	34	36	10	+0.095
1N5262	51	2.5	125	1100	0.1	37	39	10	+0.096
1N5263	56	2.2	150	1300	0.1	41	43	10	+0.096
1N5264	60	2.1	170	1400	0.1	44	46	10	+0.097
1N5265	62	2.0	185	1400	0.1	45	47	10	+0.097
1N5266	68	1.8	230	1600	0.1	49	52	10	+0.097
1N5267	75	1.7	270	1700	0.1	53	56	10	+0.098
1N5268	82	1.5	330	2000	0.1	59	62	10	+0.098
1N5269	87	1.4	370	2200	0.1	65	68	10	+0.099
1N5270	91	1.4	400	2300	0.1	66	69	10	+0.099
1N5271	100	1.3	500	2600	0.1	72	76	10	+0.110
1N5272	110	1.1	750	3000	0.1	80	84	10	+0.110
1N5273	120	1.0	900	4000	0.1	86	91	10	+0.110
1N5274	130	0.95	1100	4500	0.1	94	99	10	+0.110
1N5275	140	0.90	1300	4500	0.1	101	106	10	+0.110
1N5276	150	0.85	1500	5000	0.1	108	114	10	+0.110
1N5277	160	0.80	1700	5500	0.1	116	122	10	+0.110
1N5278	170	0.74	1900	5500	0.1	123	129	10	+0.110
1N5279	180	0.68	2200	6000	0.1	130	137	10	+0.110
1N5280	190	0.66	2400	6500	0.1	137	144	10	+0.110
1N5281	200	0.65	2500	7000	0.1	144	152	10	+0.110

NOTE 1 – TOLERANCE AND VOLTAGE DESIGNATION

Tolerance designation — The JEDEC type numbers shown indicate a tolerance of ±10% with guaranteed limits on only V_Z, I_R and V_F as shown in the above table. Units with guaranteed limits on all six parameters are indicated by suffix "A" for ±10% tolerance and suffix "B" for ±5.0% units.

Non-Standard voltage designation — To designate units with zener voltages other than those assigned JEDEC numbers, the type number should be used.

EXAMPLE:



NOTE 2 – SPECIAL SELECTIONS AVAILABLE INCLUDE:

1 — Nominal zener voltages between those shown.

2 — Matched sets: (Standard Tolerances are ±5.0%, ±3.0%, ±2.0%, ±1.0%) depending on voltage per device.

a. Two or more units for series connection with specified tolerance on total voltage. Series matched sets make zener voltages in excess of 200 volts possible as well as providing lower temperature coefficients, lower dynamic impedance and greater power handling ability.

b. Two or more units matched to one another with any specified tolerance.

3 — Tight voltage tolerances: 1.0%, 2.0%, 3.0%.

NOTE 3 – TEMPERATURE COEFFICIENT (θ_{VZ})

Test conditions for temperature coefficient are as follows:

a. $I_{ZT} = 7.5$ mA, $T_1 = 25°C$,
$T_2 = 125°C$ (1N5221A, B thru 1N5242A, B.)

b. I_{ZT} = Rated I_{ZT}, $T_1 = 25°C$,
$T_2 = 125°C$ (1N5243A, B thru 1N5281A, B.)

Device to be temperature stabilized with current applied prior to reading breakdown voltage at the specified ambient temperature.

1N5221 thru 1N5281 series (continued)

TYPICAL REVERSE CHARACTERISTICS FOR SELECTED ZENER DIODES

Curves marked T_A were obtained from dc measurements at thermal equilibrium; lead length = ⅜"; thermal resistance of heat sink = 30°C/W.
Curves marked T_J were obtained from pulse tests; mounting conditions are not a factor.

$V_{Z(Nominal)} = 3.3$ Volts

FIGURE 2

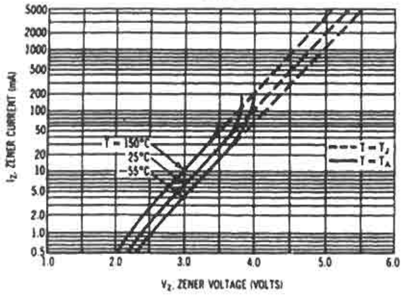
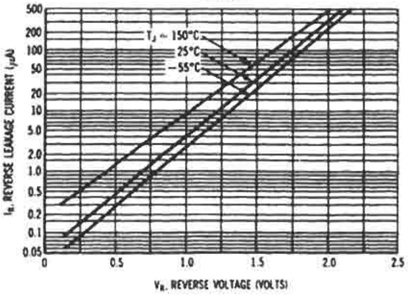


FIGURE 3



$V_{Z(Nominal)} = 5.1$ Volts

FIGURE 4

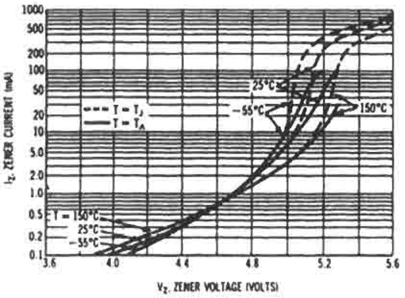
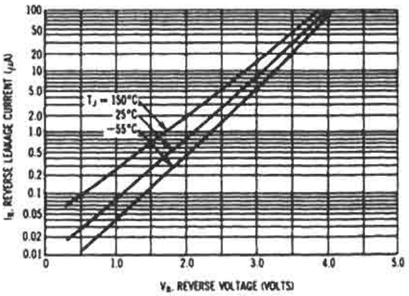


FIGURE 5



$V_{Z(Nominal)} = 27$ Volts

FIGURE 6

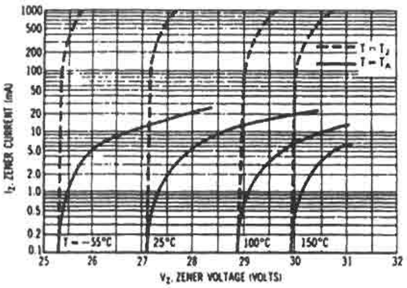
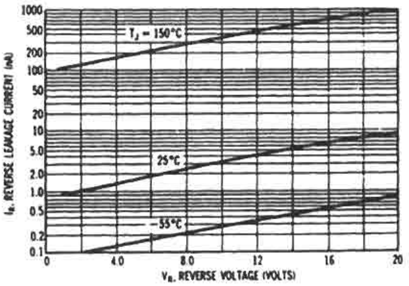


FIGURE 7



1N5221 thru 1N5281 series (continued)

TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION

(90% of the units are in the ranges indicated)

FIGURE 8 — RANGE FOR UNITS TO 12 VOLTS

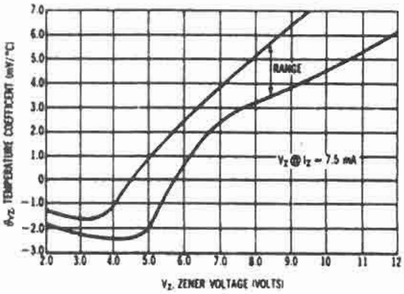


FIGURE 9 — RANGE FOR UNITS 12 TO 200 VOLTS

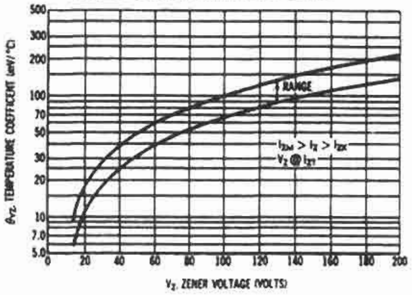


FIGURE 10 — EFFECT OF ZENER CURRENT

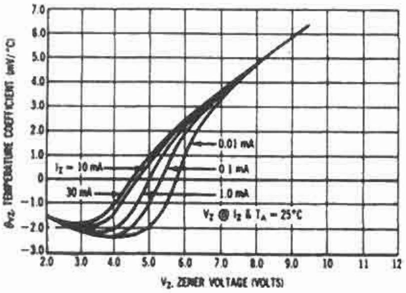
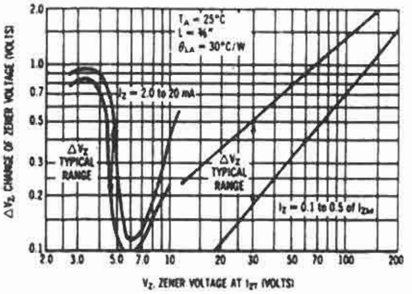


FIGURE 11 — VOLTAGE REGULATION



TYPICAL ZENER IMPEDANCE

FIGURE 12 — EFFECT OF ZENER CURRENT

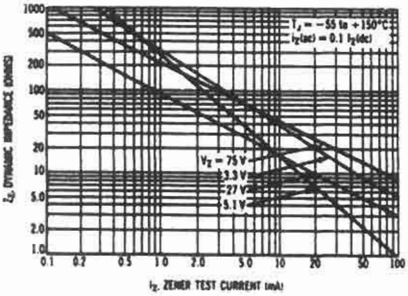
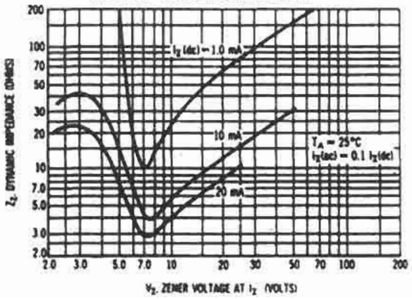


FIGURE 13 — EFFECT OF ZENER VOLTAGE



1N5221 thru 1N5281 Series (continued)

FIGURE 14 — TYPICAL THERMAL RESPONSE

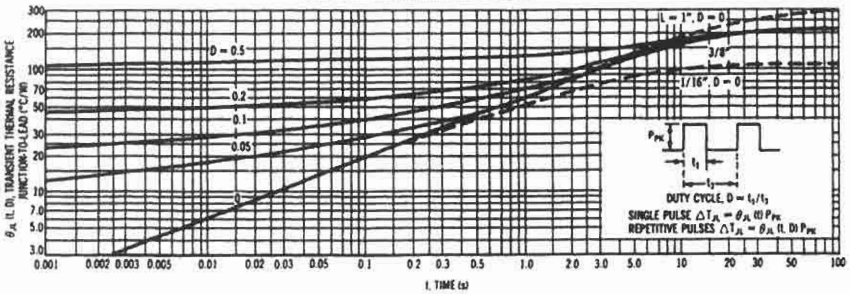


FIGURE 15 — TYPICAL THERMAL RESISTANCE

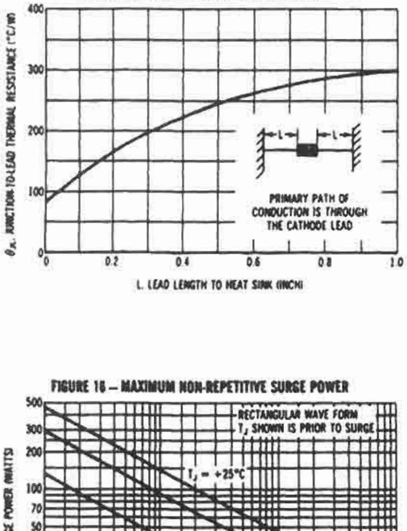
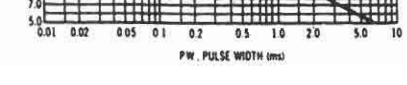


FIGURE 16 — MAXIMUM NON-REPETITIVE SURGE POWER



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions, in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance and P_D is the power dissipation. θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use and for printed circuit board wiring.

Junction Temperature, T_J, may be found from:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 14 for a train of power pulses or from Figure 15 for dc power.

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of T_J (ΔT_J) may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figures 8, 9, and 10.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, use short leads, especially to the cathode, and keep current excursions as low as possible.

Data of Figure 14 should not be used to compute surge capability. Surge limitations are given in Figure 16. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 16 be exceeded.

1N5221 thru 1N5281 Series (continued)

FIGURE 17 — TYPICAL CAPACITANCE

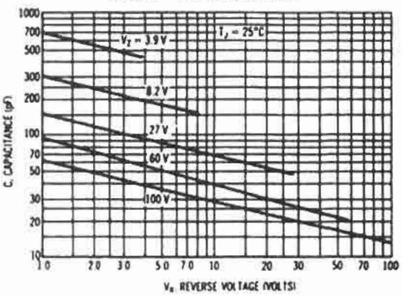


FIGURE 18 — TYPICAL FORWARD CHARACTERISTICS

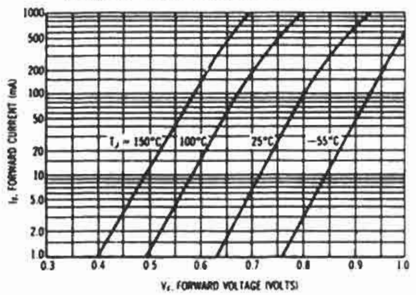


FIGURE 19 — TYPICAL NOISE DENSITY

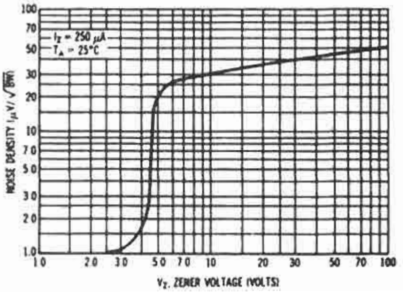
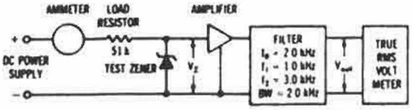


FIGURE 20 — NOISE DENSITY MEASUREMENT METHOD


AMMETER
LOAD RESISTOR
AMPLIFIER
+
−
DC POWER SUPPLY
51 k
TEST ZENER
V_Z
FILTER
f_0 = 2.0 kHz
f_1 = 1.0 kHz
f_2 = 3.0 kHz
BW = 2.0 kHz
V_{out}
TRUE RMS VOLT METER

NOISE DENSITY (VOLTS PER SQUARE ROOT BANDWIDTH) = $\dfrac{V_{out}}{\text{OVERALL GAIN} \sqrt{BW}}$

WHERE: BW = FILTER BANDWIDTH (Hz)
V_{out} = OUTPUT NOISE (VOLTS RMS)

The input voltage and load resistance are high so that the zener diode is driven from a constant current source. The amplifier is low noise so that the amplifier noise is negligible compared to that of the test zener. The filter bandpass is known so that the noise density can be calculated from the formula shown. The data of Figure 19 and the formula can also be used to find noise for any system bandwidth.

APPENDIX 6

Table A6.1 lists the approximate electrical characteristics for the 1N914A diode. This device or its equivalent is available from multiple manufacturers.

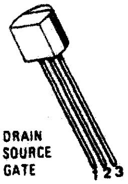
TABLE A6.1 Approximate Ratings for a 1N914A Diode

Parameter	*Rating*
Peak inverse voltage	75 volts
Average forward current	75 milliamps (below 25°C) 10 milliamps (at 150°C)
Reverse current	25 nanoamps (at 25°C) 50 microamps (at 150°C)
Power dissipation	250 milliwatts
Capacitance	4 picofarads
Reverse recovery time	8 nanoseconds

APPENDIX 7

Data sheet for the Motorola MPF102 transistor (page 3-724). Copyright of Motorola, Inc. Used by permission.

MPF102 (SILICON)



PIN 1. DRAIN
2. SOURCE
3. GATE

CASE 29 (5)
(TO-92)

Drain and Source may be interchanged

Silicon N-channel junction field-effect transistor designed for VHF amplifier and mixer applications.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D (1)	310 2.82	mW mW/°C
Operating Junction Temperature	T_J (1)	125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	BV_{GSS}	25	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0) (V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100 C)	I_{GSS}	 — —	 2.0 2.0	 nAdc μAdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 2.0 nAdc)	$V_{GS(off)}$	—	8.0	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 0.2 mAdc)	V_{GS}	0.5	7.5	Vdc
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	2.0	20	mAdc
DYNAMIC CHARACTERISTICS				
Forward Transfer Admittance (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	$\lvert y_{fs} \rvert$	2000	7500	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.0	pF
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$\lvert y_{fs} \rvert$	1600	—	μmhos
Input Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{is})$	—	800	μmhos
Output Conductance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	$Re(y_{os})$	—	200	μmhos

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

(1) Continuous package improvements have enhanced these guaranteed Maximum Ratings as follows: P_D = 1.0 W @ T_C = 25°C, Derate above 25°C – 8.0 mW/°C, T_J = -65 to +150°C, θ_{JC} = 125° C/W.

APPENDIX 8

Data sheets for the Motorola 1N4728 through 1N4764 zener diodes (pages 1-105 through 1-109). Copyright of Motorola, Inc. Used by permission.

1N4728 thru 1N4764 (SILICON)
1M110ZS10 thru 1M200ZS10

Designers Data Sheet

1.0 WATT SURMETIC 30 SILICON ZENER DIODES

. . . a complete series of 1.0 Watt Zener Diodes with limits and operating characteristics that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

- To 80 Watts Surge Rating @ 1.0 ms
- Maximum Limits Guaranteed on Six Electrical Parameters
- Package No Larger Than the Conventional 400 mW Package

Designer's Data for "Worst Case" Conditions

The Designers Data sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

1.0 WATT
ZENER REGULATOR DIODES
3.3–200 VOLTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*DC Power Dissipation @ $T_A = 50^oC$ Derate above 50^oC	P_D	1.0 6.67	Watt mW/°C
DC Power Dissipation @ $T_L = 75^oC$ Lead Length = 3/8" Derate above 75^oC	P_D	3.0 24	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

MECHANICAL CHARACTERISTICS

CASE: Void-free, transfer-molded, thermosetting plastic

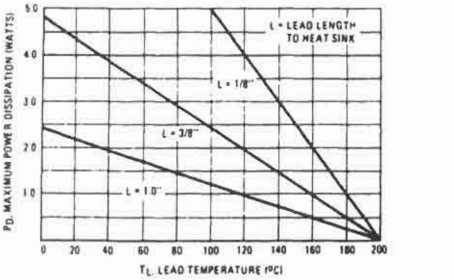
FINISH: All external surfaces are corrosion resistant and leads are readily solderable and weldable

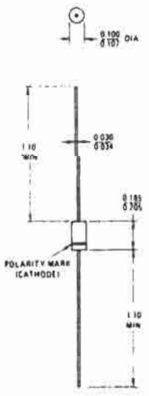
POLARITY: Cathode indicated by polarity band. When operated in zener mode, cathode will be positive with respect to anode

MOUNTING POSITION: Any

WEIGHT: 0.4 gram (approx)

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





To convert inches to millimeters multiply by 25.4
All JEDEC dimensions and notes apply

CASE 59
DO-41

*Indicates JEDEC Registered Data

1N4728 thru 1N4764 (continued)
1M110ZS10 thru 1M200ZS10

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) *V_F = 1.5 V max, I_F = 200 mA for all types

JEDEC Type No. (Note 1)	Motorola Type No. (Note 2)	*Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 2 & 3)	*Test Current I_{ZT} mA	*Max Zener Impedance (Note 4)			*Leakage Current		*Surge Current @ T_A = 25°C i_r – mA (Note 5)
				Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} Ohms	I_{ZK} mA	I_R µA Max	@ V_R Volts	
1N4728	1M3.3ZS10	3.3	76	10	400	1.0	100	1.0	1380
1N4729	1M3.6ZS10	3.6	69	10	400	1.0	100	1.0	1260
1N4730	1M3.9ZS10	3.9	64	9.0	400	1.0	50	1.0	1190
1N4731	1M4.3ZS10	4.3	58	9.0	400	1.0	10	1.0	1070
1N4732	1M4.7ZS10	4.7	53	8.0	500	1.0	10	1.0	970
1N4733	1M5.1ZS10	5.1	49	7.0	550	1.0	10	1.0	890
1N4734	1M5.6ZS10	5.6	45	5.0	600	1.0	10	2.0	810
1N4735	1M6.2ZS10	6.2	41	2.0	700	1.0	10	3.0	730
1N4736	1M6.8ZS10	6.8	37	3.5	700	1.0	10	4.0	660
1N4737	1M7.5ZS10	7.5	34	4.0	700	0.5	10	5.0	605
1N4738	1M8.2ZS10	8.2	31	4.5	700	0.5	10	6.0	550
1N4739	1M9.1ZS10	9.1	28	5.0	700	0.5	10	7.0	500
1N4740	1M10ZS10	10	25	7.0	700	0.25	10	7.6	454
1N4741	1M11ZS10	11	23	8.0	700	0.25	5.0	8.4	414
1N4742	1M12ZS10	12	21	9.0	700	0.25	5.0	9.1	380
1N4743	1M13ZS10	13	19	10	700	0.25	5.0	9.9	344
1N4744	1M15ZS10	15	17	14	700	0.25	5.0	11.4	304
1N4745	1M16ZS10	16	15.5	16	700	0.25	5.0	12.2	285
1N4746	1M18ZS10	18	14	20	750	0.25	5.0	13.7	250
1N4747	1M20ZS10	20	12.5	22	750	0.25	5.0	15.2	225
1N4748	1M22ZS10	22	11.5	23	750	0.25	5.0	16.7	205
1N4749	1M24ZS10	24	10.5	25	750	0.25	5.0	18.2	190
1N4750	1M27ZS10	27	9.5	35	750	0.25	5.0	20.6	170
1N4751	1M30ZS10	30	8.5	40	1000	0.25	5.0	22.8	150
1N4752	1M33ZS10	33	7.5	45	1000	0.25	5.0	25.1	135
1N4753	1M36ZS10	36	7.0	50	1000	0.25	5.0	27.4	125
1N4754	1M39ZS10	39	6.5	60	1000	0.25	5.0	29.7	115
1N4755	1M43ZS10	43	6.0	70	1500	0.25	5.0	32.7	110
1N4756	1M47ZS10	47	5.5	80	1500	0.25	5.0	35.8	95
1N4757	1M51ZS10	51	5.0	95	1500	0.25	5.0	38.8	90
1N4758	1M56ZS10	56	4.5	110	2000	0.25	5.0	42.6	80
1N4759	1M62ZS10	62	4.0	125	2000	0.25	5.0	47.1	70
1N4760	1M68ZS10	68	3.7	150	2000	0.25	5.0	51.7	65
1N4761	1M75ZS10	75	3.3	175	2000	0.25	5.0	56.0	60
1N4762	1M82ZS10	82	3.0	200	3000	0.25	5.0	62.2	55
1N4763	1M91ZS10	91	2.8	250	3000	0.25	5.0	69.2	50
1N4764	1M100ZS10	100	2.5	350	3000	0.25	5.0	76.0	45
–	1M110ZS10	110	2.3	450	4000	0.25	5.0	83.6	–
–	1M120ZS10	120	2.0	550	4500	0.25	5.0	91.2	–
–	1M130ZS10	130	1.9	700	5000	0.25	5.0	98.8	–
–	1M150ZS10	150	1.7	1000	6000	0.25	5.0	114.0	–
–	1M160ZS10	160	1.6	1100	6500	0.25	5.0	121.6	–
–	1M180ZS10	180	1.4	1200	7000	0.25	5.0	136.8	–
–	1M200ZS10	200	1.2	1500	8000	0.25	5.0	152.0	–

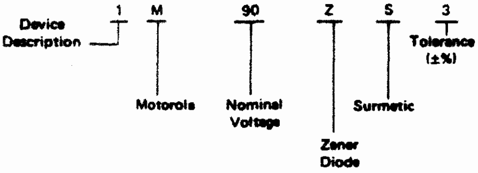
*Indicates JEDEC Registered Data

NOTE 1 – TOLERANCE AND TYPE NUMBER DESIGNATION

The JEDEC type numbers listed have a standard tolerance on the nominal zener voltage of ±10%. A standard tolerance of ±5% on individual units is also available and is indicated by suffixing "A" to the standard type number.

NOTE 2 – SPECIALS AVAILABLE INCLUDE:

(A) NOMINAL ZENER VOLTAGES BETWEEN THE VOLTAGES SHOWN AND TIGHTER VOLTAGE TOLERANCES: To designate units with zener voltages other than those assigned JEDEC numbers and/or tight voltage tolerances (±5%, ±3%, ±2%, ±1%), the Motorola type number should be used.

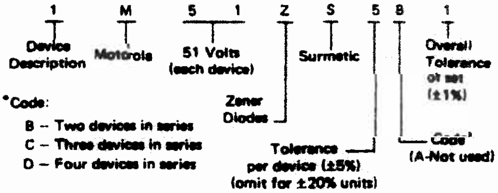


Example: 1M90ZS3

(B) MATCHED SETS: (Standard Tolerances are ±5.0%, ±3.0%, ±2.0%, ±1.0%).

Zener diodes can be obtained in sets consisting of two or more matched devices. The method for specifying such matched sets is similar to the one described in (A), except that two extra suffixes are added to the code number described.

These units are marked with code letters to identify the matched sets and, in addition, each unit in a set is marked with the same serial number, which is different for each set being ordered.



*Code:

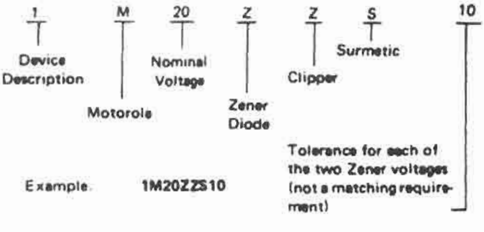
B – Two devices in series
C – Three devices in series
D – Four devices in series

Example: 1M51ZS5B1

1N4728 thru 1N4764 (continued)
1M110ZS10 thru 1M200ZS10

(C) ZENER CLIPPERS: (Standard Tolerance ±10% and ±5%).

Special clipper diodes with opposing Zener junctions built into the device are available by using the following nomenclature



NOTE 3 – ZENER VOLTAGE (V_Z) MEASUREMENT

Motorola guarantees the zener voltage when measured at 90 seconds while maintaining the lead temperature (T_L) at 30°C ± 1°C, 3/8" from the diode body.

NOTE 4 – ZENER IMPEDANCE (Z_Z) DERIVATION

The zener impedance is derived from the 60 cycle ac voltage, which results when an ac current having an rms value equal to 10% of the dc zener current (I_{ZT} or I_{ZK}) is superimposed on I_{ZT} or I_{ZK}.

NOTE 5 – SURGE CURRENT (i_r) NON-REPETITIVE

The rating listed in the electrical characteristics table is maximum peak, non-repetitive, reverse surge current of 1/2 square wave or equivalent sine wave pulse of 1/120 second duration superimposed on the test current, I_{ZT}, per JEDEC registration, however, actual device capability is as described in Figures 4 and 5.

APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance (°C/W) and P_D is the power dissipation. The value for θ_{LA} will vary and depends on the device mounting method. θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use and for printed circuit board wiring.

The temperature of the lead can also be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 2 for a train of power pulses (L = 3/8 inch) or from Figure 3 for dc power.

$$\Delta T_{JL} = \theta_{JL} P_D$$

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of $T_J(\Delta T_J)$ may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figures 6 and 7.

Under high power-pulse operation, the zener voltage will very with time and may also be affected significantly by the zener resistance. For best regulation, keep current excursions as low as possible.

Data of Figure 2 should not be used to compute surge capability. Surge limitations are given in Figure 4. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 4 be exceeded.

1N4728 thru 1N4764 (continued)
1M110ZS10 thru 1M200ZS10

FIGURE 2 – TYPICAL THERMAL RESPONSE, LEAD LENGTH L = 3/8 INCH

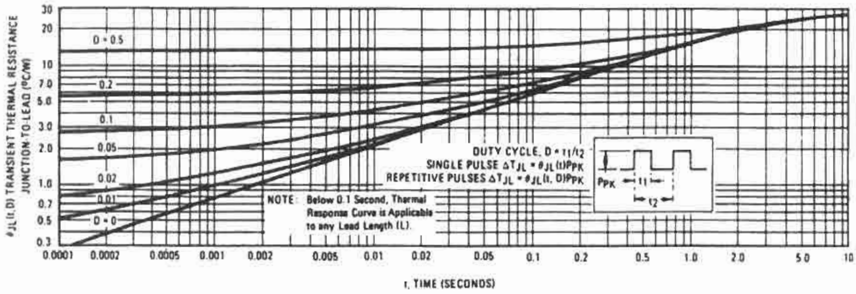


FIGURE 3 – TYPICAL THERMAL RESISTANCE

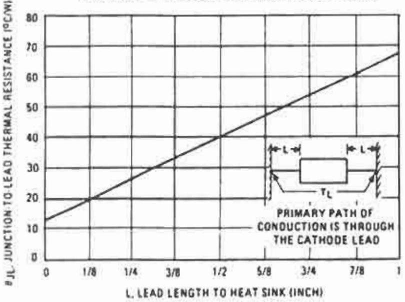


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE POWER

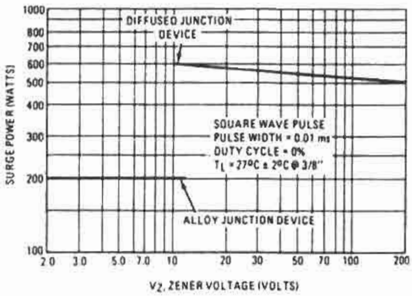
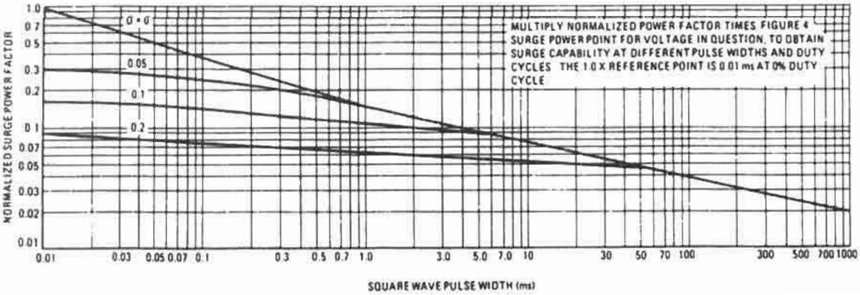


FIGURE 5 – SURGE POWER FACTOR



1N4728 thru 1N4764 (continued)
1M110ZS10 thru 1M200ZS10

TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION

(90% OF THE UNITS ARE IN THE RANGES INDICATED)

FIGURE 6 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS TO 12 VOLTS

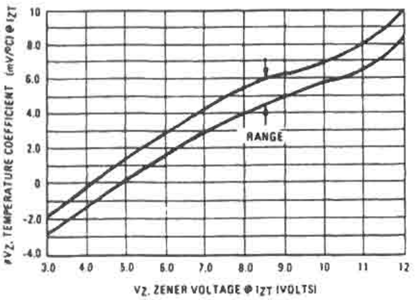


FIGURE 7 – TEMPERATURE COEFFICIENT-RANGE FOR UNITS 10 TO 200 VOLTS

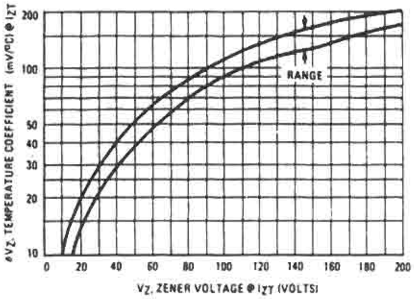


FIGURE 8 – VOLTAGE REGULATION

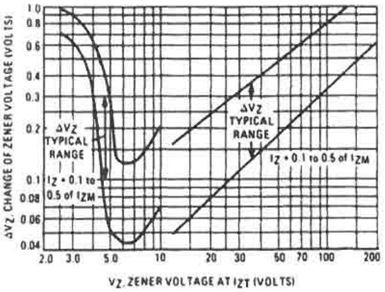
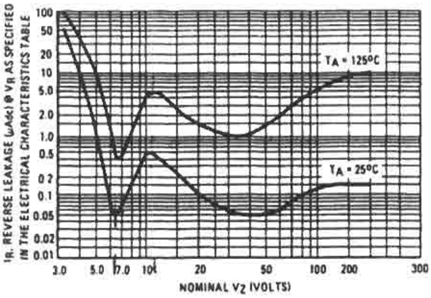


FIGURE 9 – MAXIMUM REVERSE LEAKAGE
(95% OF THE UNITS ARE BELOW THE VALUES SHOWN)



APPENDIX 9

Data sheets for the Motorola 2N3440 transistor (pages 2-509 through 2-512). Copyright of Motorola, Inc. Used by permission.

2N3439 (SILICON)
2N3440

NPN SILICON HIGH VOLTAGE POWER TRANSISTORS

. . . designed for use in consumer and industrial line-operated applications. These devices are particularly suited for audio, video and differential amplifiers as well as high-voltage, low-current inverters, switching and series pass regulators

- High DC Current Gain –
  h_{FE} = 40 - 160 @ I_C = 20 mAdc
- Current-Gain–Bandwidth Product –
  f_T = 15 MHz (Min) @ I_C = 10 mAdc
- Low Output Capacitance –
  C_{ob} = 10 pF (Max) @ f = 1.0 MHz

1 AMPERE
POWER TRANSISTORS
NPN SILICON

250-350 VOLTS
10 WATTS

*MAXIMUM RATINGS

Rating	Symbol	2N3439	2N3440	Unit
Collector Emitter Voltage	V_{CEO}	350	250	Vdc
Collector-Base Voltage	V_{CB}	450	300	Vdc
Emitter Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous	I_C	1.0		Adc
Base Current	I_B	0.5		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.7		Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 0.057		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

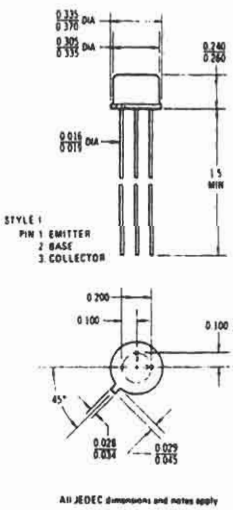
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	175	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	 2N3439 2N3440	$V_{CEO(sus)}$	 350 250		Vdc
Collector Cutoff Current (V_{CE} = 300 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	 2N3439 2N3440	I_{CEO}		 20 50	µAdc
Collector Cutoff Current (V_{CE} = 450 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 300 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 2N3439 2N3440	I_{CEX}		 500 500	µAdc
*Collector Cutoff Current (V_{CB} = 360 Vdc, I_E = 0) (V_{CB} = 250 Vdc, I_E = 0)	 2N3439 2N3440	I_{CBO}		 20 20	µAdc
*Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}		20	µAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc) *(I_C = 20 mAdc, V_{CE} = 10 Vdc)	 2N3439 Both Types	h_{FE}	 30 40	 160	
*Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{CE(sat)}$		0.5	Vdc
*Base-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{BE(sat)}$		1.3	Vdc
***DYNAMIC CHARACTERISTICS**					
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc)		f_T	15		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}		10	pF
Input Capacitance (V_{EB} = 5.0 Vdc, I_C = 0, f = 1.0 MHz)		C_{ib}	–	75	pF
Small-signal Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25		
Real Part of Common Emitter Small Signal Short-Circuit Input Impedance (V_{CE} = 10 Vdc, I_C = 5.0 mAdc, f = 1.0 MHz)		$Re(h_{ie})$	–	300	Ohms

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

All JEDEC dimensions and notes apply

CASE 31
TO-5

2N3439, 2N3440 (continued)

FIGURE 1 – DC CURRENT GAIN

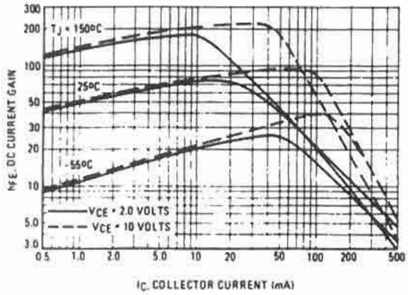


FIGURE 2 – SATURATION REGION

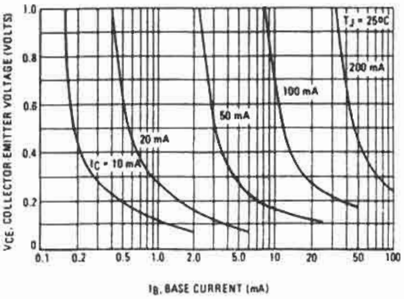


FIGURE 3 – "ON" VOLTAGES

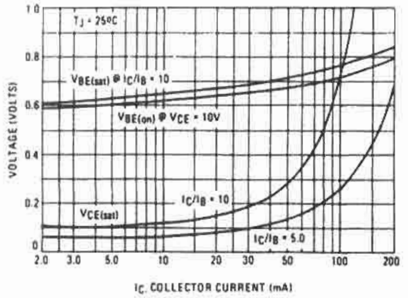


FIGURE 4 – TEMPERATURE COEFFICIENTS

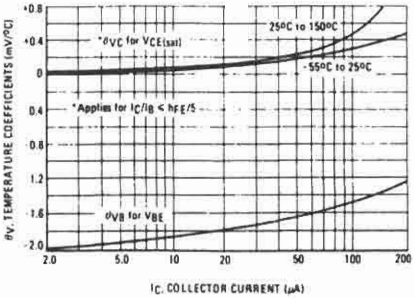


FIGURE 5 – EFFECTS OF BASE-EMITTER RESISTANCE

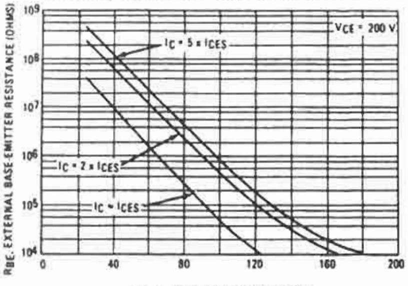
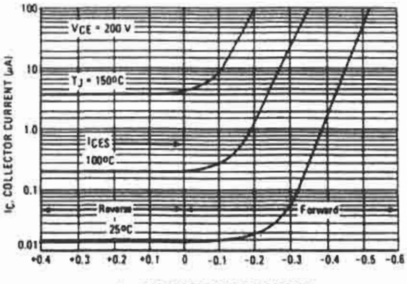


FIGURE 6 – CUT-OFF REGION



2N3439, 2N3440 (continued)

FIGURE 7 – TURN-ON TIME

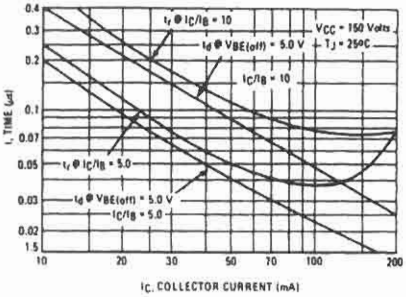


FIGURE 8 – TURN-OFF TIME

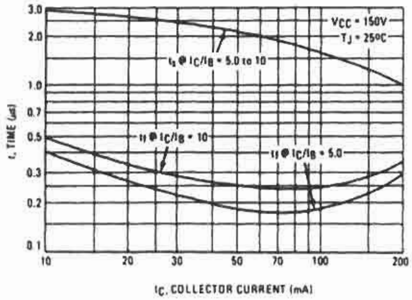
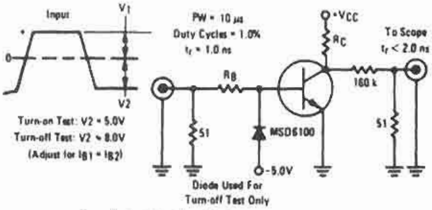


FIGURE 9 – SWITCHING TIME EQUIVALENT TEST CIRCUIT


Input
V_1
0
V_2
Turn-on Test: V2 = 5.0V
Turn-off Test: V2 ≈ 8.0V
(Adjust for $I_{B1} = I_{B2}$)
PW = 10 μs
Duty Cycles = 1.0%
t_r = 1.0 ns
R_B
51
MSD6100
-5.0V
Diode Used For
Turn-off Test Only
+V_{CC}
R_C
160 k
To Scope
t_r < 2.0 ns
51

Note: V_{CC} and R_C adjusted for $V_{CE(off)}$ = 150 V and I_C as desired, R_B chosen for desired I_{B1}, V_1 = 10V

FIGURE 10 – CURRENT-GAIN–BANDWIDTH PRODUCT

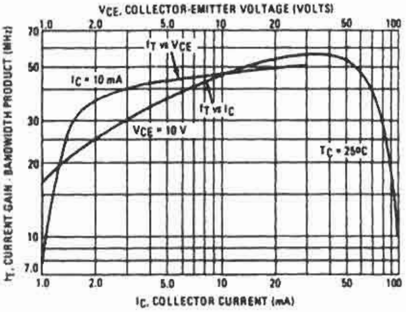


FIGURE 11 – OUTPUT ADMITTANCE

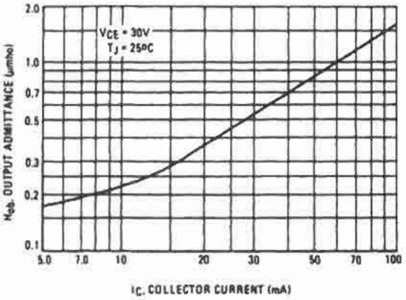
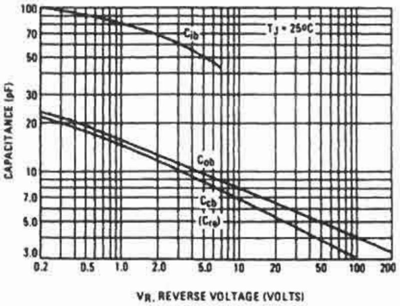


FIGURE 12 – CAPACITANCE



2N3439, 2N3440 (continued)

FIGURE 13 – TYPICAL THERMAL RESPONSE

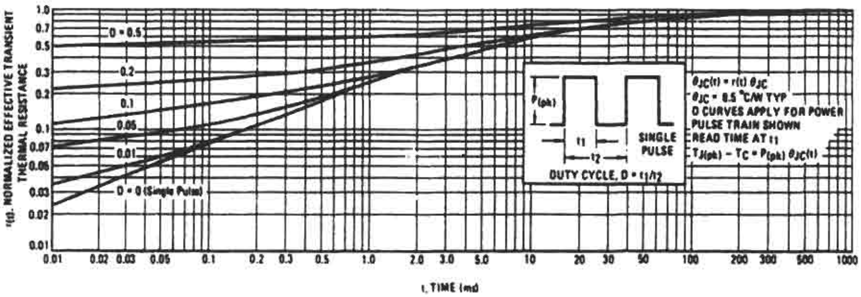


FIGURE 14 – ACTIVE-REGION SAFE OPERATING AREA

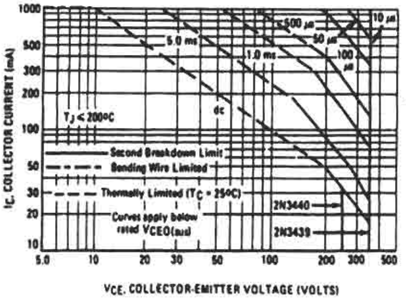
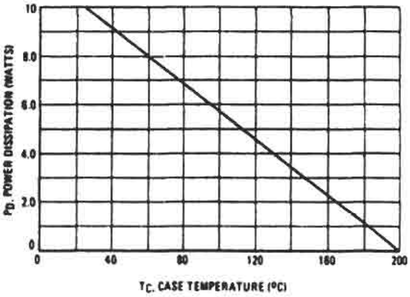


FIGURE 15 – POWER DERATING



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 14 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ = 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

2N3444 (SILICON)

For Specifications, See 2N3252 Data.

APPENDIX 10

Thermal Calculations for Transistors

The material in this appendix will enable you to compare the specifications of a given transistor with the requirements of a given application, and to make a judgment regarding the use of heat sinks. You will be able to determine whether a heat sink is required and, if it is, to specify the one needed.

When current flows through a semiconductor device, heat is generated. In the case of a forward-biased transistor, most of the heat is generated in the collector-base junction. The manufacturer specifies a maximum temperature (T_j) for the internal junction. Operation at higher temperatures will likely damage the transistor.

To keep the junction at an acceptable temperature, it is necessary to provide a path for the heat to escape the junction and reach the ambient air. As the heat travels from the junction to the air, it encounters opposition, or *thermal resistance.* There is thermal resistance between the junction and the case (θ_{JC}), resistance between the case and the heat sink (θ_{CS}), and apparent resistance between the heat sink and the ambient air (θ_{SA}). The sum of these thermal resistances is the total thermal resistance between the junction and the ambient air (θ_{JA}). In equation form, we have

$$\boxed{\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \qquad \text{(A10.1)}}$$

In the case of a transistor with no heat sink, the total thermal resistance between the junction and the ambient air (θ_{JA}) is the sum of the junction-to-case thermal resistance (θ_{JC}) plus an effective resistance called *case-to-air* (θ_{CA}). The primary mechanism for heat transfer between the junction and the case is through conduction. From the case to the air, on the other hand, the mechanism is primarily radiation and convection, which appears as a much higher thermal resistance.

The manufacturer's data sheet will normally provide the value of junction-to-case thermal resistance (θ_{JC}). The overall junction-to-ambient thermal resistance (θ_{JA}), on the other hand, is not always provided. Table A10.1 can be used as an estimate of θ_{JA} if the exact value is not available in the data sheet.

TABLE A10.1

Transistor Case Style	*Thermal Resistance (°C/W)*
TO-3	32
TO-5	150
TO-18	300
TO-39	150
TO-66	62
TO-220	50

The thermal resistance between the heat sink and the air (θ_{SA}) is provided by the manufacturer of the heat sink. The value of thermal resistance between the transistor case and the heat sink (θ_{CS}) depends upon how the transistor is mounted to the heat sink—that is, whether the transistor is screwed directly to the heat sink (metal-to-metal), whether heat-conductive grease is used, whether an insulating wafer is used, and even how securely the mounting screws are tightened. Table A10.2 provides representative values for θ_{CS} under different mounting conditions for two of the most common power transistor packages.

The power dissipated in the collector-base junction can be estimated with Equation (A10.2):

$$\boxed{P_D = I_C V_{CE} \qquad \text{(A10.2)}}$$

where I_C and V_{CE} are DC or average values. The maximum power that can be dissipated in a junction without the use of an external heat sink can be determined with Equation (A10.3):

$$\boxed{P_D = \frac{T_j(\max) - T_A}{\theta_{JA}} \qquad \text{(A10.3)}}$$

where T_j(max) is the highest design temperature (not necessarily the highest temperature allowed by the manufacturer), T_A is the highest ambient air temperature

TABLE A10.2

Case Style	*Dry Metal Contact*	*Heat Compound*	*Insulating Wafer*
TO-3	0.5°C/W	0.12°C/W	0.36°C/W
TO-220	1.2°C/W	1.0°C/W	1.7°C/W

to be encountered, and θ_{JA} is the junction-to-air thermal resistance described previously.

For a particular application, the required junction-to-air thermal resistance (whether a heat sink is used or not) can be determined with Equation (A10.4).

$$\theta_{JA}(\textit{required}) = \frac{T_j(\max) - T_A}{P_D} \tag{A10.4}$$

If the required value for θ_{JA} is less than the value of θ_{JC}, then a transistor with a higher power rating must be used. In other words, even if we had a perfect heat sink, the junction temperature would still exceed the $T_j(\max)$ limit. If the required value for θ_{JA} is greater than the actual θ_{JA} (Table A10.1) for the particular package being considered, no heat sink will be needed.

If a heat sink is needed for a particular application, then the required value of thermal resistance for the heat sink (θ_{SA}) is determined by Equation (A10.5).

$$\theta_{SA} = \theta_{JA}(\textit{required}) - \theta_{JC} - \theta_{CS} \tag{A10.5}$$

The transistor manufacturer does not always include values for θ_{JC} and/or θ_{JA} in the data sheet. However, the derating factor is usually available. The thermal resistance for either junction-to-case or junction-to-air is equal to the reciprocal of the respective derating factor. That is,

$$\theta_{JC} = \frac{1}{\rho_C} \tag{A10.6}$$

where ρ_C is the derating factor for the case temperature. Similarly,

$$\theta_{JA} = \frac{1}{\rho_A} \tag{A10.7}$$

where ρ_A is the derating factor for ambient air.

Example 1

A particular transistor has a quiescent collector current of 1.2 amps and a quiescent collector-to-emitter voltage of 12 volts. The design goal allows a maximum junction temperature of 140°C and a maximum ambient temperature of 65°C. Determine whether this transistor can be used in this application. If it can, does it need a heat sink? If so, what is the required thermal resistance of the heat sink?

Solution. The manufacturer's data sheet provides the following information:

1. θ_{JC}	1.8°C/W
2. T_j(rating)	–55 to +150°C
3. Package	TO-220

The power actually dissipated in the junction can be estimated with Equation (A10.2) as

$$P_D = I_C V_{CE} = 1.2\ A \times 12\ V = 14.4\ W$$

The required thermal resistance from junction-to-air is estimated with Equation (A10.4).

$$\theta_{JA}(required) = \frac{T_j(\max) - T_A}{P_D} = \frac{140°\text{C} - 65°\text{C}}{14.4W} = 5.21°\text{C}/W$$

Since the required value of θ_{JA} is greater than θ_{JC}, this transistor can be used for this application. Table A10.1 lists the value of θ_{JA} for a TO-220 package as 50°C/W. Since the required value of θ_{JA} is less than the value of θ_{JA} for the package itself, a heat sink will be required. It will need a thermal resistance as determined by Equation (A10.5).

$$\theta_{SA} = 5.21°\text{C/W} - 1.8°\text{C/W} - 1.7°\text{C/W} = 1.71°\text{C/W}$$

Example 2

A certain transistor has the following thermal characteristics listed on the manufacturer's data sheet:

1. θ_{JC}	3.125°C/W
2. T_j(max)	150°C
3. Package	TO-3

What is the most power that can be dissipated at room temperature (25°C) without requiring a heat sink?

Solution. The maximum power without a heat sink can be estimated with Equation (A10.3) as

$$P_D = \frac{T_j(\max) - T_A}{\theta_{JA}} = \frac{150°\text{C} - 25°\text{C}}{32°\text{C}/W} = 3.91\ W$$

Example 3

A particular design requires an NPN transistor to conduct 75 milliamperes with a collector-to-emitter voltage of 15 volts. The highest ambient temperature is expected to be 70°C, and it is a goal to keep the junction at 125°C or below. Can a 2N2222A transistor be used in this application? If so, is a heat sink required? If a heat sink is required, what is its required thermal resistance (θ_{SA})?

Solution. The manufacturer's data sheet for a 2N2222A provides the following information:

1. T_j(max)	200°C
2. Package	TO-18
3. I_C(max)	0.8 amps
4. V_{CE}(max)	40 volts
5. Derating factor above $T_C = 25°C$	12 mW/°C
6. Derating factor above $T_A = 25°C$	3.33 mW/°C

The required junction-to-air resistance can be computed with Equation (A10.4) as

$$\begin{aligned}\theta_{JA}(required) &= \frac{T_j(\max) - T_A}{P_D} \\ &= \frac{125°C - 70°C}{75\ mA \times 15\ V} \\ &= 48.9°C\,/\,W\end{aligned}$$

The junction-to-case thermal resistance can be computed with Equation (A10.6) as

$$\theta_{JC} = \frac{1}{\rho_C} = \frac{1}{12\ mW\,/\,°C} = 83.3°C\,/\,W$$

Since the required θ_{JA} is less than the θ_{JC} of the transistor, we cannot use this device; it would overheat even with an ideal heat sink.

APPENDIX 11

Interpretation of Oscilloscope Displays

Numerous examples throughout the text include an oscilloscope display to reveal the operational characteristics of the actual circuit. All of these figures are actual plotted outputs from a digitizing oscilloscope. Although much of the display output is similar to more familiar analog oscilloscopes, Figure A11.1 and the following descriptions will assist the reader who is unfamiliar with this type of equipment.

Each of the following headings describes the purpose of the corresponding item in Figure A11.1.

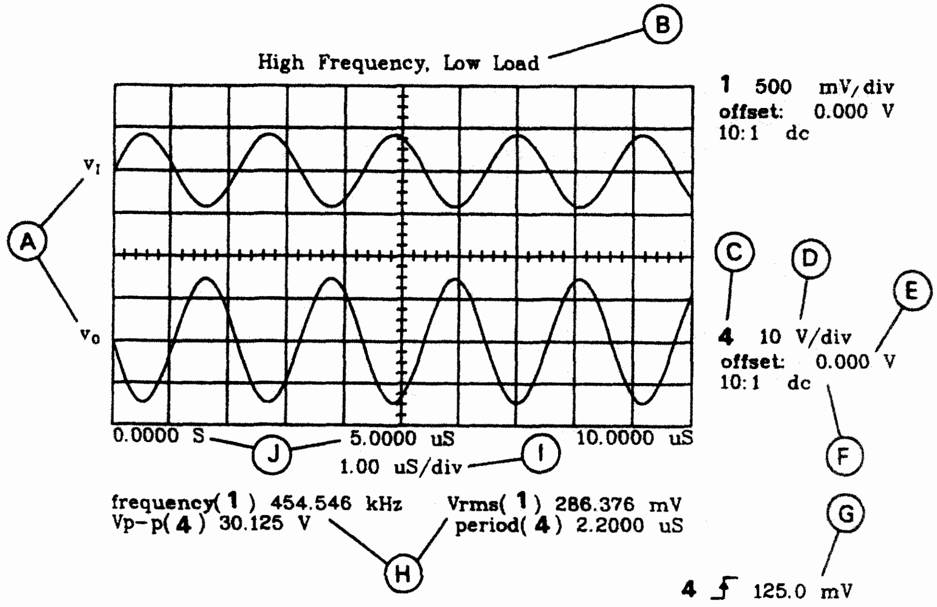


FIGURE A11.1 Identification of important areas on the digitizing oscilloscope displays.

Item A. This is a reference to the schematic diagram. The annotations indicate where on the circuit each waveform was taken.

Item B. This annotation provides a brief description of the circuit conditions at the time of the measurements. Descriptions include such things as relative frequency, relative line voltage, or load conditions.

Item C. The oscilloscope is a four-channel device. That is, it is capable of displaying four different waveforms at the same time. The larger, bold numbers indicate which channel is associated with the subsequent parameter list.

Item D. This displays the vertical sensitivity of the indicated channel. It has the same meaning as the Volts/cm or Volts/Division parameter on an analog oscilloscope.

Item E. The offset specification indicates the amount of DC offset that has been set into the indicated channel. A positive offset has the effect of moving the waveform upward; a negative offset shifts the waveform downward. In either case, the amount of shift is established by the Volts/Division setting (Item D).

Item F. This ratio indicates the type of probe being used (e.g., 1:1 or 10:1). The attenuation effects of the probe are automatically accounted for in the display, so no mental arithmetic is required to obtain the correct answer. Additionally, the type of coupling (AC or DC) is displayed.

Item G. This portion of the display describes the trigger conditions. First, the larger, bold number indicates which channel served as the trigger source. Second, the arrow, pointing up or down on the rising or falling edge, respectively, indicates the slope of the trigger (i.e., positive or negative). Finally, the voltage value is the setting for the trigger level.

Item H. The lower portion of each display will vary depending on what characteristics of the displayed waveform are of interest. Each of the listed parameters will have a larger, bold number to indicate the channel reference. The remaining descriptive label and value are self-explanatory. Some example parameters include frequency, +width (positive pulse width), –width (negative pulse width), period, Vrms, Vavg, Vp-p, Vmin, Vmax, and so on.

Item I. This is the Time/Division setting for the horizontal sweep of the oscilloscope. It is interpreted in the same way as the Time/cm or Time/Division setting on an analog oscilloscope.

Item J. These labels simply indicate the relative time at various points across the screen (i.e., left, center, and right).

A few figures in the text (e.g., Figure 3.16) have some additional dashed lines superimposed on the oscilloscope display. These are used for measuring the time (horizontal) and voltage (vertical) between two points on the waveform. When the lines are visible, there are normally corresponding time and/or voltage parameters listed in the lower portion of the display (in the area indicated by item H in Figure A11.1). These additional parameters are each associated with a particular channel and include such measurements as these:

Vmarker1 indicates the voltage level represented by one of the horizontal dashed lines.

Vmarker2 is the voltage level of the second horizontal dashed line.

delta V is the difference in voltage between the levels of Vmarker2 and Vmarker1.

start marker is the time position (as indicated by item J in Figure A11.1) of one of the vertical dashed lines.

stop marker is the time position of the second vertical dashed line.

delta t is the difference in time between the setting of the stop marker and the start marker described.

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